

# Processors, FPGAs, and ASICs

## Part 2: Processors to Fixed-Function

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# Spectrum of IC choices

**Flexible, efficient**

**You choose**



Full Custom

Polygons (Intel)

ASIC

Circuit (Sony)

Gate Array

Wires

FPGA

Logic network

PLD

Logic function

GP Processor

Program (e.g., ARM)

SP Processor

Program (e.g., DSP)

Multifunction

Settings (e.g., Accelerometer)

Fixed-function

Part number (e.g., 7400)

**Cheap, quick to design**

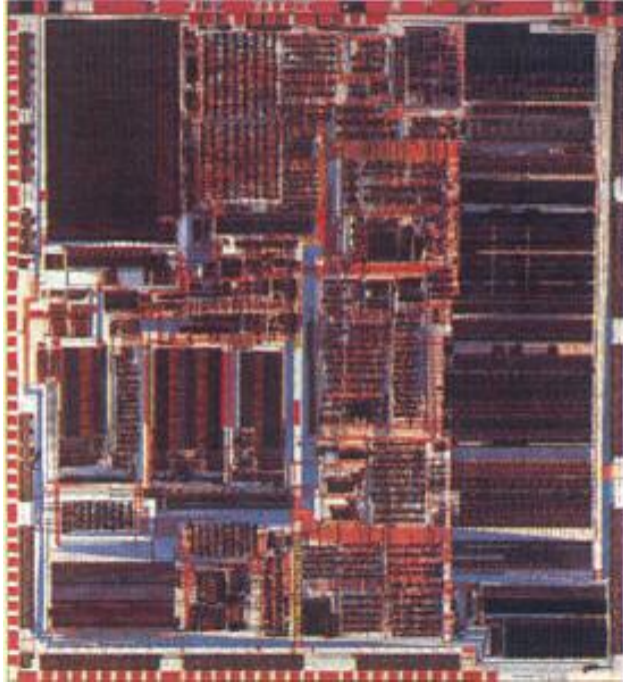
Euclid



## Euclid's Algorithm

```
int gcd(int m, int n)
{
    int r;
    while ((r = m % n) != 0) {
        m = n;
        n = r;
    }
    return n;
}
```

The  
Intel  
80386  
c. 1985



# i386 Programmer's Model

31	0	
eax		Mostly
ebx		General-
ecx		Purpose
edx		Registers
esi		Source index
edi		Destination index
ebp		Base pointer
esp		Stack pointer
eflags		Status word
eip		Instruction Pointer

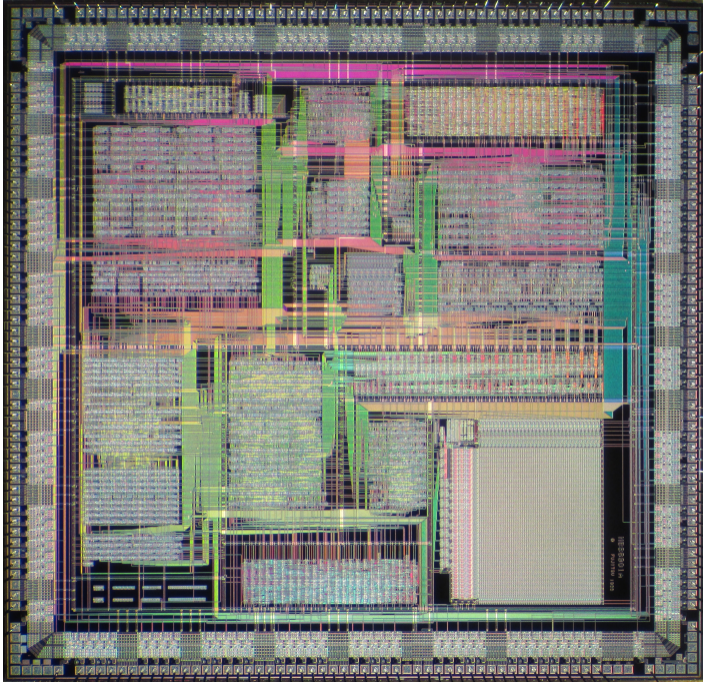
15	0	
cs		Code segment
ds		Data segment
ss		Stack segment
es		Extra segment
fs		Data segment
gs		Data segment

## Euclid on the i386

```
int gcd(int m, int n)
{
    int r;
    while ((r = m % n) != 0) {
        m = n;
        n = r;
    }
    return n;
}
```

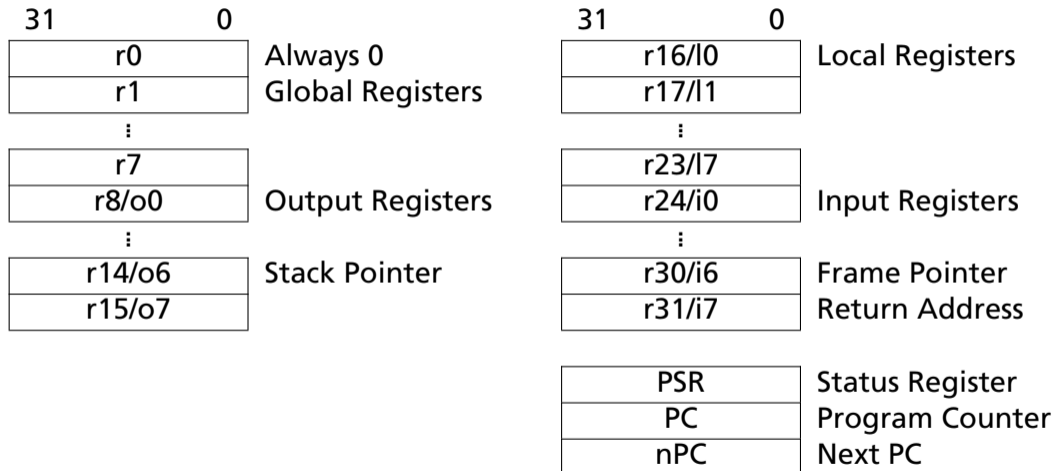
```
gcd:  pushl  %ebp
      movl  %esp,%ebp
      pushl %ebx
      movl  8(%ebp),%eax
      movl  12(%ebp),%ecx
      jmp   .L6
.L4:  movl  %ecx,%eax
      movl  %ebx,%ecx
.L6:  cld
      idivl %ecx
      movl  %edx,%ebx
      testl %edx,%edx
      jne  .L4
      movl  %ecx,%eax
      movl  -4(%ebp),%ebx
      leave
      ret
```

Sun's  
SPARC  
Processor  
c. 1987





# SPARC Programmer's Model

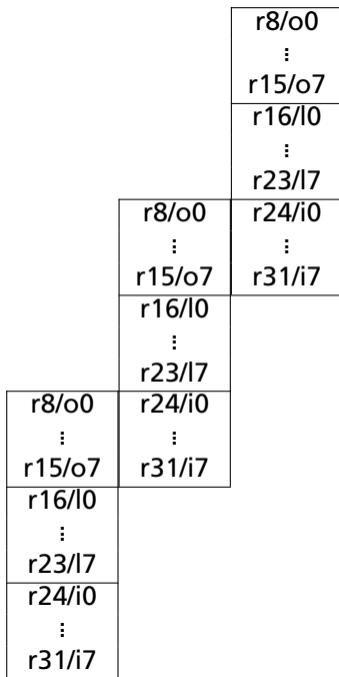


# SPARC Register Windows

The output registers of the calling procedure become the inputs to the called procedure

The global registers remain unchanged

The local registers are not visible across procedures

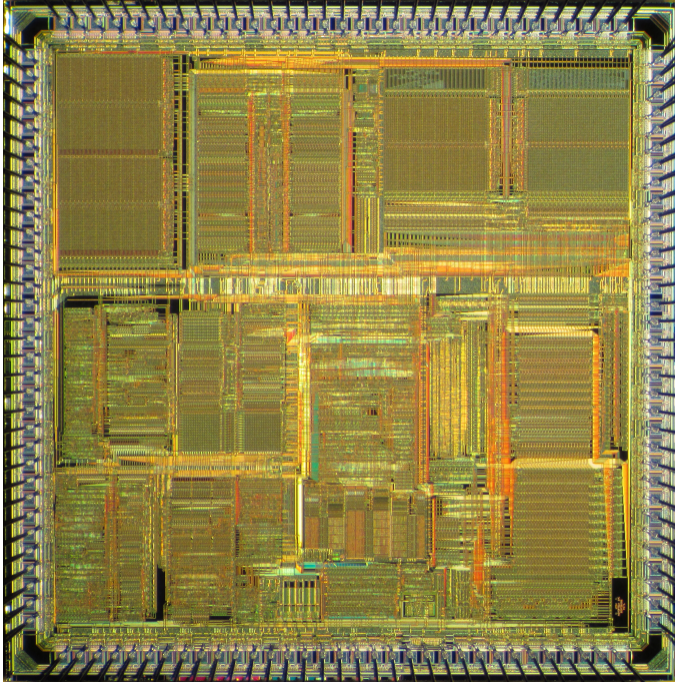


## Euclid on the SPARC

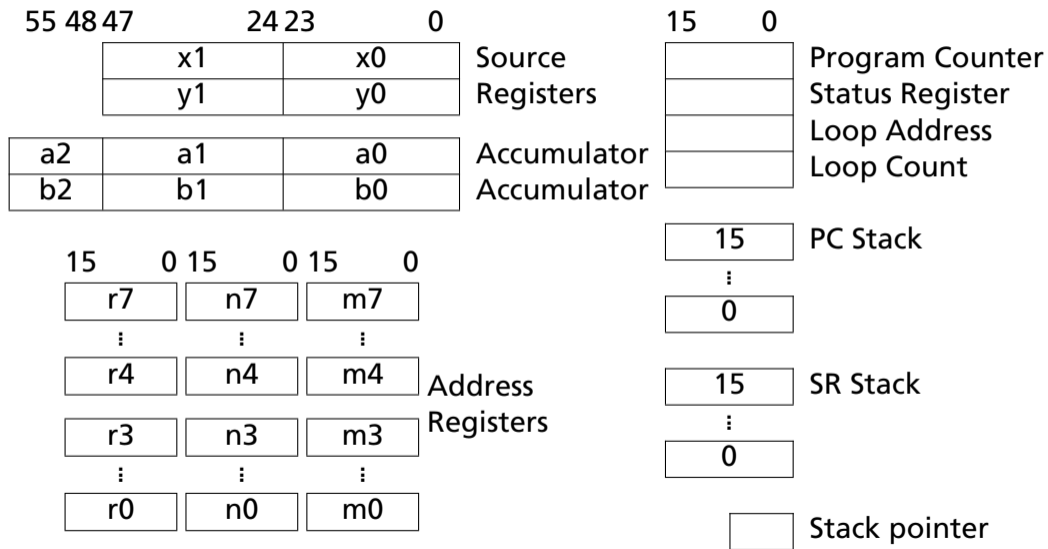
```
int gcd(m, n)
int m, n;
{
    int r;
    while ((r = m % n) != 0) {
        m = n;
        n = r;
    }
    return n;
}
```

```
gcd: save    %sp,-96,%sp
      mov    %i0,%o0
      call   .rem,2
      mov    %i1,%o1
      mov    %o0,%i5
      tst    %i5
      be    L2
L1:   mov    %i1,%o0
      call   .rem,2
      mov    %i1,%o1
      mov    %o0,%i5
      tst    %i5
      bne,a  L1
      mov    %i1,%o0
L2:   ret
      restore %g0,%i1,%o0
```

Motorola's  
DSP56000  
c. 1986

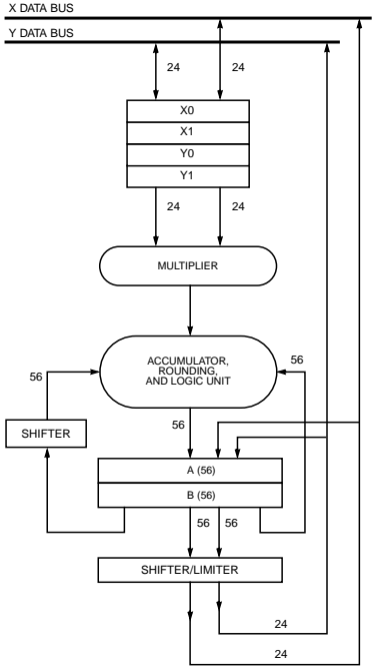


# DSP 56000 Programmer's Model

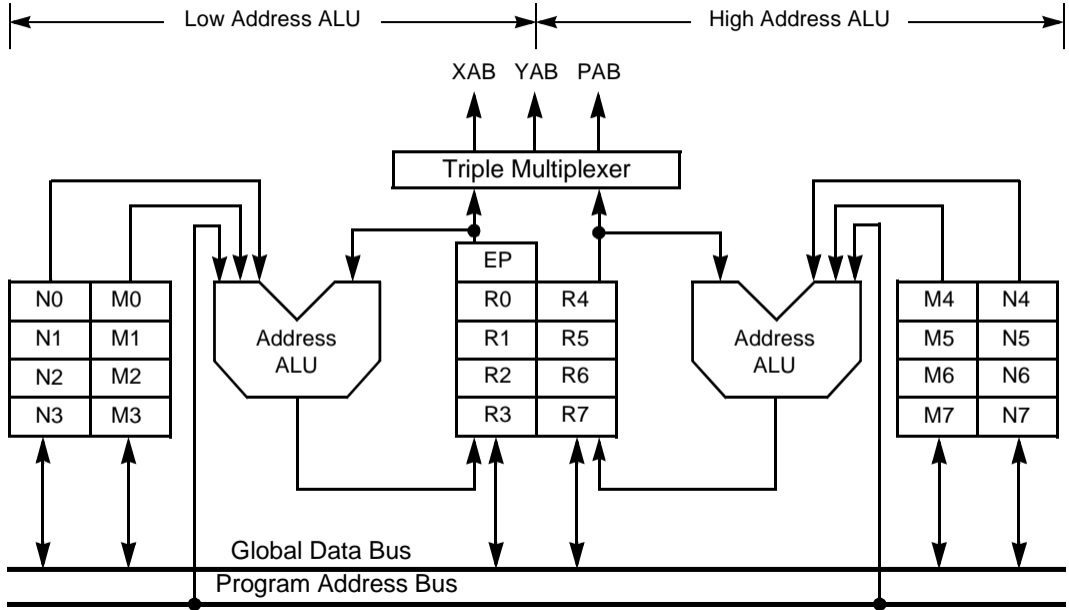


# Motorola DSP56000

## Data ALU



# Motorola DSP56000 AGU



## FIR Filter in 56000

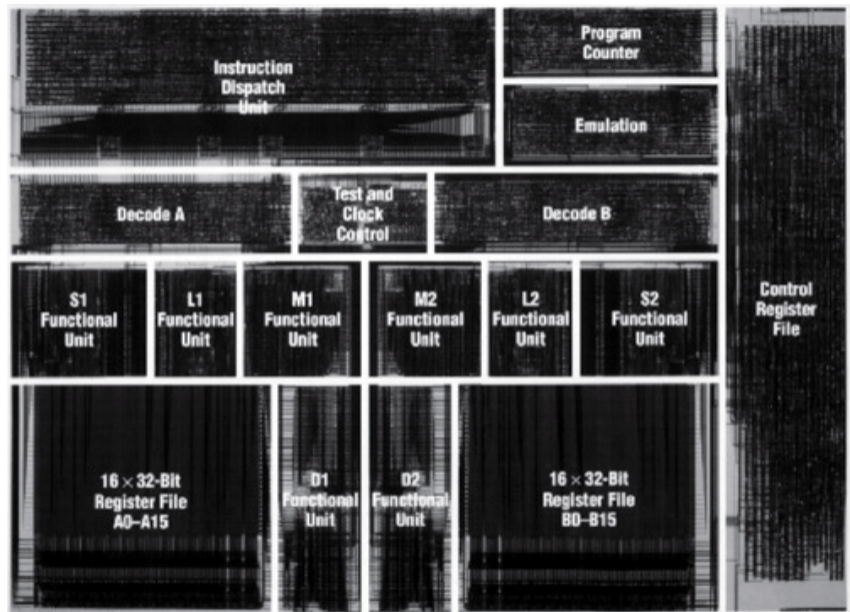
```
move  #samples, r0
move  #coeffs, r4
move  #n-1, m0
move  m0, m4
movep y:input, x:(r0)
clr   a          x:(r0)+, x0  y:(r4)+, y0

rep   #n-1
mac   x0,y0,a    x:(r0)+, x0  y:(r4)+, y0

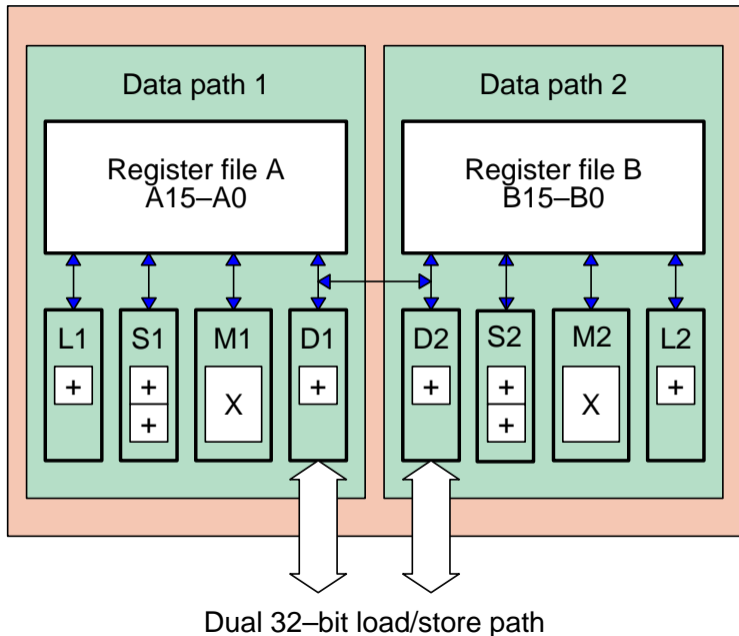
macr  x0,y0,a    (r0)-
movep a, y:output
```



TI  
TMS320  
C6201  
VLIW  
DSP  
c. 1997



TI  
TMS320  
C6000  
VLIW  
DSP



## FIR in One 'C6 Assembly Instruction

FIRLOOP:

```
          LDH .D1  *A1++, A2  ; Fetch next sample
||        LDH .D2  *B1++, B2  ; Fetch next coefficient
|| [B0]  SUB .L2  B0, 1, B0   ; Decrement loop count
|| [B0]  B   .S2  FIRLOOP    ; Branch if non-zero
||        MPY .M1X A2, B2, A3  ; Sample × Coefficient
||        ADD .L1  A4, A3, A4  ; Accumulate result
```

## FIR in One 'C6 Assembly Instruction

FIRLOOP:

```
          LDH .D1  *A1++, A2  ; Fetch next sample
||        LDH .D2  *B1++, B2  ; Fetch next coefficient
|| [B0]  SUB .L2  B0, 1, B0   ; Decrement loop count
|| [B0]  B   .S2  FIRLOOP    ; Branch if non-zero
||        MPY .M1X A2, B2, A3  ; Sample × Coefficient
||        ADD .L1  A4, A3, A4  ; Accumulate result
```




Run in parallel

## FIR in One 'C6 Assembly Instruction

Load a halfword (16 bits)

FIRLOOP:



```
LDH .D1 *A1++, A2 ; Fetch next sample
|| LDH .D2 *B1++, B2 ; Fetch next coefficient
|| [B0] SUB .L2 B0, 1, B0 ; Decrement loop count
|| [B0] B .S2 FIRLOOP ; Branch if non-zero
|| MPY .M1X A2, B2, A3 ; Sample × Coefficient
|| ADD .L1 A4, A3, A4 ; Accumulate result
```

## FIR in One 'C6 Assembly Instruction

Do this on unit D1  
↓

```
FIRLOOP:
    LDH .D1 *A1++, A2 ; Fetch next sample
||     LDH .D2 *B1++, B2 ; Fetch next coefficient
|| [B0] SUB .L2 B0, 1, B0 ; Decrement loop count
|| [B0] B .S2 FIRLOOP ; Branch if non-zero
||     MPY .M1X A2, B2, A3 ; Sample × Coefficient
||     ADD .L1 A4, A3, A4 ; Accumulate result
```

## FIR in One 'C6 Assembly Instruction

FIRLOOP:

```
          LDH .D1  *A1++, A2  ; Fetch next sample
||        LDH .D2  *B1++, B2  ; Fetch next coefficient
|| [B0]  SUB .L2  B0, 1, B0  ; Decrement loop count
|| [B0]  B   .S2  FIRLOOP   ; Branch if non-zero
||        MPY .M1X A2, B2, A3  ; Sample × Coefficient
||        ADD .L1  A4, A3, A4  ; Accumulate result
```

↑  
Use the cross path

## FIR in One 'C6 Assembly Instruction

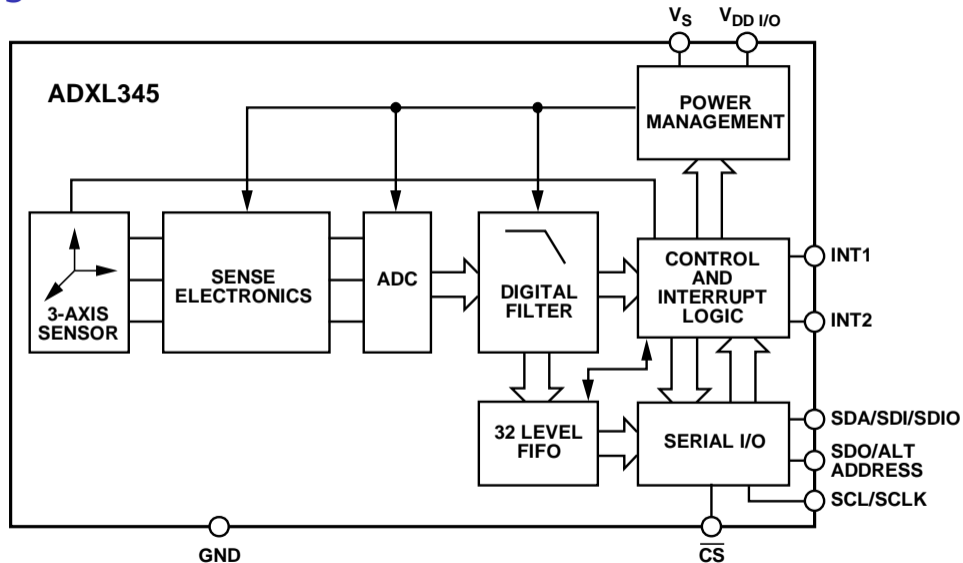
FIRLOOP:

```
          LDH .D1  *A1++, A2  ; Fetch next sample
||        LDH .D2  *B1++, B2  ; Fetch next coefficient
|| [B0]  SUB .L2  B0, 1, B0   ; Decrement loop count
|| [B0]  B      .S2  FIRLOOP ; Branch if non-zero
||      ↑      MPY .M1X A2, B2, A3 ; Sample × Coefficient
||      |      ADD .L1  A4, A3, A4 ; Accumulate result
```

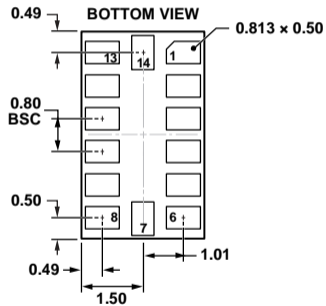
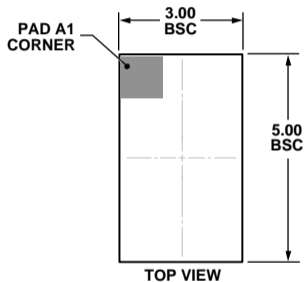
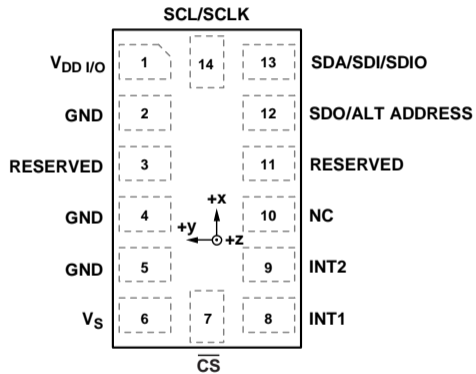
Predicated instruction (only if B0 non-zero)



# Analog Devices ADXL345 Accelerometer



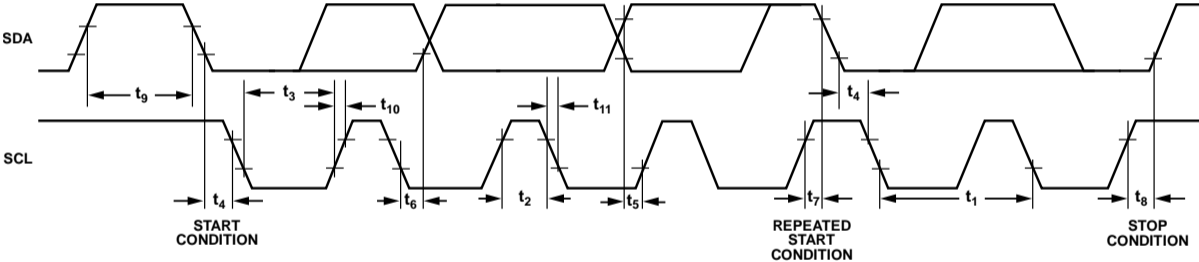
# 14 pins, 3mm by 5mm



# DE1-SoC Connections to the ADXL345 Accelerometer



# I<sup>2</sup>C Bus Protocol



# ADXL345 Registers (30, 8-bit)

Address		Name	Type	Reset Value	Description
Hex	Dec				
0x00	0	DEVID	R	11100101	Device ID
0x01 to 0x1C	1 to 28	Reserved			Reserved; do not access
0x1D	29	THRESH_TAP	R/W	00000000	Tap threshold
0x1E	30	OFSX	R/W	00000000	X-axis offset
0x1F	31	OFSY	R/W	00000000	Y-axis offset
0x20	32	OFSZ	R/W	00000000	Z-axis offset
0x21	33	DUR	R/W	00000000	Tap duration
0x22	34	Latent	R/W	00000000	Tap latency
0x23	35	Window	R/W	00000000	Tap window
0x24	36	THRESH_ACT	R/W	00000000	Activity threshold
0x25	37	THRESH_INACT	R/W	00000000	Inactivity threshold
0x26	38	TIME_INACT	R/W	00000000	Inactivity time
0x27	39	ACT_INACT_CTL	R/W	00000000	Axis enable control for activity and inactivity detection
0x28	40	THRESH_FF	R/W	00000000	Free-fall threshold
0x29	41	TIME_FF	R/W	00000000	Free-fall time
0x2A	42	TAP_AXES	R/W	00000000	Axis control for single tap/double tap
0x2B	43	ACT_TAP_STATUS	R	00000000	Source of single tap/double tap
0x2C	44	BW_RATE	R/W	00001010	Data rate and power mode control
0x2D	45	POWER_CTL	R/W	00000000	Power-saving features control
0x2E	46	INT_ENABLE	R/W	00000000	Interrupt enable control
0x2F	47	INT_MAP	R/W	00000000	Interrupt mapping control
0x30	48	INT_SOURCE	R	00000010	Source of interrupts
0x31	49	DATA_FORMAT	R/W	00000000	Data format control
0x32	50	DATA0	R	00000000	X-Axis Data 0
0x33	51	DATA1	R	00000000	X-Axis Data 1
0x34	52	DATAY0	R	00000000	Y-Axis Data 0
0x35	53	DATAY1	R	00000000	Y-Axis Data 1
0x36	54	DATAZ0	R	00000000	Z-Axis Data 0
0x37	55	DATAZ1	R	00000000	Z-Axis Data 1
0x38	56	FIFO_CTL	R/W	00000000	FIFO control
0x39	57	FIFO_STATUS	R	00000000	FIFO status

# Register Documentation (only 3 pages)

## REGISTER DEFINITIONS

### Register 0x00—DEVID (Read/Only)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	0	1	0	1

The DEVID register holds a final device ID code of 0x35 (345 octal).

### Register 0x10—THRESH\_TAP (Read/Write)

The THRESH\_TAP register is eight bits and holds the threshold value for detecting activity. The data format is unsigned, so the magnitude of the inactivity event is compared with the value in the THRESH\_INACT register. The scale factor is 62.5 mg/LSB. A value of 0 may result in undesirable behavior if the inactivity interrupt is enabled.

### Register 0x1E, Register 0x1F, Register 0x20—OFSX, OFSY, OFSZ (Read/Write)

The OFSX, OFSY, and OFSZ registers are each eight bits and offer user-set offset adjustments in two complement format with a scale factor of 15.6 mg/LSB (that is, 0x7F = 2 g). The value stored in the offset registers is automatically added to the acceleration data, and the resulting value is stored in the output data registers. For additional information regarding offset calibration and the use of the offset registers, refer to the Offset Calibration section.

### Register 0x21—DUR (Read/Write)

The DUR register is eight bits and contains an unsigned time value representing the maximum time that an event must be above the THRESH\_TAP threshold to qualify as a tap event. The scale factor is 62.5  $\mu$ s/LSB. A value of 0 disables the single tap/ double tap functions.

### Register 0x22—Latent (Read/Write)

The latent register is eight bits and contains an unsigned time value representing the wait time from the detection of a tap event to the start of the time window (defined by the window register) during which a possible second tap can be detected. The scale factor is 1.25 ms/LSB. A value of 0 disables the double tap function.

### Register 0x23—Window (Read/Write)

The window register is eight bits and contains an unsigned time value representing the amount of time after the expiration of the latency time (determined by the latent register) during which a second valid tap can begin. The scale factor is 1.25 ms/LSB. A value of 0 disables the double tap function.

### Register 0x24—THRESH\_FF (Read/Write)

The THRESH\_FF register is eight bits and holds the threshold value for detecting activity. The data format is unsigned, so the magnitude of the activity event is compared with the value in the THRESH\_INACT register. The scale factor is 62.5 mg/LSB. A value of 0 may result in undesirable behavior if the activity interrupt is enabled.

### Register 0x25—THRESH\_INACT (Read/Write)

The THRESH\_INACT register is eight bits and holds the threshold value for detecting activity. The data format is unsigned, so the magnitude of the inactivity event is compared with the value in the THRESH\_INACT register. The scale factor is 62.5 mg/LSB. A value of 0 may result in undesirable behavior if the inactivity interrupt is enabled.

### Register 0x26—TIME\_INACT (Read/Write)

The TIME\_INACT register is eight bits and contains an unsigned time value representing the amount of time that acceleration must be less than the value in the THRESH\_INACT register for inactivity to be declared. The scale factor is 1  $\mu$ s/LSB. Unlike the other interrupt functions, which use unfiltered data (see the Threshold section), the inactivity function uses filtered output data. At least one output sample must be generated for the inactivity interrupt to be triggered. This results in the function appearing unresponsive if the TIME\_INACT register is set to a value less than the time constant of the output data rate. A value of 0 results in an interrupt when the output data is less than the value in the THRESH\_INACT register.

### Register 0x27—INACT\_CTL (Read/Write)

D7	D6	D5	D4
ACT_x enable	ACT_y enable	ACT_z enable	
D3	D2	D1	D0
INACT_x enable	INACT_y enable	INACT_z enable	

### INACT\_AC/DC and INACT\_AC/DC Bits

A setting of 0 selects dc-coupled operation, and a setting of 1 enables ac-coupled operation. In dc-coupled operation, the current acceleration magnitude is compared directly with THRESH\_ACT and THRESH\_INACT to determine whether activity or inactivity is detected.

In ac-coupled operation for activity detection, the acceleration value at the start of activity detection is taken as a reference value. New samples of acceleration are then compared to this reference value, and if the magnitude of the difference exceeds the THRESH\_ACT value, the device triggers an activity interrupt. Similarly, in ac-coupled operation for inactivity detection, a reference value is used for comparison and is updated whenever the device exceeds the inactivity threshold. After the reference value is selected, the device compares the magnitude of the difference between the reference value and the current acceleration with THRESH\_INACT. If the difference is less than the value in THRESH\_INACT for the time in TIME\_INACT, the device is considered inactive and the inactivity interrupt is triggered.

## ACT\_x Enable Bits and INACT\_x Enable Bits

A setting of 1 enables x, y, or z-axis participation in detecting activity or inactivity. A setting of 0 excludes the selected axis from participation. If all axes are excluded, the function is disabled. For activity detection, all participating axes are logically ORed, causing the activity function to trigger when any of the participating axes exceeds the threshold. For inactivity detection, all participating axes are logically ANDed, causing the inactivity function to trigger only if all participating axes are below the threshold for the specified time.

### Register 0x28—THRESH\_FF (Read/Write)

The THRESH\_FF register is eight bits and holds the threshold value, in unsigned format, for free-fall detection. The acceleration on all axes is compared with the value in THRESH\_FF to determine if a free-fall event occurred. The scale factor is 62.5 mg/LSB. Note that a value of 0 mg may result in undesirable behavior if the free-fall interrupt is enabled. Values between 300 mg and 600 mg (0x05 to 0x09) are recommended.

### Register 0x29—TIME\_FF (Read/Write)

The TIME\_FF register is eight bits and stores an unsigned time value representing the minimum time that the value of all axes must be less than THRESH\_FF to generate a free-fall interrupt. The scale factor is 5 ms/LSB. A value of 0 may result in undesirable behavior if the free-fall interrupt is enabled. Values between 100 ms and 350 ms (0x14 to 0x46) are recommended.

### Register 0x2A—TAP\_AXES (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
Suppress	TAP_x enable	TAP_y enable	TAP_z enable				
0	0	0	0	0	0	0	0

## Suppress Bit

Setting the suppress bit suppresses double tap detection if acceleration greater than the value in THRESH\_TAP is present after activity. See the Tap Detection section for more details.

## TAP\_x Enable Bits

A setting of 1 in the TAP\_X enable, TAP\_Y enable, or TAP\_Z enable bit enables x, y, or z-axis participation in tap detection. A setting of 0 excludes the selected axis from participation in tap detection.

### Register 0x2B—ACT\_TAP\_STATUS (Read/Only)

D7	D6	D5	D4	D3	D2	D1	D0
ACT_x source	ACT_y source	ACT_z source	Asleep	TAP_x source	TAP_y source	TAP_z source	
0	0	0	0	0	0	0	0

## ACT\_x Source and TAP\_x Source Bits

These bits indicate the first axis involved in a tap or activity event. A setting of 1 corresponds to involvement in the event, and a setting of 0 corresponds to no involvement. When new data is available, these bits are not cleared but are overwritten by the new data. The ACT\_TAP\_STATUS register should be read before clearing the interrupt. Disabling an axis from participation clears the corresponding source bit when the next activity or single tap/double tap event occurs.

## Asleep Bit

A setting of 1 in the asleep bit indicates that the part is asleep, and a setting of 0 indicates that the part is not asleep. This bit toggles only if the device is configured for auto sleep. See the AUTO\_SLEEP BIT section for more information on auto sleep mode.

### Register 0x2C—BW\_RATE (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	LOW_POWER				Rate
0	0	0	0				

## LOW\_POWER Bit

A setting of 0 in the LOW\_POWER bit selects normal operation, and a setting of 1 selects reduced power operation, which has somewhat higher noise (see the Power Modes section for details).

## Rate Bits

These bits select the device bandwidth and output data rate (see Table 7 and Table 8 for details). The default value is 0x0A, which translates to a 100 Hz output data rate. An output data rate should be selected that is appropriate for the communication protocol and frequency selected. Selecting too high of an output data rate with a low communication speed results in samples being discarded.

### Register 0x2D—POWER\_CTL (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	Link	AUTO_SLEEP	Measure	Sleep	Wakeup	
0	0	0	0	0	0	0	0

## Link Bit

A setting of 1 in the link bit with both the activity and inactivity functions enabled delays the start of the activity function until inactivity is detected. After activity is detected, inactivity detection begins, preventing the detection of activity. This bit serially links the activity and inactivity functions. When this bit is set to 0, the inactivity and activity functions are concurrent. Additional information can be found in the Link Mode section.

When clearing the link bit, it is recommended that the part be placed into standby mode and then set back to measurement mode with a subsequent write. This is done to ensure that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the link bit is cleared may have additional noise, especially if the device was asleep when the bit was cleared.

## AUTO\_SLEEP BIT

If the link bit is set, a setting of 1 in the AUTO\_SLEEP bit enables the auto-sleep functionality. In this mode, the ADXL345 automatically switches to sleep mode if the inactivity function is enabled and inactivity is detected (that is, when acceleration is below the THRESH\_INACT value for at least the time indicated by TIME\_INACT). If activity is also enabled, the ADXL345 automatically wakes up from sleep after detecting activity and returns to operation at the output data rate set in the BW\_RATE register. A setting of 0 in the AUTO\_SLEEP bit disables automatic switching to sleep mode. See the description of the Sleep Bit in this section for more information on sleep mode.

If the link bit is not set, the AUTO\_SLEEP feature is disabled and setting the AUTO\_SLEEP bit does not have an impact on device operation. Refer to the Link Bit section or the Link Mode section for more information on utilization of the link feature.

When clearing the AUTO\_SLEEP bit, it is recommended that the part be placed into standby mode and then set back to measurement mode with a subsequent write. This is done to ensure that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the AUTO\_SLEEP bit is cleared may have additional noise, especially if the device was asleep when the bit was cleared.

## Measure Bit

A setting of 0 in the measure bit places the part into standby mode, and a setting of 1 places the part into measurement mode. The ADXL345 powers up in standby mode with minimum power consumption.

## Sleep Bit

A setting of 0 in the sleep bit puts the part into the normal mode of operation, and a setting of 1 places the part into sleep mode. Sleep mode suppresses DATA\_READY, stops transmission of data to FIFO, and switches the sampling rate to one specified by the wakeup bits. In sleep mode, only the activity function can be used. When the DATA\_READY interrupt is suppressed, the output data registers (Register 0x32 to Register 0x37) are still updated at the sampling rate set by the wakeup bits (D1:D0).

When clearing the sleep bit, it is recommended that the part be placed into standby mode and then set back to measurement mode with a subsequent write. This is done to ensure that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the sleep bit is cleared may have additional noise, especially if the device was asleep when the bit was cleared.

## Wakeup Bits

These bits control the frequency of readings in sleep mode as described in Table 20.

Table 20. Frequency of Readings in Sleep Mode

Setting		Frequency (Hz)
D1	D0	
0	0	8
0	1	4
1	0	2
1	1	1

### Register 0x2E—INT\_ENABLE (Read/Write)

D7	D6	D5	D4
DATA_READY	SINGLE_TAP	DOUBLE_TAP	Activity
D3 <td>D2</td> <td>D1</td> <td>D0</td>	D2	D1	D0
Inactivity	FREE_FALL	Watermark	Overrun

Setting bits in this register to a value of 1 enables their respective functions to generate interrupts, whereas a value of 0 prevents the functions from generating interrupts. The DATA\_READY, watermark, and overrun bits enable only the interrupt output; the functions are always enabled. It is recommended that interrupts be configured before enabling their outputs.

### Register 0x2F—INT\_MAP (R/W)

D7	D6	D5	D4
DATA_READY	SINGLE_TAP	DOUBLE_TAP	Activity
D3 <td>D2</td> <td>D1</td> <td>D0</td>	D2	D1	D0
Inactivity	FREE_FALL	Watermark	Overrun

Any bits set to 0 in this register send their respective interrupts to the INT1 pin, whereas bits set to 1 send their respective interrupts to the INT2 pin. All selected interrupts for a given pin are ORed.

### Register 0x30—INT\_SOURCE (Read/Only)

D7	D6	D5	D4
DATA_READY	SINGLE_TAP	DOUBLE_TAP	Activity
D3 <td>D2</td> <td>D1</td> <td>D0</td>	D2	D1	D0
Inactivity	FREE_FALL	Watermark	Overrun

Bits set to 1 in this register indicate that their respective functions have triggered an event, whereas a value of 0 indicates that the corresponding event has not occurred. The DATA\_READY, watermark, and overrun bits are always set if the corresponding events occur, regardless of the INT\_ENABLE register settings, and are cleared by reading data from the DATAX, DATAY, and DATAZ registers. The DATA\_READY and watermark bits may require multiple reads, as indicated in the FIFO mode description in the FIFO section. Other bits, and the corresponding interrupts, are cleared by reading the INT\_SOURCE register.

### Register 0x31—DATA\_FORMAT (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
SELF_TEST	SP1	INT_FORMAT	0	FULL_RES	Activity	Range	
0	0	0	0	0	0	0	0

The DATA\_FORMAT register controls the presentation of data to Register 0x32 through Register 0x37. All data, except that for the  $\pm 16$  g range, must be clipped to avoid rollover.

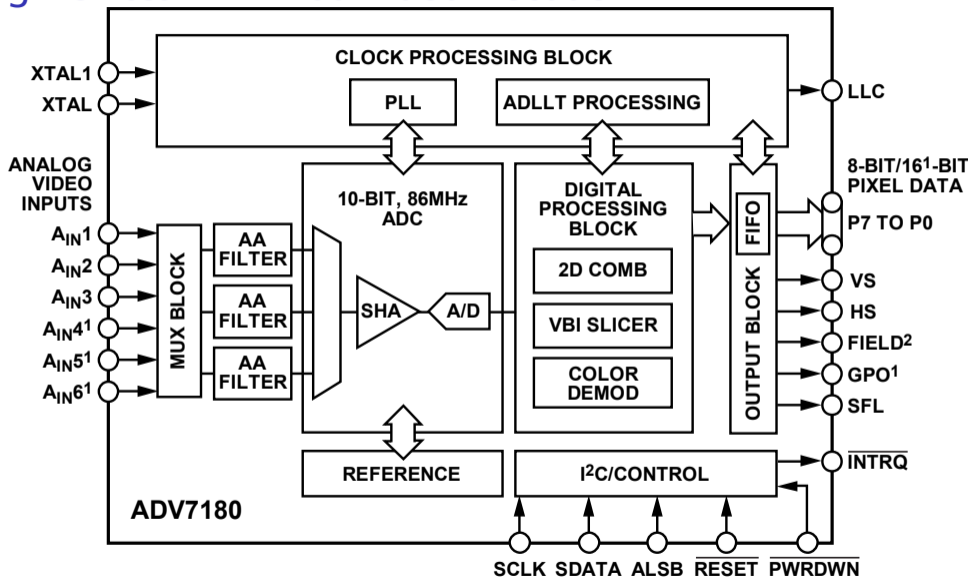
## SELF\_TEST Bit

A setting of 1 in the SELF\_TEST bit applies a self-test force to the sensor, causing a shift in the output data. A value of 0 disables the self-test force.

## SP1 Bit

A value of 1 in the SP1 bit sets the device to 3-wire SPI mode, and a value of 0 sets the device to 4-wire SPI mode.

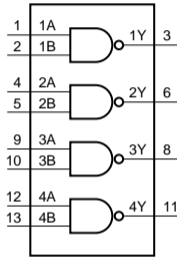
# Analog Devices ADV7180 Video Decoder



Address	Dec	Input Register Name	RW	7	6	5	4	3	2	1	0	Reset Value	Reset	
Dec	Hex											Value	(Hex)	
0	00	Input Control	RW	VID_SEL[3]	VID_SEL[2]	VID_SEL[1]	VID_SEL[0]	INSEL[3]	INSEL[2]	INSEL[1]	INSEL[0]	00000000	00	
1	01	Video Selection	RW	ENVSPLL	BETACAM	ENVSPHOC	SOPE					11001000	C8	
3	03	Output Control	RW	VBF_EN	TOD	OF_SEL[3]	OF_SEL[2]	OF_SEL[1]	OF_SEL[0]	SD_DUP_AV	00001100	C0		
4	04	Extended Output Control	RW	BT_056-4				TIM_OE	BL_C_VBI	EN_SPL_PFN	Range	01x0101	45	
5	05	Reserved												
6	06	Reserved												
7	07	Autodetect Enable	RW	AD_SEC525_EN	AD_SECAM_EN	AD_3443_EN	AD_360_EN	AD_PALN_EN	AD_PALM_EN	AD_NTSC_EN	AD_PAL_EN	01111111	7F	
8	08	Contrast	RW	CON[7]	CON[6]	CON[5]	CON[4]	CON[3]	CON[2]	CON[1]	CON[0]	10000000	80	
9	09	Reserved												
10	0A	Brightness	RW	BRE[7]	BRE[6]	BRE[5]	BRE[4]	BRE[3]	BRE[2]	BRE[1]	BRE[0]	00000000	00	
11	0B	Hue	RW	HUE[7]	HUE[6]	HUE[5]	HUE[4]	HUE[3]	HUE[2]	HUE[1]	HUE[0]	00000000	00	
12	0C	Default Value Y	RW	DEF_Y[3]	DEF_Y[2]	DEF_Y[1]	DEF_Y[0]	DEF_Y[3]	DEF_Y[2]	DEF_Y[1]	DEF_Y[0]	00110110	36	
13	0D	Default Value C	RW	DEF_C[7]	DEF_C[6]	DEF_C[5]	DEF_C[4]	DEF_C[3]	DEF_C[2]	DEF_C[1]	DEF_C[0]	01111000	7C	
14	0E	ADI Control 1	RW									00000000	00	
15	0F	Power Management	RW	RESET								00000000	00	
16	10	Status 1	R	CDL_RLL	AD_RESUL[2]	AD_RESUL[1]	AD_RESUL[0]	FOLLOW_PW	PSF_LOCK	LOST_LOCK	RL_LOCK			
17	11	IDENT	R	IDENT[7]	IDENT[6]	IDENT[5]	IDENT[4]	IDENT[3]	IDENT[2]	IDENT[1]	IDENT[0]	00011100	7C	
18	12	Status 2	R	PSF_ND[2]	PSF_ND[1]	LL_ND[2]	LL_ND[1]	MAN_AGE_DONE	MPFLD[2]	MPFLD[1]	MPFLD[0]			
19	13	Status 3	R	PAL_SW_LOCK	INTERLACED	STD_FL[2]	STD_FL[1]	FREE_RLN_ACT	Reserved	SD_OP_S0[4]	SEMO	INSTR_HLOCK		
20	14	Analog Clamp Control	RW									00010010	12	
21	15	Digital Clamp Control 1	RW	DCT[1]	DCT[0]	DCPE						00000000	00	
22	16	Reserved												
23	17	Shaping Filter Control 1	RW	CSFM[2]	CSFM[1]	CSFM[0]	YSFM[4]	YSFM[3]	YSFM[2]	YSFM[1]	YSFM[0]	00000001	01	
24	18	Shaping Filter Control 2	RW	WYSFM[6]	WYSFM[5]	WYSFM[4]	WYSFM[3]	WYSFM[2]	WYSFM[1]	WYSFM[0]		10010011	93	
25	19	Comb Filter Control	RW									11110001	F1	
29	1D	ADI Control 2	RW	TBI_LLC	ENBRXTAL							01000040	40	
29	1D	ADI Control 2	RW	TBI_LLC	ENBRXTAL							01000040	40	
37	27	Pixel Delay Control	RW	SWPC	AUTO_PDC_EN	CTA[2]	CTA[1]	CTA[0]				01011000	58	
43	2B	Misc Gain Control	RW	CRE								11110001	E1	
44	2C	AGC Mode Control	RW	LAG[2]	LAG[1]	LAG[0]						10101110	A6	
45	2D	Chroma Gain 1	R	CAG[1]	CAG[0]							11110000	F4	
46	2E	Chroma Gain 2	R	CMG[1]	CMG[0]							00000000	00	
47	2F	Luma Gain 1	R	LAG[1]	LAG[0]							1111xxxx	F0	
47	2F	Luma Gain 1	R	LAG[1]	LAG[0]							1111xxxx	F0	
48	30	Luma Gain Control 2	R	LMG[2]	LMG[1]	LMG[0]						xxxxxxxx	80	
48	30	Luma Gain 2	R	LMG[2]	LMG[1]	LMG[0]						xxxxxxxx	80	
49	31	VSyncField Control 1	RW									00010010	12	
50	32	VSyncField Control 2	RW	VSRHO	VSRHE							01000001	41	
51	33	VSyncField Control 3	RW	VSRHO	VSRHE							10000100	84	
52	34	HS Position Control 1	RW	HSR[6]	HSR[5]	HSR[4]	HSR[3]	HSR[2]	HSR[1]	HSR[0]		00000000	00	
53	35	HS Position Control 2	RW	HSR[7]	HSR[6]	HSR[5]	HSR[4]	HSR[3]	HSR[2]	HSR[1]	HSR[0]	00000000	02	
54	36	HS Position Control 3	RW	HSR[7]	HSR[6]	HSR[5]	HSR[4]	HSR[3]	HSR[2]	HSR[1]	HSR[0]	00000000	00	
55	37	Relaxity	RW	PHS	PPS							00000001	01	
56	38	NTSC Comb Control	RW	CTAPN[2]	CTAPN[0]	CCAN[2]	CCAN[1]	CCAN[0]	CCAN[3]	CCAN[2]	CCAN[1]	CCAN[0]	10000000	80
57	39	PAL Comb Control	RW	CTAPSP[1]	CTAPSP[0]	CCAMP[2]	CCAMP[1]	CCAMP[0]	CCAMP[3]	CCAMP[2]	CCAMP[1]	CCAMP[0]	11000000	C0
58	3A	ADC Control	RW									00010000	10	
61	3D	Manual Window Control	RW	CKLTH[3]	CKLTH[1]	CKLTH[0]						01110010	82	
65	41	Resample Control	RW	SPL_BV								00000001	01	
72	48	Gamma Control 1	RW	GDEC[15]	GDEC[14]	GDEC[13]	GDEC[12]	GDEC[11]	GDEC[10]	GDEC[9]	GDEC[8]	00000000	00	
73	49	Gamma Control 2	RW	GDEC[17]	GDEC[16]	GDEC[15]	GDEC[14]	GDEC[13]	GDEC[12]	GDEC[11]	GDEC[10]	00000000	00	
74	4A	Gamma Control 3	RW	GDEC[15]	GDEC[14]	GDEC[13]	GDEC[12]	GDEC[11]	GDEC[10]	GDEC[9]	GDEC[8]	00000000	00	
75	4B	Gamma Control 4	RW	GDEC[17]	GDEC[16]	GDEC[15]	GDEC[14]	GDEC[13]	GDEC[12]	GDEC[11]	GDEC[10]	00000000	00	
76	4C	Gamma Control 5	RW									xxxx0000	00	
77	4D	CTIDNR Control 1	RW									11011111	F7	
78	4E	CTIDNR Control 2	RW	CTL_C_TH[7]	CTL_C_TH[6]	CTL_C_TH[5]	CTL_C_TH[4]	CTL_C_TH[3]	CTL_C_TH[2]	CTL_C_TH[1]	CTL_C_TH[0]	00001000	08	
80	50	CTIDNR Control 4	RW	DNR_TH[7]	DNR_TH[6]	DNR_TH[5]	DNR_TH[4]	DNR_TH[3]	DNR_TH[2]	DNR_TH[1]	DNR_TH[0]	00001000	08	
81	51	Lock Count	RW	PSGLE	SRLS	COL[1]						01101000	84	
88	58	VSyncField Pre Control	RW									00000000	00	
89	59	General Purpose Outputs	RW									00000000	00	
143	8F	Free-Run Line Length 1	R		LLC_PAD_SEL[2]	LLC_PAD_SEL[1]	LLC_PAD_SEL[0]					00000000	00	
153	99	CLAP 1	R	CCAP[7]	CCAP[6]	CCAP[5]	CCAP[4]	CCAP[3]	CCAP[2]	CCAP[1]	CCAP[0]			
154	9A	CLAP 2	R	CCAP[7]	CCAP[6]	CCAP[5]	CCAP[4]	CCAP[3]	CCAP[2]	CCAP[1]	CCAP[0]			

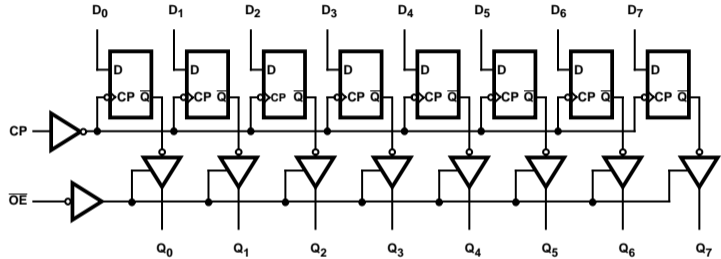


# Fixed-function: The 7400 series



7400

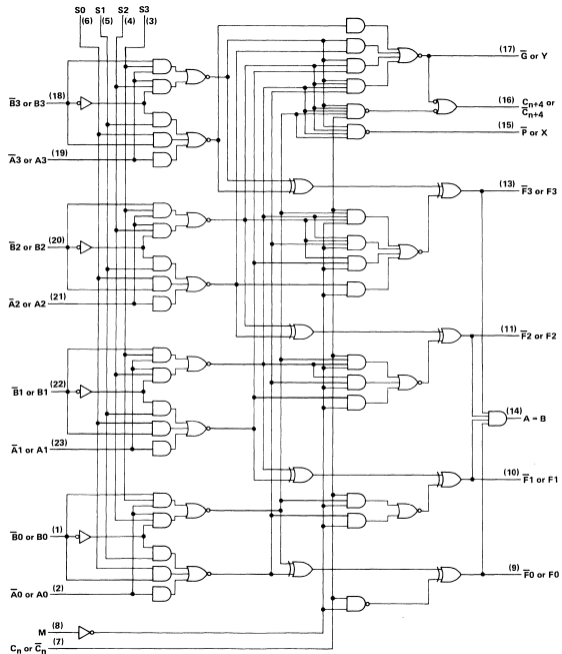
Quad NAND Gate



74374

Octal D Flip-Flop

# The 74181 4-bit ALU



The  
74181  
4-bit  
ALU

