

Facial Recognition using hardware accelerated Convolutional Neural Networks

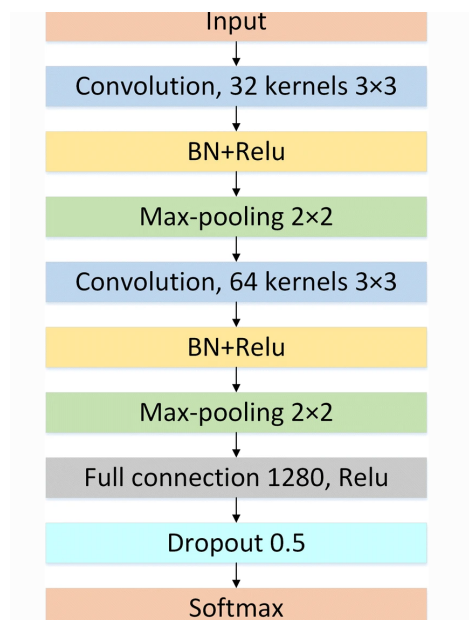
Ryan Kennedy (rdk2132), Felix Hanau (fjh2116), Daniel Cooke (dwc2122), Richard Mouradian (rom2110), Liam Bishop (lb3306)

Overview

The idea for our project is to make a Convolutional Neural Network accelerator for a Computer Vision Model which will perform facial recognition. Computer Vision models which rely on CNN's are very taxing on a processor because of the constant heavy computations needed to process images. To alleviate this we will get the FPGA to perform very fast and parallelized computations which may include but are not limited to convolution, max and softmax which will all be done on pixel matrices. We will use the software as a controller for the CNN which will take video input from a camera (peripheral) and feed it to the CNN one layer at a time taking the output from each layer as the input to the next. Upon completion of the final layer of computation we will get a probability vector which the software will process and decide what the image is. Finally we can set up a display to say whose face was recognized upon completion of the model and a decision has been made for who's face it sees.

CNN model Idea

SCNNB (Shallow Convolutional Neural Network with batch normalization)



The benefits of this Neural Network is the low memory footprint, computations and iterations for convergence which save both time and memory and will allow us to hopefully do the entire computation process on the fpga while maintaining the high accuracy associated with CNN's.

Peripherals

For inputs, we will be using a camera via USB to collect sample images of an object. We will also be using a button on the FPGA board to start recording samples. We will be using a display to show what's currently being viewed on the camera as well as a secondary image that will display what stored object the viewed object is similar to.

Software

Initially implement the CNN in software and use this to compare against the accelerated CNN in terms of performance, power consumption or accuracy. Add downscaling of images implemented in software if needed for performance. Receive output layer (e.g. probability vector indicating the most likely results) and use it to print the most likely result.

Hardware

Due to the highly parallelizable nature of the CNN computation we plan to use the FPGA as an accelerator for the FPGA. The most computationally intensive layers of the CNN can be accelerated to improve the performance of the CNN over using only the CPU. The software will feed images into the FPGA to be processed and then the probability of the image classification will be returned to the software and displayed to the user.

Milestones

Milestone 1: Full software implementation to serve as reference for accelerated CNN

April 3rd, 2022

Milestone 2: CNN Layer Modules done

April 17th, 2022

Milestone 3: Software Controller, Interface and Peripheral connection completed

April 31st, 2022