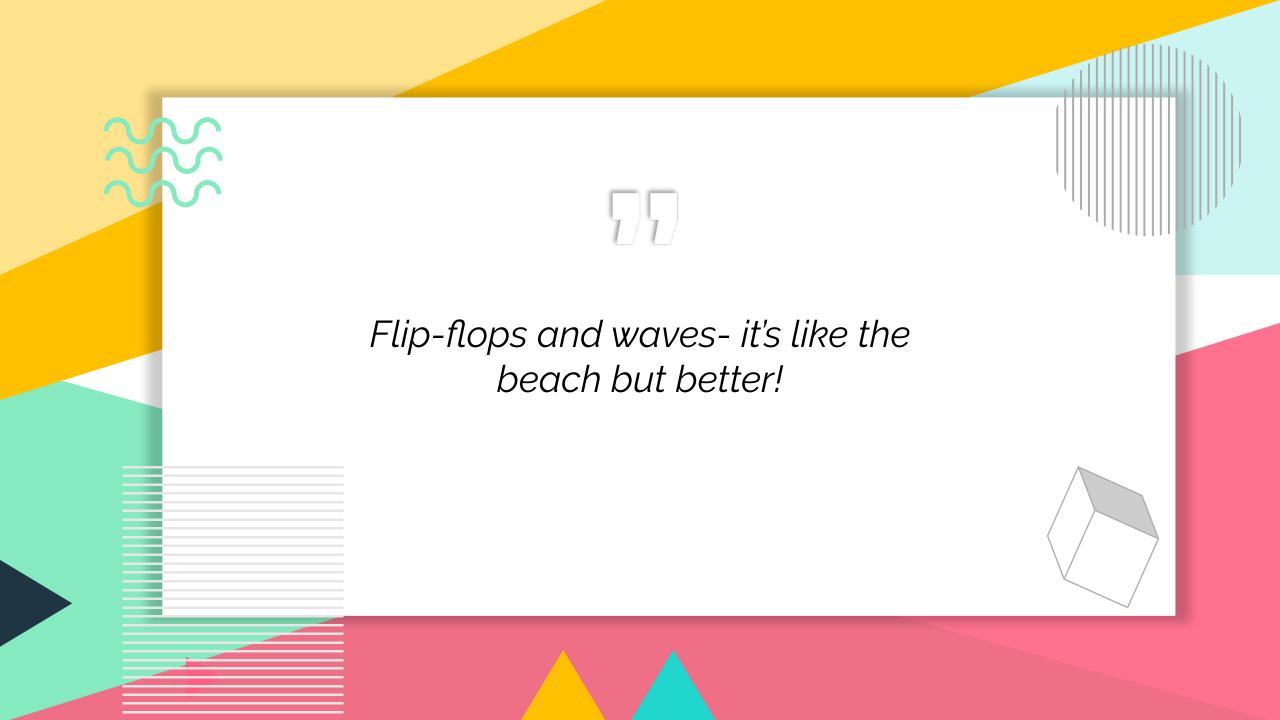
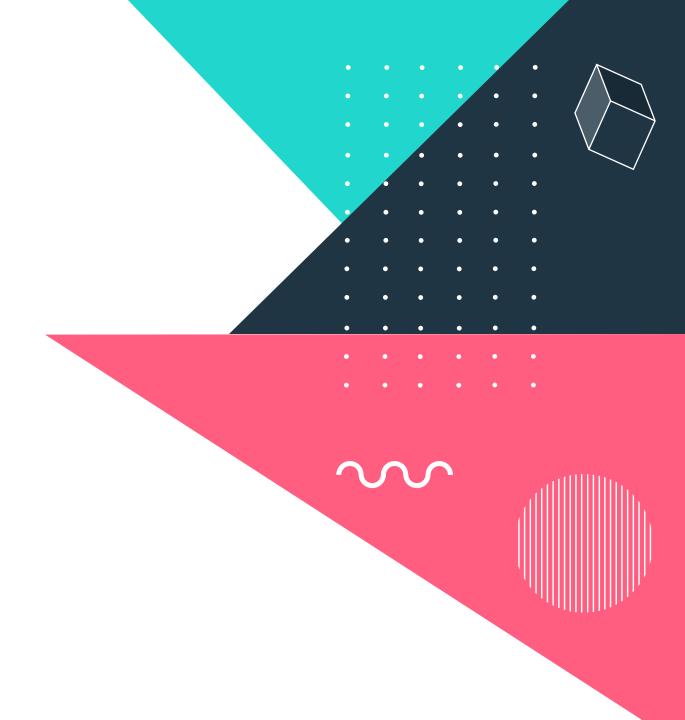
Wave Visualizer Tvisha Gangwani, Jino Haro, Ishraq Khandaker, Klarizsa Padilla, Zhongtai Ren



Motivation

CONSTANT interaction with oscilloscopes. How do they work? Build our own to find out!

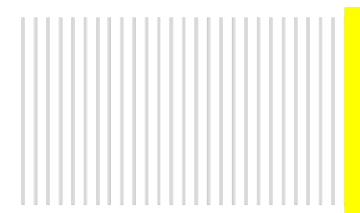


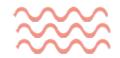


Overview

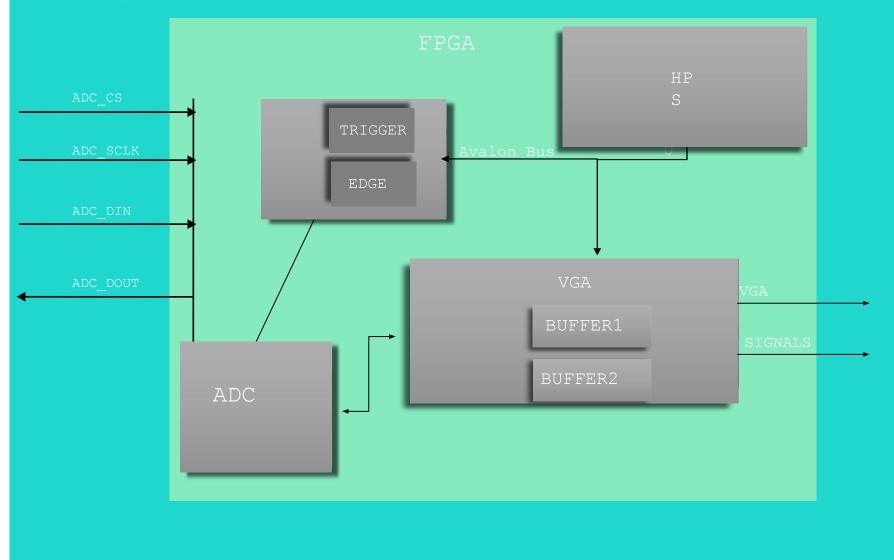
Utilize the FPGA's ADC to sample and display waveforms

Allow for user input to declare the trigger value and select a rising or falling edge for the trigger





ARCHITECTURE



HARDWARE

VGA: hardcoded values, software input, buffers to display waveform.

DISPLAYS: HEX display the voltage on the first 4 seven segments and trigger value on the last 2.

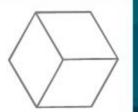
ADC: the backbone of our project! Configured ADC to sample data and send it to the VGA







References



New appreciation for oscilloscopes!

Learning how to program an ADC was extremely challenging but we learned a wealth of new skills including:

Research of product Tools to debug The importance of timing!

Invaluable support from the TAs and Professor Edwards

New to Verilog programing this semester, at the end of lab1 we would not have imagined we would come to enjoy the process of planning, designing and implementing a solution on an FPGA. Now, we don't want to give the FPGA back!

Grateful for the internet!

ADC Datasheet: LTC2308

https://www.analog.com/media/en/technic al-documentation/data-sheets/2308fc.pdf

Digital Scope Implemented on Altera DE1-SoC:

https://people.ece.cornell.edu/land/course s/eceprojectsland/STUDENTPROJ/2015t o2016/hj424/



SOFTWARE

Interface layout

Buttons and mouse usage

MEMORY ACCESS AND TIMING



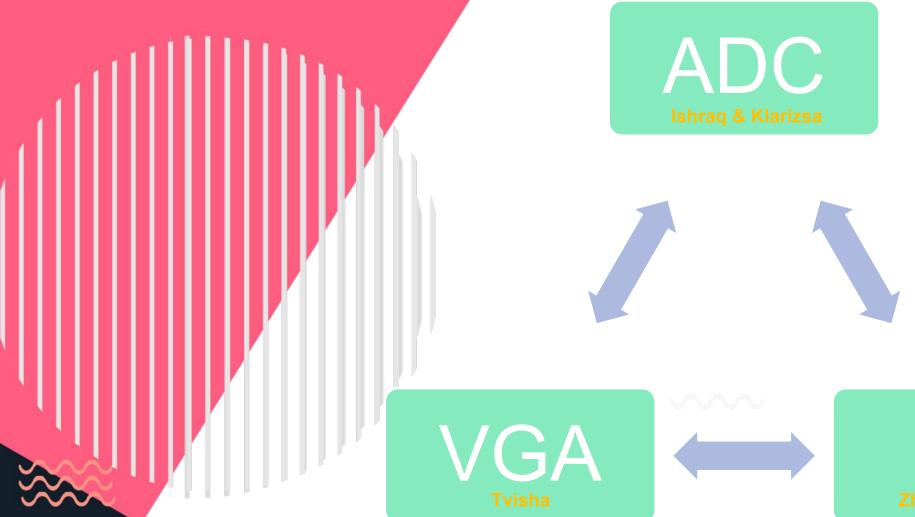
TIMING DIAGRAMS FOR ADC



TIMING DIAGRAMS FOR COMMUNICATION PROTOCOL



PROJECT PLAN







DEBUGGING

- Mouse
- Software Input
- Accessing Buffers Merging Code
- Communication
- **Hex Display**
- Test Bench
- "Magic" Timing Diagram Paper

Features

Manipulate trigger value

Rising or falling edge selection

Mouse selection



EXAMPLE OF SAMPLING

