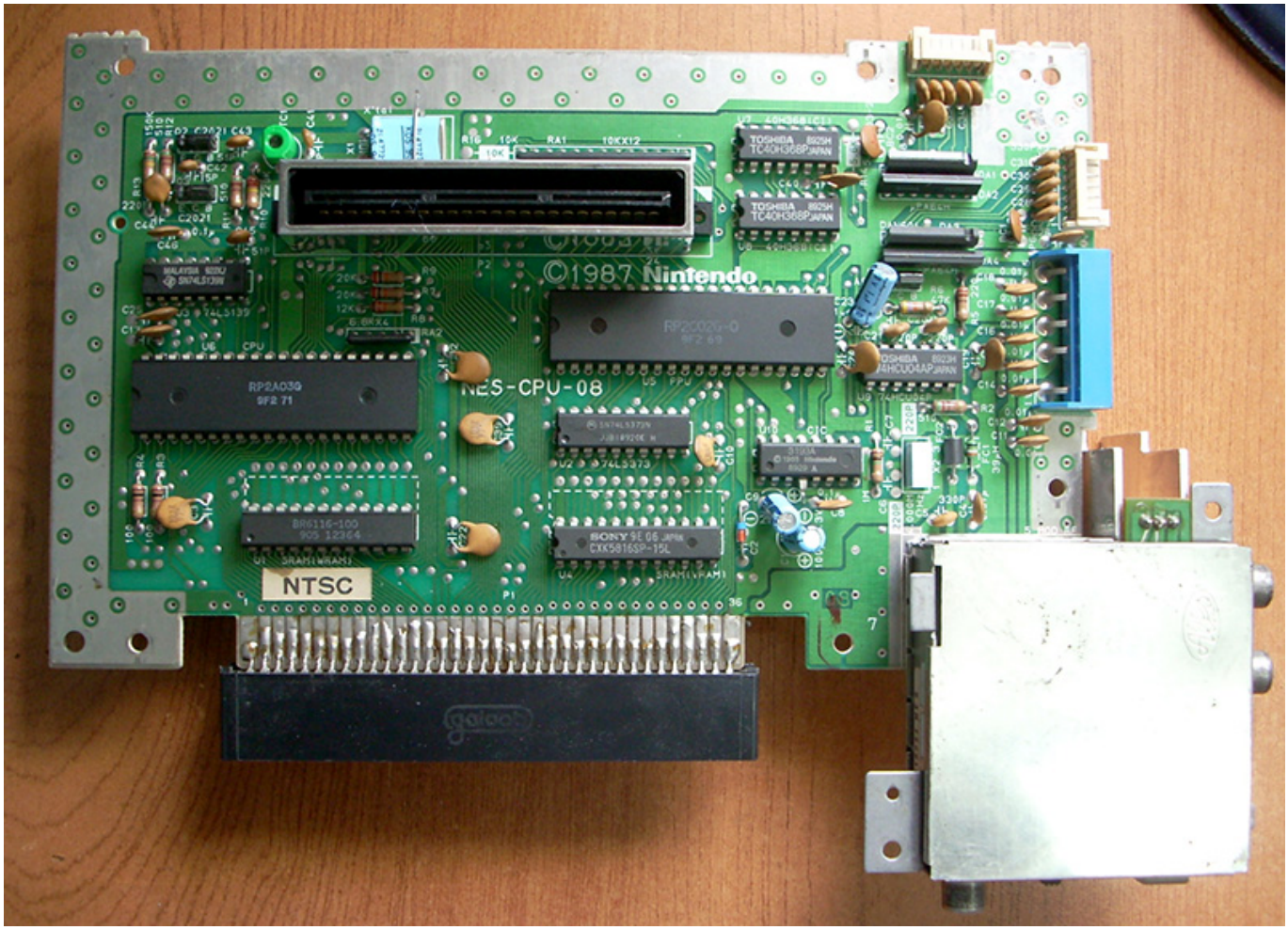
nes-pacs

This project aims to emulate the hardware of the Nintendo Entertainment System (NES) on an Altera Cyclone V FPGA.



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Background

The NES uses an 8-bit processor, with a 16-bit address space, based on the MOS Technology 6502.

Objectives

Write working implementations of the following NES components in SystemVerilog:

- Ricoh 2A03 processor (including audio processing unit)
- NES Picture Processing Unit (PPU)

Implement a regression test suite to ensure that the CPU and PPU excecute instructions accurately. This will begin by writing simulations in quartus and end with loading NES games onto the fpga.

Project Team

This project is conducted as part of Stephen Edwards' Embedded Systems (CSEE 4840) course at Columbia University.

- Philip Schiffrin (pjs2186)
- Akira Baruah (akb2158)
- Chaiwen Chou (cc3636)
- Sean Liu (sl3497)

References

Coming soon!