BlazePPS (Blaze Packet Processing System)
CSEE W4840 Project Proposal

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We are working with David Lariviere to extend a project that has been worked on by groups in previous semesters and is currently being worked on by Bhargav Sethuram (see 10Gb/s packet Processing on Hybrid SoC/FPGA Platform). We are attempting to meet with Bhargav so that we can come up-to-speed on the precise status of the project and determine how we can extend it. We are most likely interested in building a custom Ethernet driver that interfaces Linux with the on-chip FIFOs through the Avalon MM interface. We may extend or modify a communication protocol developed by the "10Gb/s Packet Processing" group that allows the software to communicate with the hardware (they did not implement it) or develop our own. We are also interested in implementing more advanced packet processing either in software or hardware. Additionally, we want to standardize the configuration and create tools that make it easy for students to set up the 10Gb/s packet processor, interface it with Linux, and pick up where we left off.