WMT –

"Whac-A-Mole" Like Game

CSEE 4840 Embedded System Design

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Acknowledgement

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We really appreciate the hard work of the TAs.

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1. Overview

Throughout this semester, we designed and implemented a “Whac-A-Mole” like game system using a TRDB-LTM touch panel. The user will interact directly with the panel while playing the game. Apart from the main game logic, we also introduced audio output along with the game to make it more fancy and commercial oriented.

Figure 1 LTM Panel

The game consists of four different scenarios. First one is a welcome page that enables the user to choose from one of the three difficulty levels and press “enter” to go to the main game page. The second page is where all the funny part happens. There are nine holes from which the moles might come out randomly at a certain rate. Not only the moles, we have also introduced baby bottles for supplement and evils that trying to destroy you. The game will run for two minutes for a round, then the last two background will show up to notify you result depending on your performance previously. After 5 seconds, the user will see the welcome page again and the system is ready for the next round.

2. Project Design

Overall system architecture is shown as follows:

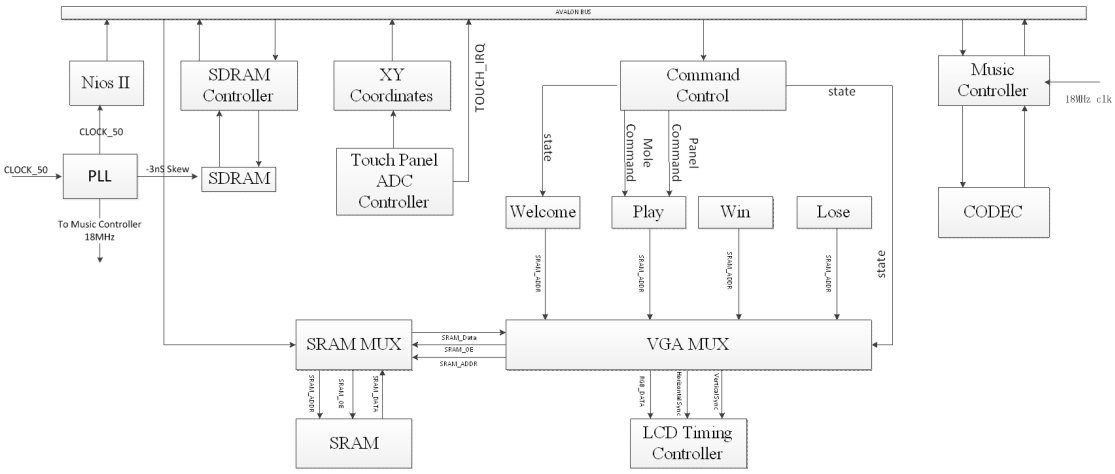


Figure 2 System Architecture

3. System Implementation

3.1 Hardware

1. Overview of the system

   The system contains three basic functions that are NIOS II CPU, ADC controller that detects the touch position and generates interrupt and an 800 x 480 resolution display. The CPU core operates at 50 MHz and the display operates at 25MHz. The CPU used SDRAM as memory and SRAM as storage. In order to use the SDRAM as memory, a PLL is needed to generate the -3nS skew clock for the CPU. Another 18MHz is also generated from the PLL.

2. Modules Used in the Hardware System

Module	Function
Adc_spi_controller.v	Control the ADC output mode
Audio_controller.v	Control the audio output
Command.v	Used to receive and distribute

	command to sub-sequent modules
Control_panel.v	Controls all the output on the control panel
DE2_TOP_PROJECT.v	Design TOP-Level
interrupt.v	Generate interrupt for touching
irq_gen.v	Generate interrupt for touching
lcd_controller.v	Lcd timing controller
lcd_spi_controller.v	Used to set the display mode of the display
lcd_timing_controller.v	Control the output HS, VS and RGB to the LCD display
letter.v	Used to display the letter
life.v	Used to display the life
lose.v	Used to display the lose message
mole_controller.v	Used to control the action of mole
musiscontroller.vhd	Used to control the music
No_GEN.v	Used to display the touch position x and y coordinate on DE2 LEDs
number.v	Used to display numbers

panel_control.v	Used to display all panel information
pause.v	Implement the pause button
play.v	Implement the Play state interface
quit.v	Implement the quit button
score.v	Used to display the score
reset_delay.v	Set the reset delay for different modules
SEG7_LUT_8.v	Display the numbers on 8 LEDs
SEG_LUT.v	Display the numbers on LED
sram_mux.v	Used to select which vga signal to output
sram.v	Sram controller
start.v	Start button
symbol.v	Used to display symbol
three_wire_controller.v	Used to set up the LCD display mode
Timmer.v	Timer on the display
welcome.v	Welcome state vga
win.v	Win state vga

xycoord_interface.v	Transmit x and y coordinates through Avalon bus.

3. Memory requirement

Content	Size	Location stored
Background(Mole Position)	64000	SRAM
Background(Control Panel)	28800	SRAM
Mole	28800	SRAM
Milk Bottle	28800	SRAM
Bomb	28800	SRAM
Indicator(Level selection)	7200	SRAM
Red Heart	7200	SRAM
Gold coin	7200	SRAM
Clock	7200	SRAM
Letters(26 letters)	2048 x 26	SRAM

4. Sprites

Sprites Catalog	Number of Sprites

Mole	2
Milk Bottle	1
Bomb	1
Gold Coin	1
Red Heart	1
Clock	1
Letters	26
Background	2

All the sprites were pre-processed using MATLAB. In our case, the SRAM only output 16 bits number at a time. So all the image sprites used in the game was transformed from 24 bit true color to 16 bit high-color. The MATLAB code can be found in the project package. To get rid of the white back ground, a matrix of 1s and 0s were generated to represent if it's a white spot. If it's a white spot, it will be replaced by the background color.

5. Peripherals

    1. LCD timing controller

        LCD timing controller is used to generate Hcount and Vcount， which generates Hsync and Vsync. The RGB data from VGA MUX is passed to the display through LCD timing controller.

    2. Touch Panel ADC Controller

        Touch panel takes the pressure when user presses the screen and generate

two 12 bit digital numbers which represent the x and y coordinates. It also generates an IRQ which will be used in the software to detect state transition or user actions.

3. XY Coordinates

   XY Coordinates is used to take the data from touch panel ADC controller and pass the data on to the Avalon bus. Software will take the data and do the next step procession.

4. Command Control

   Command control takes the data from the CPU and writes them into the assigned registers. There two type of commands. One is Mole_ctrl, which is used to control the mole activity. In other words, it controls whether there is a mole, milk bottle or bomb and if it's hit or not. The other command, which we call Panel_ctrl, it contains all the information that we need on the control panel, like score, life and current state. By decoding these two commands, the system will be able to switch between different state and conduct the game logic.

5. Welcome, Play, Win, Lose

   This four peripheral contains all the basic information the game need in four different states. Like in the Welcome, we have the initial interface for users to choose the game difficulty they want. In the Play state, users can play the game, pause the game and quit the game. If the user wins the game, Win state will pop up. Otherwise, lose state will show up.

6. SRAM MUX

   At the beginning of the game, we have to write all the data we need into the SRAM. Data are basically background images, sprites, and some colors we need. This was done by using the SDRAM as memory and writing all the data into the SRAM through Avalon bus at the beginning of the game. Once all the

data has been written to SRAM, the SRAM is automatically disconnect from the Avalon bus and connected to VGA MUX.

7. VGA MUX

   VGA MUX is used to choose which states to load. It's controlled only by current state. It takes the address from the proper state and uses it to read the colors from SRAM.

6. Lesson learned

- ELF error is usually due to wiring mistake in the top level connection of NIOS.
- Every time you copy an entire project, remember to recreate the nios project. Otherwise the BSP package is mapped to the old SOPC.
- Should have design the interface more easy to use. Should split all the variables instead of putting all of them together
- Build the design using small modules.

3.2 Display Dynamic Items

For the implementation of Verilog programs to control all the dynamical elements appearing and disappearing as well as the nine holes on the touch panel, we got the signal from the software, which indicate which element needs to appear or disappear. Then we used the first 27 bits of the 32-bit input for the identifier and the state of each element in the nine holes, three for each. For each three-bit, two of them represent that element is; 00 for the mole, 01 for the evil, 10 for the baby bottle. The third one is the state of the element; 1 represents going up while 0 represents going down. For all the period while a certain element need to be presented on the screen, we would get a 1 on the third bit of that hole. Once the element is hit or timed out, we would receive a 0 immediately.

The logic is as follows.

We defined three layers for each cell on the screen (a cell consists of the background, the hole and the space for the element to be placed). The lowest layer is the grass

background and the upper half of the black hole. The middle layer is the element, while the highest layer is the lower half of the black hole.

Instead of just appearing on the screen suddenly, we would make it go up one pixel by one pixel to mock the real situation when we get the signal that an element need to appear. By increasing the height of the element starting at 0 till 120 pixels could achieve this.

When a 0 on the third bit is detected, the height of the item will be set to 0, which means it will disappear on the screen.

We have downloaded the pictures of the three items from the Internet as shown below.

Figure 3 Items for the game

We used Matlab to get the matrix representations of the pictures in the first place. In order to display the item without the white edge, we wrote a Python script to calculate the edges of the item for each picture and then feed the edge information into the Verilog. When an item needs to be printed on the screen, the program will check whether the pixel being printed is inside the edge of the item, if so, the overwrite signal will be sent, otherwise, the hardware will just print the background grass or hole accordingly.

3.3 Software

In the software part, the main task is to corporate with the hardware and music to make our touching screen work.

The procedure is described as followed:

(a) User chooses the game mode among Easy, Normal and Hard on the Welcome page.

(b) After pressing "Start", the game starts. The item to be shown among mole, bottle and bomb and the position of the item is randomized. Every mole appears for one second.

(c) When a state change is detected, it goes to Pause, Quit or Item status.

(d) In the Pause status, the timer is stopped and the item is held at the original position.

(e) In the Quit status, it jumps to the Welcome page.

(f) In the Item page, there are three situations:

- Item is mole: The total score adds five points if the mole is hit, otherwise one life is deducted from the lives.

- Item is bottle: The lives add one if it is smaller than three.

- Item is bomb: One life is deducted from lives. If the lives are equal to zero, it goes to the Lose page and goes to the Welcome page after remaining for 5 seconds.

(g) Win page appears if the game last more than one minutes.

Here is the block diagram of the game mechanism:

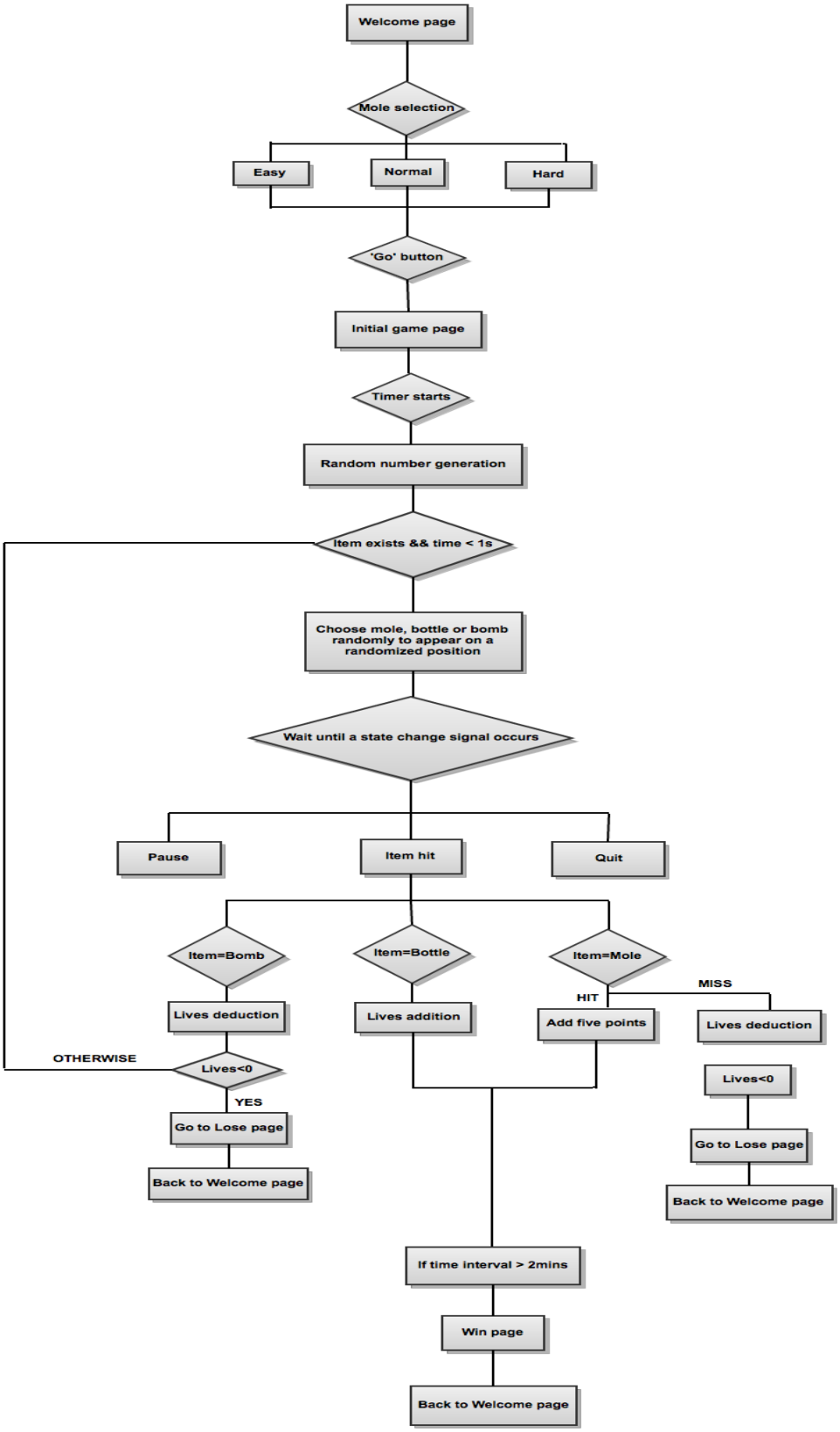


Figure 4 Software block diagram

3.4 Audio

In this game we have two kinds of audio: the game music and the game sound effects. All the sound tracks are downloaded from internet converted by matlab, and stored in the SDRAM as .h files (we used SDRAM as the CPU memory because it has enough space for the music), so that we can directly access them in the software level instead of read from other memory.

Audio Architecture:

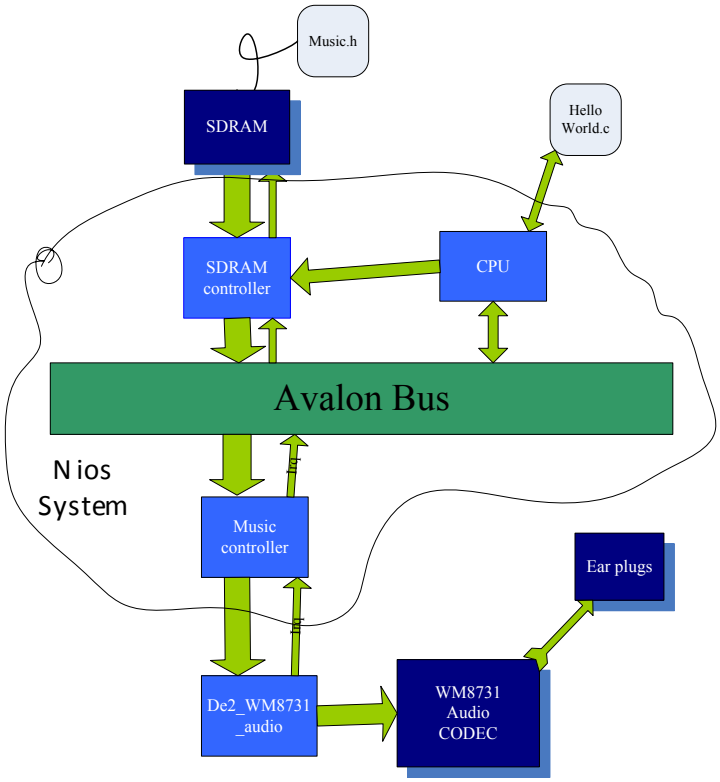


Figure 5 Audio Architecture

As shown in the picture, CPU controls SDRAM to transfer audio data to audio part through nios-system (sopc). Parts are described below:

— WM8731 CODEC is the audio function chip on the DE2 Board.

- de2_WM8731 is the vhdl code that controls the chip by providing it clocks and shifting audio data into it.
- Music controller is the interface VHDL that maps the audio part into the Nios-system.
- SDRAM controller is the interface VHDL that maps the SDRAM into the Nios-system.
- SDRAM and CPU are self-explained components which if you don't understand you'd better drop the class and choose Agriculture as your major.
- Main.c is your weapon to command audio part when to play what; Music.h is where your melody waiting to be played.

Key issues

How to make it sound.

Our digital sound data are actually arrays of 16-bit sample values, if we align the sample value in sequence, they will appear as sound wave. WM8731 audio chip makes sounds by align sample values in sequence and convert them into analog signals.

To make the WM8731 work, understanding its controller de2_WM8731_audio is critical. de2_WM8731_audio.vhd has two main jobs: provide clocks, and shift audio data bits into the WM8731 audio chip. Data bits are shifted one bit at a time into the Audio chip(left and right channel), change between channels every 16 bits(same 16 bits), after the 16 bits are shifted into both L/R channel, it reads another 16-bit sample and keep on shift in. There're two important clocks needed to ensure the bits are shifted properly---LRCK and BCK. BCK is Bit-stream clock, it controls the pace that data bits are shifted into the WM8731 chip, one bit per BCK clock cycle. LRCK controls the alternation between L/R channel, when LRCK = 1, bits are shifted into the L channel, and shift in to R channel when LRCK = 0. Both LRCK and BCK are generated from the proper working clock of de2_WM8731_audio.vhd---18.432M Hz.

To generate the bck and lrck, there are many other signals used, such as LRCK_divider, BCK_divider, set_lrck, etc. Words are not enough to express what I want to tell, see the timing diagram:

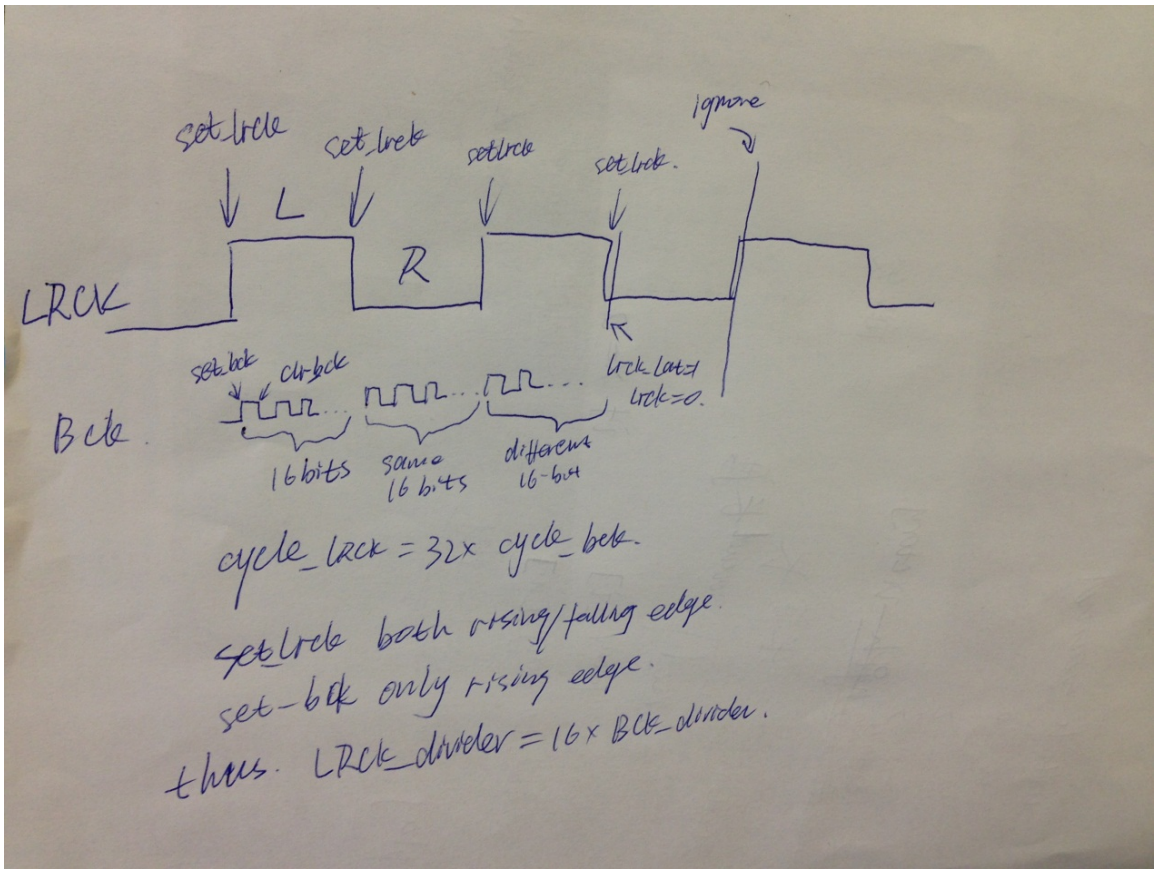


Figure 6 Timing diagram

In the diagram, you can see the relation between LRCK_divider and BCK_divider.

Another important thing is the choice of sample rate. With higher sample rate, you can get more accurate sounds, and of course, higher working clock frequency, which means smaller divider. The calculation is as follows:

LRCK_divider = 18.432M Hz/(sample rates*2)

And knowing the relation between LRCK and BCK, you can easily calculate BCK_divider and everything.

We firstly used 6000Hz sample rates, the music we get made us don't want to play the game. Thus we used 22050Hz sample rates, the game reminded us of our childhood.

Another thing to mention, there's no 18.432 M Hz clock available on chip, only 50M Hz and 27M Hz, thus, we used a .pll (phase lock loop) to generate the 18.432M hz from 50M Hz on chip.

How to send data in.

The audio play hardware is readily configured, but how to send the data in?

In order to save the on chip memory, and prevent any discrepancy in data transfer between two different clock domains, we used a 256-2bytes buffer to buffer the music writing. The picture will explain itself.

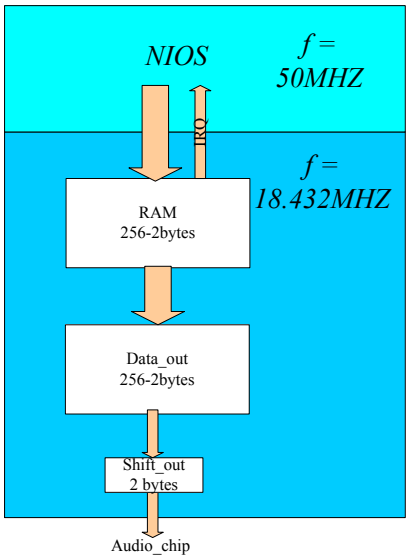


Figure 7 Data transfer block diagram

When Data_out had fully read RAM's data (address count to 256), irq =1, nios detects it and sends a new array of 256-2bytes data in.

Software control.

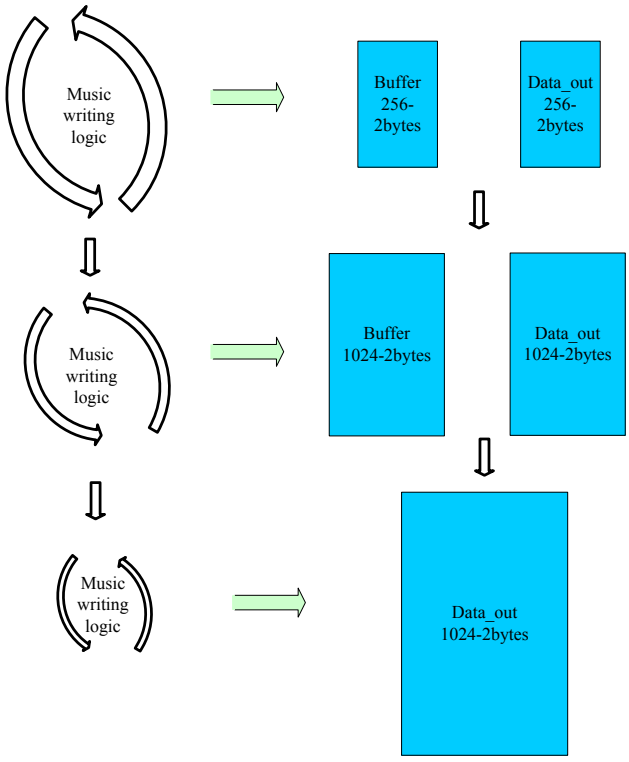
In the design, besides from the game music, we have sound effects during the game play—hit, miss, explo, life---and the stand by period---press button. We merge the music and sound effects with the function as follows:

When no sound effects are triggered, audio_to_play = music_to_play, only the music will be played. When sound effect triggered Audio_to_play = music_to_play/4

+ sound_to_play*3/4. Music's volume is decreased to 1/4 when merge with sound , because our sounds' volume itself is small, we gave it larger portion of volume. You cannot simply add the sound and music together, because the 16bits samples will overflow, the value of audio_to_play should be kept at a total scale of 1 to prevent this.

Structure Optimization.

One important issue of using SDRAM as CPU's memory is that its speed is a bit slow. Thus, when we firstly link the audio software and hardware together, the music we hear is half or even the 1/4 of the normal speed. There are two reasons that may cause this: firstly, the CPU cannot respond the audio hardware's interrupts frequently, thus the data stored in the audio buffer is not timely refreshed and is been played several times before it is refreshed; secondly, the music writing logic loop is too big, it need to be small because this part of code is executed most frequently by CPU, and will slow down the whole game if not succinct enough. The solution is, increase the buffer size in hardware so that it does not call for interruption too frequently, and optimize the music writing loop logic:

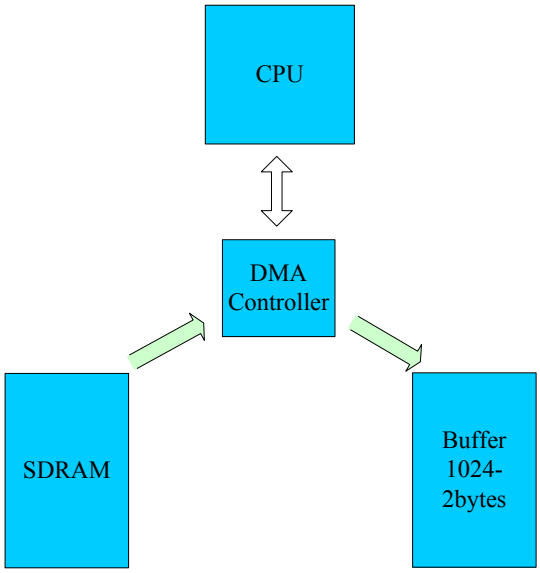


During this process, we found that the extra music buffer is not really necessary because the CPU f=50MHz is much higher than Audio chip f=18.432MHz, discrepancies in the domain boundary can be omitted, so we got rid of it to save on-chip memory and compile time.

In this way, we successfully get the right music and sound.

DMA

Another way to deal with the CPU and audio speed thing is to use a DMA (direct-memory-access) controller. It can serve itself transferring data from SDRAM to audio hardware. With DMA, CPU only need to tell it the starting address for the transfer and how many bytes (2 bytes) to transfer at the beginning of the transfer, instead of transfer every bytes (2 bytes) by itself during the whole process of transfer.



We tried this and it worked. However, we didn't include this in our final design, because we can also solve the problem by optimizing the structure, and we think that the structure optimization should always be the first choice before we resort to any other extra resources.

Audio Experience.

We tried many methods in implementing the audio during our design. At first, we

tried to synthesis the music directly in the VHDL code, similar to lab 3, and we found that the music is too simple, not exciting at all, and the sound effects are hard to generate, thus we decide to download the music; we put music in the SDRAM and sound in the VHDL, trying to merge them together in the hardware, it turns out to be a little bit complicated doing it in hardware, and due to the large size of soundtracks in ROM(high sample rates), the compile time became ridiculous. At last, we decide to put all audio tracks in the SDRAM, emerge them in the software before sending to the hardware; it turns out to be lot easier than doing it in hardware. After that, we tried to implement a Direct Memory Access controller in SOPC to control the music data transfer, so that sending audio data will not occupy CPU much and game performance can be improved. However, as reason indicated above, we didn't include it in our final design.

4. Responsibilities and Future Work

Jian was in charge of the overall hardware design and implementation; Si's main responsibility was to implement the dynamic display on the screen; Shuting managed the software and Lingchuan achieved the working audios. Throughout the project, all the team members worked together for the debugging and testing.

For the future work, we want to:

1. Make it possible for more than one items coming out the holes simultaneously.
2. Apart from the specific sounds played when you successfully whac or miss an item, implement visual efforts for all the events on the screen.

5. Code

N.B. Since the header file for the music is too large, we didn't attach it here. But it will come with the project file.

nios_system.v

```
//megafunction wizard: %Altera SOPC Builder%
//GENERATION: STANDARD
```

```
//VERSION: WM1.0


//Legal Notice: (C)2013 Altera Corporation. All rights reserved.  Your
//use of Altera Corporation's design tools, logic functions and other
//software and tools, and its AMPP partner logic functions, and any
//output files any of the foregoing (including device programming or
//simulation files), and any associated documentation or information are
//expressly subject to the terms and conditions of the Altera Program
//License Subscription Agreement or other applicable license agreement,
//including, without limitation, that your use is for the sole purpose
//of programming logic devices manufactured by Altera and sold by Altera
//or its authorized distributors.  Please refer to the applicable
//agreement for further details.

// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module audio_controller_0_avalon_slave_0_arbitrator (
                                                      // inputs:

audio_controller_0_avalon_slave_0_readdata,
                                                       clk,

cpu_0_data_master_address_to_slave,

cpu_0_data_master_byteenable,

cpu_0_data_master_dbs_address,

cpu_0_data_master_dbs_write_16,

cpu_0_data_master_no_byte_enables_and_last_term,
                                                       cpu_0_data_master_read,

cpu_0_data_master_waitrequest,
                                                       cpu_0_data_master_write,

cpu_0_instruction_master_address_to_slave,

cpu_0_instruction_master_dbs_address,

cpu_0_instruction_master_read,
                                                       reset_n,

                                                      // outputs:

audio_controller_0_avalon_slave_0_address,

audio_controller_0_avalon_slave_0_chipselect,

audio_controller_0_avalon_slave_0_read,
```

```
audio_controller_0_avalon_slave_0_readdata_from_sa,

audio_controller_0_avalon_slave_0_reset_n,

audio_controller_0_avalon_slave_0_write,

audio_controller_0_avalon_slave_0_writedata,

cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0,

cpu_0_data_master_granted_audio_controller_0_avalon_slave_0,

cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0,

cpu_0_data_master_read_data_valid_audio_controller_0_avalon_slave_0,

cpu_0_data_master_requests_audio_controller_0_avalon_slave_0,

cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0,

cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0,

cpu_0_instruction_master_read_data_valid_audio_controller_0_avalon_slave_0,

cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0,

d1_audio_controller_0_avalon_slave_0_end_xfer
                                                                    )
;

  output  [  4: 0] audio_controller_0_avalon_slave_0_address;
  output           audio_controller_0_avalon_slave_0_chipselect;
  output           audio_controller_0_avalon_slave_0_read;
  output  [ 15: 0] audio_controller_0_avalon_slave_0_readdata_from_sa;
  output           audio_controller_0_avalon_slave_0_reset_n;
  output           audio_controller_0_avalon_slave_0_write;
  output  [ 15: 0] audio_controller_0_avalon_slave_0_writedata;
  output  [  1: 0] cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0;
  output           cpu_0_data_master_granted_audio_controller_0_avalon_slave_0;
  output
cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0;
  output
cpu_0_data_master_read_data_valid_audio_controller_0_avalon_slave_0;
  output           cpu_0_data_master_requests_audio_controller_0_avalon_slave_0;
  output           cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0;
  output
cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0;
  output
cpu_0_instruction_master_read_data_valid_audio_controller_0_avalon_slave_0;
  output           cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0;
  output           d1_audio_controller_0_avalon_slave_0_end_xfer;
  input   [ 15: 0] audio_controller_0_avalon_slave_0_readdata;
  input            clk;
  input   [ 24: 0] cpu_0_data_master_address_to_slave;
  input   [  3: 0] cpu_0_data_master_byteenable;
  input   [  1: 0] cpu_0_data_master_dbs_address;
  input   [ 15: 0] cpu_0_data_master_dbs_write_16;
  input            cpu_0_data_master_no_byte_enables_and_last_term;
```

```
  input              cpu_0_data_master_read;
  input              cpu_0_data_master_waitrequest;
  input              cpu_0_data_master_write;
  input     [ 24: 0] cpu_0_instruction_master_address_to_slave;
  input     [  1: 0] cpu_0_instruction_master_dbs_address;
  input              cpu_0_instruction_master_read;
  input              reset_n;

  wire      [  4: 0] audio_controller_0_avalon_slave_0_address;
  wire               audio_controller_0_avalon_slave_0_allgrants;
  wire               audio_controller_0_avalon_slave_0_allow_new_arb_cycle;
  wire               audio_controller_0_avalon_slave_0_any_bursting_master_saved_grant;
  wire               audio_controller_0_avalon_slave_0_any_continuerequest;
  reg       [  1: 0] audio_controller_0_avalon_slave_0_arb_addend;
  wire               audio_controller_0_avalon_slave_0_arb_counter_enable;
  reg       [  1: 0] audio_controller_0_avalon_slave_0_arb_share_counter;
  wire      [  1: 0] audio_controller_0_avalon_slave_0_arb_share_counter_next_value;
  wire      [  1: 0] audio_controller_0_avalon_slave_0_arb_share_set_values;
  wire      [  1: 0] audio_controller_0_avalon_slave_0_arb_winner;
  wire               audio_controller_0_avalon_slave_0_arbitration_holdoff_internal;
  wire               audio_controller_0_avalon_slave_0_beginbursttransfer_internal;
  wire               audio_controller_0_avalon_slave_0_begins_xfer;
  wire               audio_controller_0_avalon_slave_0_chipselect;
  wire      [  3: 0] audio_controller_0_avalon_slave_0_chosen_master_double_vector;
  wire      [  1: 0] audio_controller_0_avalon_slave_0_chosen_master_rot_left;
  wire               audio_controller_0_avalon_slave_0_end_xfer;
  wire               audio_controller_0_avalon_slave_0_firsttransfer;
  wire      [  1: 0] audio_controller_0_avalon_slave_0_grant_vector;
  wire               audio_controller_0_avalon_slave_0_in_a_read_cycle;
  wire               audio_controller_0_avalon_slave_0_in_a_write_cycle;
  wire      [  1: 0] audio_controller_0_avalon_slave_0_master_qreq_vector;
  wire               audio_controller_0_avalon_slave_0_non_bursting_master_requests;
  wire               audio_controller_0_avalon_slave_0_read;
  wire      [ 15: 0] audio_controller_0_avalon_slave_0_readdata_from_sa;
  reg                audio_controller_0_avalon_slave_0_reg_firsttransfer;
  wire               audio_controller_0_avalon_slave_0_reset_n;
  reg       [  1: 0] audio_controller_0_avalon_slave_0_saved_chosen_master_vector;
  reg                audio_controller_0_avalon_slave_0_slavearbiterlockenable;
  wire               audio_controller_0_avalon_slave_0_slavearbiterlockenable2;
  wire               audio_controller_0_avalon_slave_0_unreg_firsttransfer;
  wire               audio_controller_0_avalon_slave_0_waits_for_read;
  wire               audio_controller_0_avalon_slave_0_waits_for_write;
  wire               audio_controller_0_avalon_slave_0_write;
  wire      [ 15: 0] audio_controller_0_avalon_slave_0_writedata;
  wire               cpu_0_data_master_arbiterlock;
  wire               cpu_0_data_master_arbiterlock2;
  wire      [  1: 0] cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0;
  wire                                                [  1:  0]
cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0_segment_0;
  wire                                                [  1:  0]
cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0_segment_1;
  wire               cpu_0_data_master_continuerequest;
  wire               cpu_0_data_master_granted_audio_controller_0_avalon_slave_0;
  wire
cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0;
  wire
cpu_0_data_master_read_data_valid_audio_controller_0_avalon_slave_0;
  wire               cpu_0_data_master_requests_audio_controller_0_avalon_slave_0;
```

```
  wire        cpu_0_data_master_saved_grant_audio_controller_0_avalon_slave_0;
  wire        cpu_0_instruction_master_arbiterlock;
  wire        cpu_0_instruction_master_arbiterlock2;
  wire        cpu_0_instruction_master_continuerequest;
  wire        cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0;
  wire
cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0;
  wire
cpu_0_instruction_master_read_data_valid_audio_controller_0_avalon_slave_0;
  wire        cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0;
  wire
cpu_0_instruction_master_saved_grant_audio_controller_0_avalon_slave_0;
  reg         d1_audio_controller_0_avalon_slave_0_end_xfer;
  reg         d1_reasons_to_wait;
  reg         enable_nonzero_assertions;
  wire        end_xfer_arb_share_counter_term_audio_controller_0_avalon_slave_0;
  wire        in_a_read_cycle;
  wire        in_a_write_cycle;
  reg
last_cycle_cpu_0_data_master_granted_slave_audio_controller_0_avalon_slave_0;
  reg
last_cycle_cpu_0_instruction_master_granted_slave_audio_controller_0_avalon_slave_0;
  wire                                                [ 24: 0]
shifted_address_to_audio_controller_0_avalon_slave_0_from_cpu_0_data_master;
  wire                                                [ 24: 0]
shifted_address_to_audio_controller_0_avalon_slave_0_from_cpu_0_instruction_master;
  wire        wait_for_audio_controller_0_avalon_slave_0_counter;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_reasons_to_wait <= 0;
      else
        d1_reasons_to_wait <= ~audio_controller_0_avalon_slave_0_end_xfer;
    end


  assign audio_controller_0_avalon_slave_0_begins_xfer = ~d1_reasons_to_wait &
((cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0 |
cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0));
  //assign audio_controller_0_avalon_slave_0_readdata_from_sa =
audio_controller_0_avalon_slave_0_readdata so that symbol knows where to group signals
which may go to master only, which is an e_assign
  assign audio_controller_0_avalon_slave_0_readdata_from_sa =
audio_controller_0_avalon_slave_0_readdata;

  assign cpu_0_data_master_requests_audio_controller_0_avalon_slave_0 =
({cpu_0_data_master_address_to_slave[24 : 6] , 6'b0} == 25'h1001100) &
(cpu_0_data_master_read | cpu_0_data_master_write);
  //audio_controller_0_avalon_slave_0_arb_share_counter set values, which is an e_mux
  assign audio_controller_0_avalon_slave_0_arb_share_set_values =
(cpu_0_data_master_granted_audio_controller_0_avalon_slave_0)? 2 :
    (cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0)? 2 :
    (cpu_0_data_master_granted_audio_controller_0_avalon_slave_0)? 2 :
    (cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0)? 2 :
    1;

  //audio_controller_0_avalon_slave_0_non_bursting_master_requests mux, which is an e_mux
  assign audio_controller_0_avalon_slave_0_non_bursting_master_requests =
```

```
cpu_0_data_master_requests_audio_controller_0_avalon_slave_0 |
      cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0 |
      cpu_0_data_master_requests_audio_controller_0_avalon_slave_0 |
      cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0;

  //audio_controller_0_avalon_slave_0_any_bursting_master_saved_grant mux, which is an
e_mux
  assign audio_controller_0_avalon_slave_0_any_bursting_master_saved_grant = 0;

  //audio_controller_0_avalon_slave_0_arb_share_counter_next_value assignment, which is an
e_assign
  assign audio_controller_0_avalon_slave_0_arb_share_counter_next_value =
audio_controller_0_avalon_slave_0_firsttransfer ?
(audio_controller_0_avalon_slave_0_arb_share_set_values - 1) :
|audio_controller_0_avalon_slave_0_arb_share_counter ?
(audio_controller_0_avalon_slave_0_arb_share_counter - 1) : 0;

  //audio_controller_0_avalon_slave_0_allgrants all slave grants, which is an e_mux
  assign audio_controller_0_avalon_slave_0_allgrants =
(|audio_controller_0_avalon_slave_0_grant_vector) |
      (|audio_controller_0_avalon_slave_0_grant_vector) |
      (|audio_controller_0_avalon_slave_0_grant_vector) |
      (|audio_controller_0_avalon_slave_0_grant_vector);

  //audio_controller_0_avalon_slave_0_end_xfer assignment, which is an e_assign
  assign audio_controller_0_avalon_slave_0_end_xfer =
~(audio_controller_0_avalon_slave_0_waits_for_read |
audio_controller_0_avalon_slave_0_waits_for_write);

  //end_xfer_arb_share_counter_term_audio_controller_0_avalon_slave_0 arb share counter
enable term, which is an e_assign
  assign end_xfer_arb_share_counter_term_audio_controller_0_avalon_slave_0 =
audio_controller_0_avalon_slave_0_end_xfer &
(~audio_controller_0_avalon_slave_0_any_bursting_master_saved_grant | in_a_read_cycle |
in_a_write_cycle);

  //audio_controller_0_avalon_slave_0_arb_share_counter arbitration counter enable, which is
an e_assign
  assign audio_controller_0_avalon_slave_0_arb_counter_enable =
(end_xfer_arb_share_counter_term_audio_controller_0_avalon_slave_0 &
audio_controller_0_avalon_slave_0_allgrants) |
(end_xfer_arb_share_counter_term_audio_controller_0_avalon_slave_0 &
~audio_controller_0_avalon_slave_0_non_bursting_master_requests);

  //audio_controller_0_avalon_slave_0_arb_share_counter counter, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          audio_controller_0_avalon_slave_0_arb_share_counter <= 0;
      else if (audio_controller_0_avalon_slave_0_arb_counter_enable)
          audio_controller_0_avalon_slave_0_arb_share_counter <=
audio_controller_0_avalon_slave_0_arb_share_counter_next_value;
    end


  //audio_controller_0_avalon_slave_0_slavearbiterlockenable slave enables arbiterlock, which
is an e_register
  always @(posedge clk or negedge reset_n)
```

```
      begin
         if (reset_n == 0)
               audio_controller_0_avalon_slave_0_slavearbiterlockenable <= 0;
         else          if          ((|audio_controller_0_avalon_slave_0_master_qreq_vector          &
end_xfer_arb_share_counter_term_audio_controller_0_avalon_slave_0)                                  |
(end_xfer_arb_share_counter_term_audio_controller_0_avalon_slave_0                                  &
~audio_controller_0_avalon_slave_0_non_bursting_master_requests))
               audio_controller_0_avalon_slave_0_slavearbiterlockenable                            <=
|audio_controller_0_avalon_slave_0_arb_share_counter_next_value;
      end


   //cpu_0/data_master audio_controller_0/avalon_slave_0 arbiterlock, which is an e_assign
   assign                                cpu_0_data_master_arbiterlock                               =
audio_controller_0_avalon_slave_0_slavearbiterlockenable                                            &
cpu_0_data_master_continuerequest;

   //audio_controller_0_avalon_slave_0_slavearbiterlockenable2 slave enables arbiterlock2,
which is an e_assign
   assign                audio_controller_0_avalon_slave_0_slavearbiterlockenable2                   =
|audio_controller_0_avalon_slave_0_arb_share_counter_next_value;

   //cpu_0/data_master audio_controller_0/avalon_slave_0 arbiterlock2, which is an e_assign
   assign                               cpu_0_data_master_arbiterlock2                               =
audio_controller_0_avalon_slave_0_slavearbiterlockenable2                                           &
cpu_0_data_master_continuerequest;

   //cpu_0/instruction_master audio_controller_0/avalon_slave_0 arbiterlock, which is an
e_assign
   assign                              cpu_0_instruction_master_arbiterlock                           =
audio_controller_0_avalon_slave_0_slavearbiterlockenable                                            &
cpu_0_instruction_master_continuerequest;

   //cpu_0/instruction_master audio_controller_0/avalon_slave_0 arbiterlock2, which is an
e_assign
   assign                             cpu_0_instruction_master_arbiterlock2                           =
audio_controller_0_avalon_slave_0_slavearbiterlockenable2                                           &
cpu_0_instruction_master_continuerequest;

   //cpu_0/instruction_master granted audio_controller_0/avalon_slave_0 last time, which is an
e_register
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)

last_cycle_cpu_0_instruction_master_granted_slave_audio_controller_0_avalon_slave_0 <= 0;
         else

last_cycle_cpu_0_instruction_master_granted_slave_audio_controller_0_avalon_slave_0       <=
cpu_0_instruction_master_saved_grant_audio_controller_0_avalon_slave_0        ?        1        :
(audio_controller_0_avalon_slave_0_arbitration_holdoff_internal                                     |
~cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0)         ?         0         :
last_cycle_cpu_0_instruction_master_granted_slave_audio_controller_0_avalon_slave_0;
      end


   //cpu_0_instruction_master_continuerequest continued request, which is an e_mux
   assign                             cpu_0_instruction_master_continuerequest                        =
```

```
last_cycle_cpu_0_instruction_master_granted_slave_audio_controller_0_avalon_slave_0 & cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0;

  //audio_controller_0_avalon_slave_0_any_continuerequest at least one master continues requesting, which is an e_mux
  assign audio_controller_0_avalon_slave_0_any_continuerequest = cpu_0_instruction_master_continuerequest |
    cpu_0_data_master_continuerequest;

  assign cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0 = cpu_0_data_master_requests_audio_controller_0_avalon_slave_0 & ~(((~cpu_0_data_master_waitrequest | cpu_0_data_master_no_byte_enables_and_last_term | !cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0) & cpu_0_data_master_write) | cpu_0_instruction_master_arbiterlock);
  //audio_controller_0_avalon_slave_0_writedata mux, which is an e_mux
  assign audio_controller_0_avalon_slave_0_writedata = cpu_0_data_master_dbs_write_16;

  assign cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0 = (({cpu_0_instruction_master_address_to_slave[24 : 6] , 6'b0} == 25'h1001100) & (cpu_0_instruction_master_read)) & cpu_0_instruction_master_read;
  //cpu_0/data_master granted audio_controller_0/avalon_slave_0 last time, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          last_cycle_cpu_0_data_master_granted_slave_audio_controller_0_avalon_slave_0 <= 0;
      else
        last_cycle_cpu_0_data_master_granted_slave_audio_controller_0_avalon_slave_0 <= cpu_0_data_master_saved_grant_audio_controller_0_avalon_slave_0 ? 1 : (audio_controller_0_avalon_slave_0_arbitration_holdoff_internal | ~cpu_0_data_master_requests_audio_controller_0_avalon_slave_0) ? 0 : last_cycle_cpu_0_data_master_granted_slave_audio_controller_0_avalon_slave_0;
    end


  //cpu_0_data_master_continuerequest continued request, which is an e_mux
  assign cpu_0_data_master_continuerequest = last_cycle_cpu_0_data_master_granted_slave_audio_controller_0_avalon_slave_0 & cpu_0_data_master_requests_audio_controller_0_avalon_slave_0;

  assign cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0 = cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0 & ~(cpu_0_data_master_arbiterlock);
  //allow new arb cycle for audio_controller_0/avalon_slave_0, which is an e_assign
  assign audio_controller_0_avalon_slave_0_allow_new_arb_cycle = ~cpu_0_data_master_arbiterlock & ~cpu_0_instruction_master_arbiterlock;

  //cpu_0/instruction_master assignment into master qualified-requests vector for audio_controller_0/avalon_slave_0, which is an e_assign
  assign audio_controller_0_avalon_slave_0_master_qreq_vector[0] = cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0;

  //cpu_0/instruction_master grant audio_controller_0/avalon_slave_0, which is an e_assign
  assign cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0 = audio_controller_0_avalon_slave_0_grant_vector[0];

  //cpu_0/instruction_master saved-grant audio_controller_0/avalon_slave_0, which is an
```

```
e_assign
  assign cpu_0_instruction_master_saved_grant_audio_controller_0_avalon_slave_0 =
audio_controller_0_avalon_slave_0_arb_winner[0] &&
cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0;

  //cpu_0/data_master assignment into master qualified-requests vector for
audio_controller_0/avalon_slave_0, which is an e_assign
  assign audio_controller_0_avalon_slave_0_master_qreq_vector[1] =
cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0;

  //cpu_0/data_master grant audio_controller_0/avalon_slave_0, which is an e_assign
  assign cpu_0_data_master_granted_audio_controller_0_avalon_slave_0 =
audio_controller_0_avalon_slave_0_grant_vector[1];

  //cpu_0/data_master saved-grant audio_controller_0/avalon_slave_0, which is an e_assign
  assign cpu_0_data_master_saved_grant_audio_controller_0_avalon_slave_0 =
audio_controller_0_avalon_slave_0_arb_winner[1] &&
cpu_0_data_master_requests_audio_controller_0_avalon_slave_0;

  //audio_controller_0/avalon_slave_0 chosen-master double-vector, which is an e_assign
  assign audio_controller_0_avalon_slave_0_chosen_master_double_vector =
{audio_controller_0_avalon_slave_0_master_qreq_vector,
audio_controller_0_avalon_slave_0_master_qreq_vector} &
({~audio_controller_0_avalon_slave_0_master_qreq_vector,
~audio_controller_0_avalon_slave_0_master_qreq_vector} +
audio_controller_0_avalon_slave_0_arb_addend);

  //stable onehot encoding of arb winner
  assign audio_controller_0_avalon_slave_0_arb_winner =
(audio_controller_0_avalon_slave_0_allow_new_arb_cycle & |
audio_controller_0_avalon_slave_0_grant_vector) ?
audio_controller_0_avalon_slave_0_grant_vector :
audio_controller_0_avalon_slave_0_saved_chosen_master_vector;

  //saved audio_controller_0_avalon_slave_0_grant_vector, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          audio_controller_0_avalon_slave_0_saved_chosen_master_vector <= 0;
      else if (audio_controller_0_avalon_slave_0_allow_new_arb_cycle)
          audio_controller_0_avalon_slave_0_saved_chosen_master_vector <=
|audio_controller_0_avalon_slave_0_grant_vector ?
audio_controller_0_avalon_slave_0_grant_vector :
audio_controller_0_avalon_slave_0_saved_chosen_master_vector;
    end


  //onehot encoding of chosen master
  assign audio_controller_0_avalon_slave_0_grant_vector =
{(audio_controller_0_avalon_slave_0_chosen_master_double_vector[1] |
audio_controller_0_avalon_slave_0_chosen_master_double_vector[3]),
    (audio_controller_0_avalon_slave_0_chosen_master_double_vector[0] |
audio_controller_0_avalon_slave_0_chosen_master_double_vector[2])};

  //audio_controller_0/avalon_slave_0 chosen master rotated left, which is an e_assign
  assign audio_controller_0_avalon_slave_0_chosen_master_rot_left =
(audio_controller_0_avalon_slave_0_arb_winner << 1) ?
(audio_controller_0_avalon_slave_0_arb_winner << 1) : 1;
```

```
  //audio_controller_0/avalon_slave_0's addend for next-master-grant
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          audio_controller_0_avalon_slave_0_arb_addend <= 1;
      else if (|audio_controller_0_avalon_slave_0_grant_vector)
          audio_controller_0_avalon_slave_0_arb_addend                                    <=
audio_controller_0_avalon_slave_0_end_xfer?
audio_controller_0_avalon_slave_0_chosen_master_rot_left                                  :
audio_controller_0_avalon_slave_0_grant_vector;
    end


  //audio_controller_0_avalon_slave_0_reset_n assignment, which is an e_assign
  assign audio_controller_0_avalon_slave_0_reset_n = reset_n;

  assign                  audio_controller_0_avalon_slave_0_chipselect                    =
cpu_0_data_master_granted_audio_controller_0_avalon_slave_0                               |
cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0;
  //audio_controller_0_avalon_slave_0_firsttransfer first transaction, which is an e_assign
  assign                audio_controller_0_avalon_slave_0_firsttransfer                   =
audio_controller_0_avalon_slave_0_begins_xfer                                             ?
audio_controller_0_avalon_slave_0_unreg_firsttransfer                                     :
audio_controller_0_avalon_slave_0_reg_firsttransfer;

  //audio_controller_0_avalon_slave_0_unreg_firsttransfer first transaction, which is an
e_assign
  assign              audio_controller_0_avalon_slave_0_unreg_firsttransfer             =
~(audio_controller_0_avalon_slave_0_slavearbiterlockenable                                &
audio_controller_0_avalon_slave_0_any_continuerequest);

  //audio_controller_0_avalon_slave_0_reg_firsttransfer first transaction, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          audio_controller_0_avalon_slave_0_reg_firsttransfer <= 1'b1;
      else if (audio_controller_0_avalon_slave_0_begins_xfer)
          audio_controller_0_avalon_slave_0_reg_firsttransfer                             <=
audio_controller_0_avalon_slave_0_unreg_firsttransfer;
    end


  //audio_controller_0_avalon_slave_0_beginbursttransfer_internal begin burst transfer, which
is an e_assign
  assign          audio_controller_0_avalon_slave_0_beginbursttransfer_internal       =
audio_controller_0_avalon_slave_0_begins_xfer;

  //audio_controller_0_avalon_slave_0_arbitration_holdoff_internal arbitration_holdoff, which
is an e_assign
  assign          audio_controller_0_avalon_slave_0_arbitration_holdoff_internal      =
audio_controller_0_avalon_slave_0_begins_xfer                                             &
audio_controller_0_avalon_slave_0_firsttransfer;

  //audio_controller_0_avalon_slave_0_read assignment, which is an e_mux
  assign                  audio_controller_0_avalon_slave_0_read                          =
(cpu_0_data_master_granted_audio_controller_0_avalon_slave_0  &  cpu_0_data_master_read)
|          (cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0          &
```

```
cpu_0_instruction_master_read);

  //audio_controller_0_avalon_slave_0_write assignment, which is an e_mux
  assign audio_controller_0_avalon_slave_0_write =
cpu_0_data_master_granted_audio_controller_0_avalon_slave_0 & cpu_0_data_master_write;

  assign shifted_address_to_audio_controller_0_avalon_slave_0_from_cpu_0_data_master =
{cpu_0_data_master_address_to_slave >> 2,
    cpu_0_data_master_dbs_address[1],
    {1 {1'b0}}};

  //audio_controller_0_avalon_slave_0_address mux, which is an e_mux
  assign audio_controller_0_avalon_slave_0_address =
(cpu_0_data_master_granted_audio_controller_0_avalon_slave_0)?
(shifted_address_to_audio_controller_0_avalon_slave_0_from_cpu_0_data_master >> 1) :

(shifted_address_to_audio_controller_0_avalon_slave_0_from_cpu_0_instruction_master >> 1);

  assign
shifted_address_to_audio_controller_0_avalon_slave_0_from_cpu_0_instruction_master =
{cpu_0_instruction_master_address_to_slave >> 2,
    cpu_0_instruction_master_dbs_address[1],
    {1 {1'b0}}};

  //d1_audio_controller_0_avalon_slave_0_end_xfer register, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_audio_controller_0_avalon_slave_0_end_xfer <= 1;
      else
        d1_audio_controller_0_avalon_slave_0_end_xfer <=
audio_controller_0_avalon_slave_0_end_xfer;
    end


  //audio_controller_0_avalon_slave_0_waits_for_read in a cycle, which is an e_mux
  assign audio_controller_0_avalon_slave_0_waits_for_read =
audio_controller_0_avalon_slave_0_in_a_read_cycle &
audio_controller_0_avalon_slave_0_begins_xfer;

  //audio_controller_0_avalon_slave_0_in_a_read_cycle assignment, which is an e_assign
  assign audio_controller_0_avalon_slave_0_in_a_read_cycle =
(cpu_0_data_master_granted_audio_controller_0_avalon_slave_0 & cpu_0_data_master_read)
|          (cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0 &
cpu_0_instruction_master_read);

  //in_a_read_cycle assignment, which is an e_mux
  assign in_a_read_cycle = audio_controller_0_avalon_slave_0_in_a_read_cycle;

  //audio_controller_0_avalon_slave_0_waits_for_write in a cycle, which is an e_mux
  assign audio_controller_0_avalon_slave_0_waits_for_write =
audio_controller_0_avalon_slave_0_in_a_write_cycle & 0;

  //audio_controller_0_avalon_slave_0_in_a_write_cycle assignment, which is an e_assign
  assign audio_controller_0_avalon_slave_0_in_a_write_cycle =
cpu_0_data_master_granted_audio_controller_0_avalon_slave_0 & cpu_0_data_master_write;

  //in_a_write_cycle assignment, which is an e_mux
```

```
  assign in_a_write_cycle = audio_controller_0_avalon_slave_0_in_a_write_cycle;

  assign wait_for_audio_controller_0_avalon_slave_0_counter = 0;
  assign {cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0_segment_1,
cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0_segment_0}                =
cpu_0_data_master_byteenable;
  assign            cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0          =
((cpu_0_data_master_dbs_address[1]                                  ==                  0))?
cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0_segment_0 :
      cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0_segment_1;


//synthesis translate_off
//////////////// SIMULATION-ONLY CONTENTS
  //audio_controller_0/avalon_slave_0 enable non-zero assertions, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          enable_nonzero_assertions <= 0;
      else
        enable_nonzero_assertions <= 1'b1;
    end


  //grant signals are active simultaneously, which is an e_process
  always @(posedge clk)
    begin
      if            (cpu_0_data_master_granted_audio_controller_0_avalon_slave_0            +
cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0 > 1)
        begin
          $write("%0d ns: > 1 of grant signals are active simultaneously", $time);
          $stop;
        end
    end


  //saved_grant signals are active simultaneously, which is an e_process
  always @(posedge clk)
    begin
      if          (cpu_0_data_master_saved_grant_audio_controller_0_avalon_slave_0          +
cpu_0_instruction_master_saved_grant_audio_controller_0_avalon_slave_0 > 1)
        begin
          $write("%0d ns: > 1 of saved_grant signals are active simultaneously", $time);
          $stop;
        end
    end



//////////////// END SIMULATION-ONLY CONTENTS

//synthesis translate_on

endmodule


// synthesis translate_off
`timescale 1ns / 1ps
```

```
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module command_0_avalon_slave_0_arbitrator (
                                             // inputs:
                                              clk,
                                              command_0_avalon_slave_0_readdata,
                                              cpu_0_data_master_address_to_slave,
                                              cpu_0_data_master_read,
                                              cpu_0_data_master_waitrequest,
                                              cpu_0_data_master_write,
                                              cpu_0_data_master_writedata,

cpu_0_instruction_master_address_to_slave,
                                              cpu_0_instruction_master_read,
                                              reset_n,

                                             // outputs:
                                              command_0_avalon_slave_0_address,

command_0_avalon_slave_0_chipselect,
                                              command_0_avalon_slave_0_read,

command_0_avalon_slave_0_readdata_from_sa,
                                              command_0_avalon_slave_0_reset_n,
                                              command_0_avalon_slave_0_write,
                                              command_0_avalon_slave_0_writedata,

cpu_0_data_master_granted_command_0_avalon_slave_0,

cpu_0_data_master_qualified_request_command_0_avalon_slave_0,

cpu_0_data_master_read_data_valid_command_0_avalon_slave_0,

cpu_0_data_master_requests_command_0_avalon_slave_0,

cpu_0_instruction_master_granted_command_0_avalon_slave_0,

cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0,

cpu_0_instruction_master_read_data_valid_command_0_avalon_slave_0,

cpu_0_instruction_master_requests_command_0_avalon_slave_0,

d1_command_0_avalon_slave_0_end_xfer
                                                    )
;

  output  [  4: 0] command_0_avalon_slave_0_address;
  output           command_0_avalon_slave_0_chipselect;
  output           command_0_avalon_slave_0_read;
  output  [ 31: 0] command_0_avalon_slave_0_readdata_from_sa;
  output           command_0_avalon_slave_0_reset_n;
  output           command_0_avalon_slave_0_write;
  output  [ 31: 0] command_0_avalon_slave_0_writedata;
```

```
  output              cpu_0_data_master_granted_command_0_avalon_slave_0;
  output              cpu_0_data_master_qualified_request_command_0_avalon_slave_0;
  output              cpu_0_data_master_read_data_valid_command_0_avalon_slave_0;
  output              cpu_0_data_master_requests_command_0_avalon_slave_0;
  output              cpu_0_instruction_master_granted_command_0_avalon_slave_0;
  output
cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0;
  output
cpu_0_instruction_master_read_data_valid_command_0_avalon_slave_0;
  output              cpu_0_instruction_master_requests_command_0_avalon_slave_0;
  output              d1_command_0_avalon_slave_0_end_xfer;
  input               clk;
  input    [ 31: 0] command_0_avalon_slave_0_readdata;
  input    [ 24: 0] cpu_0_data_master_address_to_slave;
  input               cpu_0_data_master_read;
  input               cpu_0_data_master_waitrequest;
  input               cpu_0_data_master_write;
  input    [ 31: 0] cpu_0_data_master_writedata;
  input    [ 24: 0] cpu_0_instruction_master_address_to_slave;
  input               cpu_0_instruction_master_read;
  input               reset_n;

  wire     [  4: 0] command_0_avalon_slave_0_address;
  wire              command_0_avalon_slave_0_allgrants;
  wire              command_0_avalon_slave_0_allow_new_arb_cycle;
  wire              command_0_avalon_slave_0_any_bursting_master_saved_grant;
  wire              command_0_avalon_slave_0_any_continuerequest;
  reg      [  1: 0] command_0_avalon_slave_0_arb_addend;
  wire              command_0_avalon_slave_0_arb_counter_enable;
  reg      [  1: 0] command_0_avalon_slave_0_arb_share_counter;
  wire     [  1: 0] command_0_avalon_slave_0_arb_share_counter_next_value;
  wire     [  1: 0] command_0_avalon_slave_0_arb_share_set_values;
  wire     [  1: 0] command_0_avalon_slave_0_arb_winner;
  wire              command_0_avalon_slave_0_arbitration_holdoff_internal;
  wire              command_0_avalon_slave_0_beginbursttransfer_internal;
  wire              command_0_avalon_slave_0_begins_xfer;
  wire              command_0_avalon_slave_0_chipselect;
  wire     [  3: 0] command_0_avalon_slave_0_chosen_master_double_vector;
  wire     [  1: 0] command_0_avalon_slave_0_chosen_master_rot_left;
  wire              command_0_avalon_slave_0_end_xfer;
  wire              command_0_avalon_slave_0_firsttransfer;
  wire     [  1: 0] command_0_avalon_slave_0_grant_vector;
  wire              command_0_avalon_slave_0_in_a_read_cycle;
  wire              command_0_avalon_slave_0_in_a_write_cycle;
  wire     [  1: 0] command_0_avalon_slave_0_master_qreq_vector;
  wire              command_0_avalon_slave_0_non_bursting_master_requests;
  wire              command_0_avalon_slave_0_read;
  wire     [ 31: 0] command_0_avalon_slave_0_readdata_from_sa;
  reg               command_0_avalon_slave_0_reg_firsttransfer;
  wire              command_0_avalon_slave_0_reset_n;
  reg      [  1: 0] command_0_avalon_slave_0_saved_chosen_master_vector;
  reg               command_0_avalon_slave_0_slavearbiterlockenable;
  wire              command_0_avalon_slave_0_slavearbiterlockenable2;
  wire              command_0_avalon_slave_0_unreg_firsttransfer;
  wire              command_0_avalon_slave_0_waits_for_read;
  wire              command_0_avalon_slave_0_waits_for_write;
  wire              command_0_avalon_slave_0_write;
  wire     [ 31: 0] command_0_avalon_slave_0_writedata;
```

```
  wire                    cpu_0_data_master_arbiterlock;
  wire                    cpu_0_data_master_arbiterlock2;
  wire                    cpu_0_data_master_continuerequest;
  wire                    cpu_0_data_master_granted_command_0_avalon_slave_0;
  wire                    cpu_0_data_master_qualified_request_command_0_avalon_slave_0;
  wire                    cpu_0_data_master_read_data_valid_command_0_avalon_slave_0;
  wire                    cpu_0_data_master_requests_command_0_avalon_slave_0;
  wire                    cpu_0_data_master_saved_grant_command_0_avalon_slave_0;
  wire                    cpu_0_instruction_master_arbiterlock;
  wire                    cpu_0_instruction_master_arbiterlock2;
  wire                    cpu_0_instruction_master_continuerequest;
  wire                    cpu_0_instruction_master_granted_command_0_avalon_slave_0;
  wire
cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0;
  wire
cpu_0_instruction_master_read_data_valid_command_0_avalon_slave_0;
  wire                    cpu_0_instruction_master_requests_command_0_avalon_slave_0;
  wire                    cpu_0_instruction_master_saved_grant_command_0_avalon_slave_0;
  reg                     d1_command_0_avalon_slave_0_end_xfer;
  reg                     d1_reasons_to_wait;
  reg                     enable_nonzero_assertions;
  wire                    end_xfer_arb_share_counter_term_command_0_avalon_slave_0;
  wire                    in_a_read_cycle;
  wire                    in_a_write_cycle;
  reg
last_cycle_cpu_0_data_master_granted_slave_command_0_avalon_slave_0;
  reg
last_cycle_cpu_0_instruction_master_granted_slave_command_0_avalon_slave_0;
  wire      [ 24: 0] shifted_address_to_command_0_avalon_slave_0_from_cpu_0_data_master;
  wire                                                    [ 24: 0]
shifted_address_to_command_0_avalon_slave_0_from_cpu_0_instruction_master;
  wire                    wait_for_command_0_avalon_slave_0_counter;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_reasons_to_wait <= 0;
      else
        d1_reasons_to_wait <= ~command_0_avalon_slave_0_end_xfer;
    end


  assign      command_0_avalon_slave_0_begins_xfer      =      ~d1_reasons_to_wait      &
((cpu_0_data_master_qualified_request_command_0_avalon_slave_0                          |
cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0));
  //assign                    command_0_avalon_slave_0_readdata_from_sa                 =
command_0_avalon_slave_0_readdata so that symbol knows where to group signals which may
go to master only, which is an e_assign
  assign                    command_0_avalon_slave_0_readdata_from_sa                 =
command_0_avalon_slave_0_readdata;

  assign                cpu_0_data_master_requests_command_0_avalon_slave_0           =
({cpu_0_data_master_address_to_slave[24 : 7] , 7'b0} == 25'h100) & (cpu_0_data_master_read
| cpu_0_data_master_write);
  //command_0_avalon_slave_0_arb_share_counter set values, which is an e_mux
  assign command_0_avalon_slave_0_arb_share_set_values = 1;

  //command_0_avalon_slave_0_non_bursting_master_requests mux, which is an e_mux
  assign                command_0_avalon_slave_0_non_bursting_master_requests         =
```

```
cpu_0_data_master_requests_command_0_avalon_slave_0 |
      cpu_0_instruction_master_requests_command_0_avalon_slave_0 |
      cpu_0_data_master_requests_command_0_avalon_slave_0 |
      cpu_0_instruction_master_requests_command_0_avalon_slave_0;

  //command_0_avalon_slave_0_any_bursting_master_saved_grant mux, which is an e_mux
  assign command_0_avalon_slave_0_any_bursting_master_saved_grant = 0;

  //command_0_avalon_slave_0_arb_share_counter_next_value assignment, which is an
e_assign
  assign command_0_avalon_slave_0_arb_share_counter_next_value =
command_0_avalon_slave_0_firsttransfer ?
(command_0_avalon_slave_0_arb_share_set_values - 1) :
|command_0_avalon_slave_0_arb_share_counter ?
(command_0_avalon_slave_0_arb_share_counter - 1) : 0;

  //command_0_avalon_slave_0_allgrants all slave grants, which is an e_mux
  assign command_0_avalon_slave_0_allgrants = (|command_0_avalon_slave_0_grant_vector)
|
      (|command_0_avalon_slave_0_grant_vector) |
      (|command_0_avalon_slave_0_grant_vector) |
      (|command_0_avalon_slave_0_grant_vector);

  //command_0_avalon_slave_0_end_xfer assignment, which is an e_assign
  assign command_0_avalon_slave_0_end_xfer =
~(command_0_avalon_slave_0_waits_for_read |
command_0_avalon_slave_0_waits_for_write);

  //end_xfer_arb_share_counter_term_command_0_avalon_slave_0 arb share counter enable
term, which is an e_assign
  assign end_xfer_arb_share_counter_term_command_0_avalon_slave_0 =
command_0_avalon_slave_0_end_xfer &
(~command_0_avalon_slave_0_any_bursting_master_saved_grant | in_a_read_cycle |
in_a_write_cycle);

  //command_0_avalon_slave_0_arb_share_counter arbitration counter enable, which is an
e_assign
  assign command_0_avalon_slave_0_arb_counter_enable =
(end_xfer_arb_share_counter_term_command_0_avalon_slave_0 &
command_0_avalon_slave_0_allgrants) |
(end_xfer_arb_share_counter_term_command_0_avalon_slave_0 &
~command_0_avalon_slave_0_non_bursting_master_requests);

  //command_0_avalon_slave_0_arb_share_counter counter, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          command_0_avalon_slave_0_arb_share_counter <= 0;
      else if (command_0_avalon_slave_0_arb_counter_enable)
          command_0_avalon_slave_0_arb_share_counter <=
command_0_avalon_slave_0_arb_share_counter_next_value;
    end


  //command_0_avalon_slave_0_slavearbiterlockenable slave enables arbiterlock, which is an
e_register
  always @(posedge clk or negedge reset_n)
    begin
```

```
        if (reset_n == 0)
            command_0_avalon_slave_0_slavearbiterlockenable <= 0;
        else if ((|command_0_avalon_slave_0_master_qreq_vector &
end_xfer_arb_share_counter_term_command_0_avalon_slave_0) |
(end_xfer_arb_share_counter_term_command_0_avalon_slave_0 &
~command_0_avalon_slave_0_non_bursting_master_requests))
            command_0_avalon_slave_0_slavearbiterlockenable <=
|command_0_avalon_slave_0_arb_share_counter_next_value;
      end


   //cpu_0/data_master command_0/avalon_slave_0 arbiterlock, which is an e_assign
   assign cpu_0_data_master_arbiterlock = command_0_avalon_slave_0_slavearbiterlockenable
& cpu_0_data_master_continuerequest;

   //command_0_avalon_slave_0_slavearbiterlockenable2 slave enables arbiterlock2, which is an
e_assign
   assign command_0_avalon_slave_0_slavearbiterlockenable2 =
|command_0_avalon_slave_0_arb_share_counter_next_value;

   //cpu_0/data_master command_0/avalon_slave_0 arbiterlock2, which is an e_assign
   assign cpu_0_data_master_arbiterlock2 =
command_0_avalon_slave_0_slavearbiterlockenable2 & cpu_0_data_master_continuerequest;

   //cpu_0/instruction_master command_0/avalon_slave_0 arbiterlock, which is an e_assign
   assign cpu_0_instruction_master_arbiterlock =
command_0_avalon_slave_0_slavearbiterlockenable &
cpu_0_instruction_master_continuerequest;

   //cpu_0/instruction_master command_0/avalon_slave_0 arbiterlock2, which is an e_assign
   assign cpu_0_instruction_master_arbiterlock2 =
command_0_avalon_slave_0_slavearbiterlockenable2 &
cpu_0_instruction_master_continuerequest;

   //cpu_0/instruction_master granted command_0/avalon_slave_0 last time, which is an
e_register
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
            last_cycle_cpu_0_instruction_master_granted_slave_command_0_avalon_slave_0
<= 0;
         else
           last_cycle_cpu_0_instruction_master_granted_slave_command_0_avalon_slave_0 <=
cpu_0_instruction_master_saved_grant_command_0_avalon_slave_0 ? 1 :
(command_0_avalon_slave_0_arbitration_holdoff_internal |
~cpu_0_instruction_master_requests_command_0_avalon_slave_0) ? 0 :
last_cycle_cpu_0_instruction_master_granted_slave_command_0_avalon_slave_0;
      end


   //cpu_0_instruction_master_continuerequest continued request, which is an e_mux
   assign cpu_0_instruction_master_continuerequest =
last_cycle_cpu_0_instruction_master_granted_slave_command_0_avalon_slave_0 &
cpu_0_instruction_master_requests_command_0_avalon_slave_0;

   //command_0_avalon_slave_0_any_continuerequest at least one master continues
requesting, which is an e_mux
   assign command_0_avalon_slave_0_any_continuerequest =
```

```
cpu_0_instruction_master_continuerequest |
      cpu_0_data_master_continuerequest;

   assign cpu_0_data_master_qualified_request_command_0_avalon_slave_0 =
cpu_0_data_master_requests_command_0_avalon_slave_0 &
~(((~cpu_0_data_master_waitrequest) & cpu_0_data_master_write) |
cpu_0_instruction_master_arbiterlock);
   //command_0_avalon_slave_0_writedata mux, which is an e_mux
   assign command_0_avalon_slave_0_writedata = cpu_0_data_master_writedata;

   assign cpu_0_instruction_master_requests_command_0_avalon_slave_0 =
(({cpu_0_instruction_master_address_to_slave[24 : 7] , 7'b0} == 25'h100) &
(cpu_0_instruction_master_read)) & cpu_0_instruction_master_read;
   //cpu_0/data_master granted command_0/avalon_slave_0 last time, which is an e_register
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               last_cycle_cpu_0_data_master_granted_slave_command_0_avalon_slave_0 <= 0;
         else
            last_cycle_cpu_0_data_master_granted_slave_command_0_avalon_slave_0 <=
cpu_0_data_master_saved_grant_command_0_avalon_slave_0 ? 1 :
(command_0_avalon_slave_0_arbitration_holdoff_internal |
~cpu_0_data_master_requests_command_0_avalon_slave_0) ? 0 :
last_cycle_cpu_0_data_master_granted_slave_command_0_avalon_slave_0;
      end


   //cpu_0_data_master_continuerequest continued request, which is an e_mux
   assign cpu_0_data_master_continuerequest =
last_cycle_cpu_0_data_master_granted_slave_command_0_avalon_slave_0 &
cpu_0_data_master_requests_command_0_avalon_slave_0;

   assign cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0 =
cpu_0_instruction_master_requests_command_0_avalon_slave_0 &
~(cpu_0_data_master_arbiterlock);
   //allow new arb cycle for command_0/avalon_slave_0, which is an e_assign
   assign command_0_avalon_slave_0_allow_new_arb_cycle = ~cpu_0_data_master_arbiterlock
& ~cpu_0_instruction_master_arbiterlock;

   //cpu_0/instruction_master assignment into master qualified-requests vector for
command_0/avalon_slave_0, which is an e_assign
   assign command_0_avalon_slave_0_master_qreq_vector[0] =
cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0;

   //cpu_0/instruction_master grant command_0/avalon_slave_0, which is an e_assign
   assign cpu_0_instruction_master_granted_command_0_avalon_slave_0 =
command_0_avalon_slave_0_grant_vector[0];

   //cpu_0/instruction_master saved-grant command_0/avalon_slave_0, which is an e_assign
   assign cpu_0_instruction_master_saved_grant_command_0_avalon_slave_0 =
command_0_avalon_slave_0_arb_winner[0] &&
cpu_0_instruction_master_requests_command_0_avalon_slave_0;

   //cpu_0/data_master assignment into master qualified-requests vector for
command_0/avalon_slave_0, which is an e_assign
   assign command_0_avalon_slave_0_master_qreq_vector[1] =
cpu_0_data_master_qualified_request_command_0_avalon_slave_0;
```

```
  //cpu_0/data_master grant command_0/avalon_slave_0, which is an e_assign
  assign cpu_0_data_master_granted_command_0_avalon_slave_0 =
command_0_avalon_slave_0_grant_vector[1];

  //cpu_0/data_master saved-grant command_0/avalon_slave_0, which is an e_assign
  assign cpu_0_data_master_saved_grant_command_0_avalon_slave_0 =
command_0_avalon_slave_0_arb_winner[1] &&
cpu_0_data_master_requests_command_0_avalon_slave_0;

  //command_0/avalon_slave_0 chosen-master double-vector, which is an e_assign
  assign command_0_avalon_slave_0_chosen_master_double_vector =
{command_0_avalon_slave_0_master_qreq_vector,
command_0_avalon_slave_0_master_qreq_vector} &
({~command_0_avalon_slave_0_master_qreq_vector,
~command_0_avalon_slave_0_master_qreq_vector} +
command_0_avalon_slave_0_arb_addend);

  //stable onehot encoding of arb winner
  assign command_0_avalon_slave_0_arb_winner =
(command_0_avalon_slave_0_allow_new_arb_cycle & |
command_0_avalon_slave_0_grant_vector) ? command_0_avalon_slave_0_grant_vector :
command_0_avalon_slave_0_saved_chosen_master_vector;

  //saved command_0_avalon_slave_0_grant_vector, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          command_0_avalon_slave_0_saved_chosen_master_vector <= 0;
      else if (command_0_avalon_slave_0_allow_new_arb_cycle)
          command_0_avalon_slave_0_saved_chosen_master_vector <=
|command_0_avalon_slave_0_grant_vector ? command_0_avalon_slave_0_grant_vector :
command_0_avalon_slave_0_saved_chosen_master_vector;
    end


  //onehot encoding of chosen master
  assign command_0_avalon_slave_0_grant_vector =
{(command_0_avalon_slave_0_chosen_master_double_vector[1] |
command_0_avalon_slave_0_chosen_master_double_vector[3]),
    (command_0_avalon_slave_0_chosen_master_double_vector[0] |
command_0_avalon_slave_0_chosen_master_double_vector[2])};

  //command_0/avalon_slave_0 chosen master rotated left, which is an e_assign
  assign command_0_avalon_slave_0_chosen_master_rot_left =
(command_0_avalon_slave_0_arb_winner << 1) ? (command_0_avalon_slave_0_arb_winner <<
1) : 1;

  //command_0/avalon_slave_0's addend for next-master-grant
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          command_0_avalon_slave_0_arb_addend <= 1;
      else if (|command_0_avalon_slave_0_grant_vector)
          command_0_avalon_slave_0_arb_addend <=
command_0_avalon_slave_0_end_xfer? command_0_avalon_slave_0_chosen_master_rot_left :
command_0_avalon_slave_0_grant_vector;
    end
```

```
  //command_0_avalon_slave_0_reset_n assignment, which is an e_assign
  assign command_0_avalon_slave_0_reset_n = reset_n;

  assign                          command_0_avalon_slave_0_chipselect                          =
cpu_0_data_master_granted_command_0_avalon_slave_0                                             |
cpu_0_instruction_master_granted_command_0_avalon_slave_0;
  //command_0_avalon_slave_0_firsttransfer first transaction, which is an e_assign
  assign command_0_avalon_slave_0_firsttransfer = command_0_avalon_slave_0_begins_xfer ?
command_0_avalon_slave_0_unreg_firsttransfer                                                   :
command_0_avalon_slave_0_reg_firsttransfer;

  //command_0_avalon_slave_0_unreg_firsttransfer first transaction, which is an e_assign
  assign                    command_0_avalon_slave_0_unreg_firsttransfer                       =
~(command_0_avalon_slave_0_slavearbiterlockenable                                              &
command_0_avalon_slave_0_any_continuerequest);

  //command_0_avalon_slave_0_reg_firsttransfer first transaction, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          command_0_avalon_slave_0_reg_firsttransfer <= 1'b1;
      else if (command_0_avalon_slave_0_begins_xfer)
          command_0_avalon_slave_0_reg_firsttransfer                                         <=
command_0_avalon_slave_0_unreg_firsttransfer;
    end


  //command_0_avalon_slave_0_beginbursttransfer_internal begin burst transfer, which is an
e_assign
  assign              command_0_avalon_slave_0_beginbursttransfer_internal                   =
command_0_avalon_slave_0_begins_xfer;

  //command_0_avalon_slave_0_arbitration_holdoff_internal arbitration_holdoff, which is an
e_assign
  assign              command_0_avalon_slave_0_arbitration_holdoff_internal                  =
command_0_avalon_slave_0_begins_xfer & command_0_avalon_slave_0_firsttransfer;

  //command_0_avalon_slave_0_read assignment, which is an e_mux
  assign                          command_0_avalon_slave_0_read                              =
(cpu_0_data_master_granted_command_0_avalon_slave_0   &   cpu_0_data_master_read)   |
(cpu_0_instruction_master_granted_command_0_avalon_slave_0                                     &
cpu_0_instruction_master_read);

  //command_0_avalon_slave_0_write assignment, which is an e_mux
  assign                          command_0_avalon_slave_0_write                             =
cpu_0_data_master_granted_command_0_avalon_slave_0 & cpu_0_data_master_write;

  assign      shifted_address_to_command_0_avalon_slave_0_from_cpu_0_data_master      =
cpu_0_data_master_address_to_slave;
  //command_0_avalon_slave_0_address mux, which is an e_mux
  assign                          command_0_avalon_slave_0_address                           =
(cpu_0_data_master_granted_command_0_avalon_slave_0)?
(shifted_address_to_command_0_avalon_slave_0_from_cpu_0_data_master >> 2) :
    (shifted_address_to_command_0_avalon_slave_0_from_cpu_0_instruction_master >> 2);

  assign   shifted_address_to_command_0_avalon_slave_0_from_cpu_0_instruction_master   =
cpu_0_instruction_master_address_to_slave;
```

```
  //d1_command_0_avalon_slave_0_end_xfer register, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_command_0_avalon_slave_0_end_xfer <= 1;
      else
        d1_command_0_avalon_slave_0_end_xfer <= command_0_avalon_slave_0_end_xfer;
    end


  //command_0_avalon_slave_0_waits_for_read in a cycle, which is an e_mux
  assign command_0_avalon_slave_0_waits_for_read =
command_0_avalon_slave_0_in_a_read_cycle & command_0_avalon_slave_0_begins_xfer;

  //command_0_avalon_slave_0_in_a_read_cycle assignment, which is an e_assign
  assign command_0_avalon_slave_0_in_a_read_cycle =
(cpu_0_data_master_granted_command_0_avalon_slave_0 & cpu_0_data_master_read) |
(cpu_0_instruction_master_granted_command_0_avalon_slave_0 &
cpu_0_instruction_master_read);

  //in_a_read_cycle assignment, which is an e_mux
  assign in_a_read_cycle = command_0_avalon_slave_0_in_a_read_cycle;

  //command_0_avalon_slave_0_waits_for_write in a cycle, which is an e_mux
  assign command_0_avalon_slave_0_waits_for_write =
command_0_avalon_slave_0_in_a_write_cycle & 0;

  //command_0_avalon_slave_0_in_a_write_cycle assignment, which is an e_assign
  assign command_0_avalon_slave_0_in_a_write_cycle =
cpu_0_data_master_granted_command_0_avalon_slave_0 & cpu_0_data_master_write;

  //in_a_write_cycle assignment, which is an e_mux
  assign in_a_write_cycle = command_0_avalon_slave_0_in_a_write_cycle;

  assign wait_for_command_0_avalon_slave_0_counter = 0;

//synthesis translate_off
//////////////// SIMULATION-ONLY CONTENTS
  //command_0/avalon_slave_0 enable non-zero assertions, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          enable_nonzero_assertions <= 0;
      else
        enable_nonzero_assertions <= 1'b1;
    end


  //grant signals are active simultaneously, which is an e_process
  always @(posedge clk)
    begin
      if (cpu_0_data_master_granted_command_0_avalon_slave_0 +
cpu_0_instruction_master_granted_command_0_avalon_slave_0 > 1)
        begin
          $write("%0d ns: > 1 of grant signals are active simultaneously", $time);
          $stop;
        end
    end
```

```
  //saved_grant signals are active simultaneously, which is an e_process
  always @(posedge clk)
    begin
      if (cpu_0_data_master_saved_grant_command_0_avalon_slave_0 +
cpu_0_instruction_master_saved_grant_command_0_avalon_slave_0 > 1)
        begin
          $write("%0d ns: > 1 of saved_grant signals are active simultaneously", $time);
          $stop;
        end
    end



//////////////// END SIMULATION-ONLY CONTENTS

//synthesis translate_on

endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_jtag_debug_module_arbitrator (
                                            // inputs:
                                              clk,
                                              cpu_0_data_master_address_to_slave,
                                              cpu_0_data_master_byteenable,
                                              cpu_0_data_master_debugaccess,
                                              cpu_0_data_master_read,
                                              cpu_0_data_master_waitrequest,
                                              cpu_0_data_master_write,
                                              cpu_0_data_master_writedata,

cpu_0_instruction_master_address_to_slave,
                                              cpu_0_instruction_master_read,
                                              cpu_0_jtag_debug_module_readdata,

cpu_0_jtag_debug_module_resetrequest,
                                              reset_n,

                                            // outputs:

cpu_0_data_master_granted_cpu_0_jtag_debug_module,

cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module,

cpu_0_data_master_read_data_valid_cpu_0_jtag_debug_module,

cpu_0_data_master_requests_cpu_0_jtag_debug_module,
```

```
cpu_0_instruction_master_granted_cpu_0_jtag_debug_module,

cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module,

cpu_0_instruction_master_read_data_valid_cpu_0_jtag_debug_module,

cpu_0_instruction_master_requests_cpu_0_jtag_debug_module,
                                                    cpu_0_jtag_debug_module_address,

cpu_0_jtag_debug_module_begintransfer,
                                                    cpu_0_jtag_debug_module_byteenable,
                                                    cpu_0_jtag_debug_module_chipselect,
                                                    cpu_0_jtag_debug_module_debugaccess,

cpu_0_jtag_debug_module_readdata_from_sa,
                                                    cpu_0_jtag_debug_module_reset_n,

cpu_0_jtag_debug_module_resetrequest_from_sa,
                                                    cpu_0_jtag_debug_module_write,
                                                    cpu_0_jtag_debug_module_writedata,
                                                    d1_cpu_0_jtag_debug_module_end_xfer
                                                )
;

  output           cpu_0_data_master_granted_cpu_0_jtag_debug_module;
  output           cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module;
  output           cpu_0_data_master_read_data_valid_cpu_0_jtag_debug_module;
  output           cpu_0_data_master_requests_cpu_0_jtag_debug_module;
  output           cpu_0_instruction_master_granted_cpu_0_jtag_debug_module;
  output
cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module;
  output           cpu_0_instruction_master_read_data_valid_cpu_0_jtag_debug_module;
  output           cpu_0_instruction_master_requests_cpu_0_jtag_debug_module;
  output  [  8: 0] cpu_0_jtag_debug_module_address;
  output           cpu_0_jtag_debug_module_begintransfer;
  output  [  3: 0] cpu_0_jtag_debug_module_byteenable;
  output           cpu_0_jtag_debug_module_chipselect;
  output           cpu_0_jtag_debug_module_debugaccess;
  output  [ 31: 0] cpu_0_jtag_debug_module_readdata_from_sa;
  output           cpu_0_jtag_debug_module_reset_n;
  output           cpu_0_jtag_debug_module_resetrequest_from_sa;
  output           cpu_0_jtag_debug_module_write;
  output  [ 31: 0] cpu_0_jtag_debug_module_writedata;
  output           d1_cpu_0_jtag_debug_module_end_xfer;
  input            clk;
  input   [ 24: 0] cpu_0_data_master_address_to_slave;
  input   [  3: 0] cpu_0_data_master_byteenable;
  input            cpu_0_data_master_debugaccess;
  input            cpu_0_data_master_read;
  input            cpu_0_data_master_waitrequest;
  input            cpu_0_data_master_write;
  input   [ 31: 0] cpu_0_data_master_writedata;
  input   [ 24: 0] cpu_0_instruction_master_address_to_slave;
  input            cpu_0_instruction_master_read;
  input   [ 31: 0] cpu_0_jtag_debug_module_readdata;
  input            cpu_0_jtag_debug_module_resetrequest;
  input            reset_n;
```

```
  wire              cpu_0_data_master_arbiterlock;
  wire              cpu_0_data_master_arbiterlock2;
  wire              cpu_0_data_master_continuerequest;
  wire              cpu_0_data_master_granted_cpu_0_jtag_debug_module;
  wire              cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module;
  wire              cpu_0_data_master_read_data_valid_cpu_0_jtag_debug_module;
  wire              cpu_0_data_master_requests_cpu_0_jtag_debug_module;
  wire              cpu_0_data_master_saved_grant_cpu_0_jtag_debug_module;
  wire              cpu_0_instruction_master_arbiterlock;
  wire              cpu_0_instruction_master_arbiterlock2;
  wire              cpu_0_instruction_master_continuerequest;
  wire              cpu_0_instruction_master_granted_cpu_0_jtag_debug_module;
  wire
cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module;
  wire              cpu_0_instruction_master_read_data_valid_cpu_0_jtag_debug_module;
  wire              cpu_0_instruction_master_requests_cpu_0_jtag_debug_module;
  wire              cpu_0_instruction_master_saved_grant_cpu_0_jtag_debug_module;
  wire    [  8: 0] cpu_0_jtag_debug_module_address;
  wire              cpu_0_jtag_debug_module_allgrants;
  wire              cpu_0_jtag_debug_module_allow_new_arb_cycle;
  wire              cpu_0_jtag_debug_module_any_bursting_master_saved_grant;
  wire              cpu_0_jtag_debug_module_any_continuerequest;
  reg     [  1: 0] cpu_0_jtag_debug_module_arb_addend;
  wire              cpu_0_jtag_debug_module_arb_counter_enable;
  reg     [  1: 0] cpu_0_jtag_debug_module_arb_share_counter;
  wire    [  1: 0] cpu_0_jtag_debug_module_arb_share_counter_next_value;
  wire    [  1: 0] cpu_0_jtag_debug_module_arb_share_set_values;
  wire    [  1: 0] cpu_0_jtag_debug_module_arb_winner;
  wire              cpu_0_jtag_debug_module_arbitration_holdoff_internal;
  wire              cpu_0_jtag_debug_module_beginbursttransfer_internal;
  wire              cpu_0_jtag_debug_module_begins_xfer;
  wire              cpu_0_jtag_debug_module_begintransfer;
  wire    [  3: 0] cpu_0_jtag_debug_module_byteenable;
  wire              cpu_0_jtag_debug_module_chipselect;
  wire    [  3: 0] cpu_0_jtag_debug_module_chosen_master_double_vector;
  wire    [  1: 0] cpu_0_jtag_debug_module_chosen_master_rot_left;
  wire              cpu_0_jtag_debug_module_debugaccess;
  wire              cpu_0_jtag_debug_module_end_xfer;
  wire              cpu_0_jtag_debug_module_firsttransfer;
  wire    [  1: 0] cpu_0_jtag_debug_module_grant_vector;
  wire              cpu_0_jtag_debug_module_in_a_read_cycle;
  wire              cpu_0_jtag_debug_module_in_a_write_cycle;
  wire    [  1: 0] cpu_0_jtag_debug_module_master_qreq_vector;
  wire              cpu_0_jtag_debug_module_non_bursting_master_requests;
  wire    [ 31: 0] cpu_0_jtag_debug_module_readdata_from_sa;
  reg               cpu_0_jtag_debug_module_reg_firsttransfer;
  wire              cpu_0_jtag_debug_module_reset_n;
  wire              cpu_0_jtag_debug_module_resetrequest_from_sa;
  reg     [  1: 0] cpu_0_jtag_debug_module_saved_chosen_master_vector;
  reg               cpu_0_jtag_debug_module_slavearbiterlockenable;
  wire              cpu_0_jtag_debug_module_slavearbiterlockenable2;
  wire              cpu_0_jtag_debug_module_unreg_firsttransfer;
  wire              cpu_0_jtag_debug_module_waits_for_read;
  wire              cpu_0_jtag_debug_module_waits_for_write;
  wire              cpu_0_jtag_debug_module_write;
  wire    [ 31: 0] cpu_0_jtag_debug_module_writedata;
  reg               d1_cpu_0_jtag_debug_module_end_xfer;
  reg               d1_reasons_to_wait;
```

```
  reg             enable_nonzero_assertions;
  wire            end_xfer_arb_share_counter_term_cpu_0_jtag_debug_module;
  wire            in_a_read_cycle;
  wire            in_a_write_cycle;
  reg
last_cycle_cpu_0_data_master_granted_slave_cpu_0_jtag_debug_module;
  reg
last_cycle_cpu_0_instruction_master_granted_slave_cpu_0_jtag_debug_module;
  wire      [ 24: 0] shifted_address_to_cpu_0_jtag_debug_module_from_cpu_0_data_master;
  wire                                                    [ 24: 0]
shifted_address_to_cpu_0_jtag_debug_module_from_cpu_0_instruction_master;
  wire            wait_for_cpu_0_jtag_debug_module_counter;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_reasons_to_wait <= 0;
      else
        d1_reasons_to_wait <= ~cpu_0_jtag_debug_module_end_xfer;
    end


  assign      cpu_0_jtag_debug_module_begins_xfer      =      ~d1_reasons_to_wait      &
((cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module                          |
cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module));
  //assign                  cpu_0_jtag_debug_module_readdata_from_sa                  =
cpu_0_jtag_debug_module_readdata so that symbol knows where to group signals which may
go to master only, which is an e_assign
  assign cpu_0_jtag_debug_module_readdata_from_sa = cpu_0_jtag_debug_module_readdata;

  assign            cpu_0_data_master_requests_cpu_0_jtag_debug_module            =
({cpu_0_data_master_address_to_slave[24    :    11]    ,    11'b0}    ==    25'h1000800)    &
(cpu_0_data_master_read | cpu_0_data_master_write);
  //cpu_0_jtag_debug_module_arb_share_counter set values, which is an e_mux
  assign cpu_0_jtag_debug_module_arb_share_set_values = 1;

  //cpu_0_jtag_debug_module_non_bursting_master_requests mux, which is an e_mux
  assign            cpu_0_jtag_debug_module_non_bursting_master_requests            =
cpu_0_data_master_requests_cpu_0_jtag_debug_module |
    cpu_0_instruction_master_requests_cpu_0_jtag_debug_module |
    cpu_0_data_master_requests_cpu_0_jtag_debug_module |
    cpu_0_instruction_master_requests_cpu_0_jtag_debug_module;

  //cpu_0_jtag_debug_module_any_bursting_master_saved_grant mux, which is an e_mux
  assign cpu_0_jtag_debug_module_any_bursting_master_saved_grant = 0;

  //cpu_0_jtag_debug_module_arb_share_counter_next_value    assignment,    which    is    an
e_assign
  assign            cpu_0_jtag_debug_module_arb_share_counter_next_value            =
cpu_0_jtag_debug_module_firsttransfer  ?  (cpu_0_jtag_debug_module_arb_share_set_values  -
1)              :              |cpu_0_jtag_debug_module_arb_share_counter              ?
(cpu_0_jtag_debug_module_arb_share_counter - 1) : 0;

  //cpu_0_jtag_debug_module_allgrants all slave grants, which is an e_mux
  assign cpu_0_jtag_debug_module_allgrants = (|cpu_0_jtag_debug_module_grant_vector) |
    (|cpu_0_jtag_debug_module_grant_vector) |
    (|cpu_0_jtag_debug_module_grant_vector) |
    (|cpu_0_jtag_debug_module_grant_vector);
```

```
  //cpu_0_jtag_debug_module_end_xfer assignment, which is an e_assign
  assign cpu_0_jtag_debug_module_end_xfer = ~(cpu_0_jtag_debug_module_waits_for_read |
cpu_0_jtag_debug_module_waits_for_write);

  //end_xfer_arb_share_counter_term_cpu_0_jtag_debug_module arb share counter enable
term, which is an e_assign
  assign end_xfer_arb_share_counter_term_cpu_0_jtag_debug_module =
cpu_0_jtag_debug_module_end_xfer &
(~cpu_0_jtag_debug_module_any_bursting_master_saved_grant | in_a_read_cycle |
in_a_write_cycle);

  //cpu_0_jtag_debug_module_arb_share_counter arbitration counter enable, which is an
e_assign
  assign cpu_0_jtag_debug_module_arb_counter_enable =
(end_xfer_arb_share_counter_term_cpu_0_jtag_debug_module &
cpu_0_jtag_debug_module_allgrants) |
(end_xfer_arb_share_counter_term_cpu_0_jtag_debug_module &
~cpu_0_jtag_debug_module_non_bursting_master_requests);

  //cpu_0_jtag_debug_module_arb_share_counter counter, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          cpu_0_jtag_debug_module_arb_share_counter <= 0;
      else if (cpu_0_jtag_debug_module_arb_counter_enable)
          cpu_0_jtag_debug_module_arb_share_counter <=
cpu_0_jtag_debug_module_arb_share_counter_next_value;
    end


  //cpu_0_jtag_debug_module_slavearbiterlockenable slave enables arbiterlock, which is an
e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          cpu_0_jtag_debug_module_slavearbiterlockenable <= 0;
      else if (({|cpu_0_jtag_debug_module_master_qreq_vector &
end_xfer_arb_share_counter_term_cpu_0_jtag_debug_module) |
(end_xfer_arb_share_counter_term_cpu_0_jtag_debug_module &
~cpu_0_jtag_debug_module_non_bursting_master_requests))
          cpu_0_jtag_debug_module_slavearbiterlockenable <=
|cpu_0_jtag_debug_module_arb_share_counter_next_value;
    end


  //cpu_0/data_master cpu_0/jtag_debug_module arbiterlock, which is an e_assign
  assign cpu_0_data_master_arbiterlock = cpu_0_jtag_debug_module_slavearbiterlockenable &
cpu_0_data_master_continuerequest;

  //cpu_0_jtag_debug_module_slavearbiterlockenable2 slave enables arbiterlock2, which is an
e_assign
  assign cpu_0_jtag_debug_module_slavearbiterlockenable2 =
|cpu_0_jtag_debug_module_arb_share_counter_next_value;

  //cpu_0/data_master cpu_0/jtag_debug_module arbiterlock2, which is an e_assign
  assign cpu_0_data_master_arbiterlock2 =
cpu_0_jtag_debug_module_slavearbiterlockenable2 & cpu_0_data_master_continuerequest;
```

```
  //cpu_0/instruction_master cpu_0/jtag_debug_module arbiterlock, which is an e_assign
  assign cpu_0_instruction_master_arbiterlock = cpu_0_jtag_debug_module_slavearbiterlockenable & cpu_0_instruction_master_continuerequest;

  //cpu_0/instruction_master cpu_0/jtag_debug_module arbiterlock2, which is an e_assign
  assign cpu_0_instruction_master_arbiterlock2 = cpu_0_jtag_debug_module_slavearbiterlockenable2 & cpu_0_instruction_master_continuerequest;

  //cpu_0/instruction_master granted cpu_0/jtag_debug_module last time, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          last_cycle_cpu_0_instruction_master_granted_slave_cpu_0_jtag_debug_module <= 0;
      else
        last_cycle_cpu_0_instruction_master_granted_slave_cpu_0_jtag_debug_module <= cpu_0_instruction_master_saved_grant_cpu_0_jtag_debug_module ? 1 : (cpu_0_jtag_debug_module_arbitration_holdoff_internal | ~cpu_0_instruction_master_requests_cpu_0_jtag_debug_module) ? 0 : last_cycle_cpu_0_instruction_master_granted_slave_cpu_0_jtag_debug_module;
    end


  //cpu_0_instruction_master_continuerequest continued request, which is an e_mux
  assign cpu_0_instruction_master_continuerequest = last_cycle_cpu_0_instruction_master_granted_slave_cpu_0_jtag_debug_module & cpu_0_instruction_master_requests_cpu_0_jtag_debug_module;

  //cpu_0_jtag_debug_module_any_continuerequest at least one master continues requesting, which is an e_mux
  assign cpu_0_jtag_debug_module_any_continuerequest = cpu_0_instruction_master_continuerequest |
    cpu_0_data_master_continuerequest;

  assign cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module = cpu_0_data_master_requests_cpu_0_jtag_debug_module & ~(((~cpu_0_data_master_waitrequest) & cpu_0_data_master_write) | cpu_0_instruction_master_arbiterlock);
  //cpu_0_jtag_debug_module_writedata mux, which is an e_mux
  assign cpu_0_jtag_debug_module_writedata = cpu_0_data_master_writedata;

  assign cpu_0_instruction_master_requests_cpu_0_jtag_debug_module = (({cpu_0_instruction_master_address_to_slave[24 : 11] , 11'b0} == 25'h1000800) & (cpu_0_instruction_master_read)) & cpu_0_instruction_master_read;
  //cpu_0/data_master granted cpu_0/jtag_debug_module last time, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          last_cycle_cpu_0_data_master_granted_slave_cpu_0_jtag_debug_module <= 0;
      else
        last_cycle_cpu_0_data_master_granted_slave_cpu_0_jtag_debug_module <= cpu_0_data_master_saved_grant_cpu_0_jtag_debug_module ? 1 : (cpu_0_jtag_debug_module_arbitration_holdoff_internal | ~cpu_0_data_master_requests_cpu_0_jtag_debug_module) ? 0 : last_cycle_cpu_0_data_master_granted_slave_cpu_0_jtag_debug_module;
```

```
    end


  //cpu_0_data_master_continuerequest continued request, which is an e_mux
  assign cpu_0_data_master_continuerequest =
last_cycle_cpu_0_data_master_granted_slave_cpu_0_jtag_debug_module &
cpu_0_data_master_requests_cpu_0_jtag_debug_module;

  assign cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module =
cpu_0_instruction_master_requests_cpu_0_jtag_debug_module &
~(cpu_0_data_master_arbiterlock);
  //allow new arb cycle for cpu_0/jtag_debug_module, which is an e_assign
  assign cpu_0_jtag_debug_module_allow_new_arb_cycle = ~cpu_0_data_master_arbiterlock &
~cpu_0_instruction_master_arbiterlock;

  //cpu_0/instruction_master assignment into master qualified-requests vector for
cpu_0/jtag_debug_module, which is an e_assign
  assign cpu_0_jtag_debug_module_master_qreq_vector[0] =
cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module;

  //cpu_0/instruction_master grant cpu_0/jtag_debug_module, which is an e_assign
  assign cpu_0_instruction_master_granted_cpu_0_jtag_debug_module =
cpu_0_jtag_debug_module_grant_vector[0];

  //cpu_0/instruction_master saved-grant cpu_0/jtag_debug_module, which is an e_assign
  assign cpu_0_instruction_master_saved_grant_cpu_0_jtag_debug_module =
cpu_0_jtag_debug_module_arb_winner[0] &&
cpu_0_instruction_master_requests_cpu_0_jtag_debug_module;

  //cpu_0/data_master assignment into master qualified-requests vector for
cpu_0/jtag_debug_module, which is an e_assign
  assign cpu_0_jtag_debug_module_master_qreq_vector[1] =
cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module;

  //cpu_0/data_master grant cpu_0/jtag_debug_module, which is an e_assign
  assign cpu_0_data_master_granted_cpu_0_jtag_debug_module =
cpu_0_jtag_debug_module_grant_vector[1];

  //cpu_0/data_master saved-grant cpu_0/jtag_debug_module, which is an e_assign
  assign cpu_0_data_master_saved_grant_cpu_0_jtag_debug_module =
cpu_0_jtag_debug_module_arb_winner[1] &&
cpu_0_data_master_requests_cpu_0_jtag_debug_module;

  //cpu_0/jtag_debug_module chosen-master double-vector, which is an e_assign
  assign cpu_0_jtag_debug_module_chosen_master_double_vector =
{cpu_0_jtag_debug_module_master_qreq_vector,
cpu_0_jtag_debug_module_master_qreq_vector} &
({~cpu_0_jtag_debug_module_master_qreq_vector,
~cpu_0_jtag_debug_module_master_qreq_vector} + cpu_0_jtag_debug_module_arb_addend);

  //stable onehot encoding of arb winner
  assign cpu_0_jtag_debug_module_arb_winner =
(cpu_0_jtag_debug_module_allow_new_arb_cycle & |
cpu_0_jtag_debug_module_grant_vector) ? cpu_0_jtag_debug_module_grant_vector :
cpu_0_jtag_debug_module_saved_chosen_master_vector;

  //saved cpu_0_jtag_debug_module_grant_vector, which is an e_register
  always @(posedge clk or negedge reset_n)
```

```
    begin
      if (reset_n == 0)
          cpu_0_jtag_debug_module_saved_chosen_master_vector <= 0;
      else if (cpu_0_jtag_debug_module_allow_new_arb_cycle)
          cpu_0_jtag_debug_module_saved_chosen_master_vector <=
|cpu_0_jtag_debug_module_grant_vector ? cpu_0_jtag_debug_module_grant_vector :
cpu_0_jtag_debug_module_saved_chosen_master_vector;
    end


  //onehot encoding of chosen master
  assign cpu_0_jtag_debug_module_grant_vector =
{(cpu_0_jtag_debug_module_chosen_master_double_vector[1] |
cpu_0_jtag_debug_module_chosen_master_double_vector[3]),
    (cpu_0_jtag_debug_module_chosen_master_double_vector[0] |
cpu_0_jtag_debug_module_chosen_master_double_vector[2])};

  //cpu_0/jtag_debug_module chosen master rotated left, which is an e_assign
  assign cpu_0_jtag_debug_module_chosen_master_rot_left =
(cpu_0_jtag_debug_module_arb_winner << 1) ? (cpu_0_jtag_debug_module_arb_winner << 1) :
1;

  //cpu_0/jtag_debug_module's addend for next-master-grant
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          cpu_0_jtag_debug_module_arb_addend <= 1;
      else if (|cpu_0_jtag_debug_module_grant_vector)
          cpu_0_jtag_debug_module_arb_addend <= cpu_0_jtag_debug_module_end_xfer?
cpu_0_jtag_debug_module_chosen_master_rot_left : cpu_0_jtag_debug_module_grant_vector;
    end


  assign cpu_0_jtag_debug_module_begintransfer = cpu_0_jtag_debug_module_begins_xfer;
  //cpu_0_jtag_debug_module_reset_n assignment, which is an e_assign
  assign cpu_0_jtag_debug_module_reset_n = reset_n;

  //assign cpu_0_jtag_debug_module_resetrequest_from_sa =
cpu_0_jtag_debug_module_resetrequest so that symbol knows where to group signals which
may go to master only, which is an e_assign
  assign cpu_0_jtag_debug_module_resetrequest_from_sa =
cpu_0_jtag_debug_module_resetrequest;

  assign cpu_0_jtag_debug_module_chipselect =
cpu_0_data_master_granted_cpu_0_jtag_debug_module |
cpu_0_instruction_master_granted_cpu_0_jtag_debug_module;
  //cpu_0_jtag_debug_module_firsttransfer first transaction, which is an e_assign
  assign cpu_0_jtag_debug_module_firsttransfer = cpu_0_jtag_debug_module_begins_xfer ?
cpu_0_jtag_debug_module_unreg_firsttransfer : cpu_0_jtag_debug_module_reg_firsttransfer;

  //cpu_0_jtag_debug_module_unreg_firsttransfer first transaction, which is an e_assign
  assign cpu_0_jtag_debug_module_unreg_firsttransfer =
~(cpu_0_jtag_debug_module_slavearbiterlockenable &
cpu_0_jtag_debug_module_any_continuerequest);

  //cpu_0_jtag_debug_module_reg_firsttransfer first transaction, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
```

```
        if (reset_n == 0)
            cpu_0_jtag_debug_module_reg_firsttransfer <= 1'b1;
        else if (cpu_0_jtag_debug_module_begins_xfer)
            cpu_0_jtag_debug_module_reg_firsttransfer <=
cpu_0_jtag_debug_module_unreg_firsttransfer;
      end


  //cpu_0_jtag_debug_module_beginbursttransfer_internal begin burst transfer, which is an
e_assign
  assign cpu_0_jtag_debug_module_beginbursttransfer_internal =
cpu_0_jtag_debug_module_begins_xfer;

  //cpu_0_jtag_debug_module_arbitration_holdoff_internal arbitration_holdoff, which is an
e_assign
  assign cpu_0_jtag_debug_module_arbitration_holdoff_internal =
cpu_0_jtag_debug_module_begins_xfer & cpu_0_jtag_debug_module_firsttransfer;

  //cpu_0_jtag_debug_module_write assignment, which is an e_mux
  assign cpu_0_jtag_debug_module_write =
cpu_0_data_master_granted_cpu_0_jtag_debug_module & cpu_0_data_master_write;

  assign shifted_address_to_cpu_0_jtag_debug_module_from_cpu_0_data_master =
cpu_0_data_master_address_to_slave;
  //cpu_0_jtag_debug_module_address mux, which is an e_mux
  assign cpu_0_jtag_debug_module_address =
(cpu_0_data_master_granted_cpu_0_jtag_debug_module)?
(shifted_address_to_cpu_0_jtag_debug_module_from_cpu_0_data_master >> 2) :
    (shifted_address_to_cpu_0_jtag_debug_module_from_cpu_0_instruction_master >> 2);

  assign shifted_address_to_cpu_0_jtag_debug_module_from_cpu_0_instruction_master =
cpu_0_instruction_master_address_to_slave;
  //d1_cpu_0_jtag_debug_module_end_xfer register, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_cpu_0_jtag_debug_module_end_xfer <= 1;
      else
        d1_cpu_0_jtag_debug_module_end_xfer <= cpu_0_jtag_debug_module_end_xfer;
    end


  //cpu_0_jtag_debug_module_waits_for_read in a cycle, which is an e_mux
  assign cpu_0_jtag_debug_module_waits_for_read =
cpu_0_jtag_debug_module_in_a_read_cycle & cpu_0_jtag_debug_module_begins_xfer;

  //cpu_0_jtag_debug_module_in_a_read_cycle assignment, which is an e_assign
  assign cpu_0_jtag_debug_module_in_a_read_cycle =
(cpu_0_data_master_granted_cpu_0_jtag_debug_module & cpu_0_data_master_read) |
(cpu_0_instruction_master_granted_cpu_0_jtag_debug_module &
cpu_0_instruction_master_read);

  //in_a_read_cycle assignment, which is an e_mux
  assign in_a_read_cycle = cpu_0_jtag_debug_module_in_a_read_cycle;

  //cpu_0_jtag_debug_module_waits_for_write in a cycle, which is an e_mux
  assign cpu_0_jtag_debug_module_waits_for_write =
cpu_0_jtag_debug_module_in_a_write_cycle & 0;
```

```
  //cpu_0_jtag_debug_module_in_a_write_cycle assignment, which is an e_assign
  assign cpu_0_jtag_debug_module_in_a_write_cycle =
cpu_0_data_master_granted_cpu_0_jtag_debug_module & cpu_0_data_master_write;

  //in_a_write_cycle assignment, which is an e_mux
  assign in_a_write_cycle = cpu_0_jtag_debug_module_in_a_write_cycle;

  assign wait_for_cpu_0_jtag_debug_module_counter = 0;
  //cpu_0_jtag_debug_module_byteenable byte enable port mux, which is an e_mux
  assign cpu_0_jtag_debug_module_byteenable =
(cpu_0_data_master_granted_cpu_0_jtag_debug_module)? cpu_0_data_master_byteenable :
    -1;

  //debugaccess mux, which is an e_mux
  assign cpu_0_jtag_debug_module_debugaccess =
(cpu_0_data_master_granted_cpu_0_jtag_debug_module)? cpu_0_data_master_debugaccess :
    0;


//synthesis translate_off
//////////////// SIMULATION-ONLY CONTENTS
  //cpu_0/jtag_debug_module enable non-zero assertions, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          enable_nonzero_assertions <= 0;
      else
        enable_nonzero_assertions <= 1'b1;
    end


  //grant signals are active simultaneously, which is an e_process
  always @(posedge clk)
    begin
      if (cpu_0_data_master_granted_cpu_0_jtag_debug_module +
cpu_0_instruction_master_granted_cpu_0_jtag_debug_module > 1)
        begin
          $write("%0d ns: > 1 of grant signals are active simultaneously", $time);
          $stop;
        end
    end


  //saved_grant signals are active simultaneously, which is an e_process
  always @(posedge clk)
    begin
      if (cpu_0_data_master_saved_grant_cpu_0_jtag_debug_module +
cpu_0_instruction_master_saved_grant_cpu_0_jtag_debug_module > 1)
        begin
          $write("%0d ns: > 1 of saved_grant signals are active simultaneously", $time);
          $stop;
        end
    end


//////////////// END SIMULATION-ONLY CONTENTS
```

```
//synthesis translate_on

endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_data_master_arbitrator (
                                      // inputs:

audio_controller_0_avalon_slave_0_readdata_from_sa,
                                      clk,

command_0_avalon_slave_0_readdata_from_sa,
                                      cpu_0_data_master_address,

cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0,

cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0,
                                      cpu_0_data_master_byteenable_sdram_0_s1,

cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0,

cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0,

cpu_0_data_master_granted_audio_controller_0_avalon_slave_0,

cpu_0_data_master_granted_command_0_avalon_slave_0,

cpu_0_data_master_granted_cpu_0_jtag_debug_module,

cpu_0_data_master_granted_interrupt_0_avalon_slave_0,

cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave,

cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0,
                                      cpu_0_data_master_granted_sdram_0_s1,

cpu_0_data_master_granted_sram_mux_0_avalon_slave_0,

cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0,

cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0,

cpu_0_data_master_qualified_request_command_0_avalon_slave_0,

cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module,

cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0,

cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave,
```

```
cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0,

cpu_0_data_master_qualified_request_sdram_0_s1,

cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0,

cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0,
                                                cpu_0_data_master_read,

cpu_0_data_master_read_data_valid_audio_controller_0_avalon_slave_0,

cpu_0_data_master_read_data_valid_command_0_avalon_slave_0,

cpu_0_data_master_read_data_valid_cpu_0_jtag_debug_module,

cpu_0_data_master_read_data_valid_interrupt_0_avalon_slave_0,

cpu_0_data_master_read_data_valid_jtag_uart_0_avalon_jtag_slave,

cpu_0_data_master_read_data_valid_musiccontroller_0_avalon_slave_0,

cpu_0_data_master_read_data_valid_sdram_0_s1,

cpu_0_data_master_read_data_valid_sdram_0_s1_shift_register,

cpu_0_data_master_read_data_valid_sram_mux_0_avalon_slave_0,

cpu_0_data_master_read_data_valid_xycoord_interface_0_avalon_slave_0,

cpu_0_data_master_requests_audio_controller_0_avalon_slave_0,

cpu_0_data_master_requests_command_0_avalon_slave_0,

cpu_0_data_master_requests_cpu_0_jtag_debug_module,

cpu_0_data_master_requests_interrupt_0_avalon_slave_0,

cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave,

cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0,
                                                cpu_0_data_master_requests_sdram_0_s1,

cpu_0_data_master_requests_sram_mux_0_avalon_slave_0,

cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0,
                                                cpu_0_data_master_write,
                                                cpu_0_data_master_writedata,
                                                cpu_0_jtag_debug_module_readdata_from_sa,

d1_audio_controller_0_avalon_slave_0_end_xfer,
                                                d1_command_0_avalon_slave_0_end_xfer,
                                                d1_cpu_0_jtag_debug_module_end_xfer,
                                                d1_interrupt_0_avalon_slave_0_end_xfer,
                                                d1_jtag_uart_0_avalon_jtag_slave_end_xfer,
                                                d1_musiccontroller_0_avalon_slave_0_end_xfer,
                                                d1_sdram_0_s1_end_xfer,
                                                d1_sram_mux_0_avalon_slave_0_end_xfer,
```

```
d1_xycoord_interface_0_avalon_slave_0_end_xfer,
                                                    interrupt_0_avalon_slave_0_irq_from_sa,
                                                    interrupt_0_avalon_slave_0_readdata_from_sa,
                                                    jtag_uart_0_avalon_jtag_slave_irq_from_sa,

jtag_uart_0_avalon_jtag_slave_readdata_from_sa,

jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa,
                                                    musiccontroller_0_avalon_slave_0_irq_from_sa,

musiccontroller_0_avalon_slave_0_readdata_from_sa,
                                                    reset_n,
                                                    sdram_0_s1_readdata_from_sa,
                                                    sdram_0_s1_waitrequest_from_sa,

sram_mux_0_avalon_slave_0_readdata_from_sa,

xycoord_interface_0_avalon_slave_0_readdata_from_sa,

                                                   // outputs:
                                                    cpu_0_data_master_address_to_slave,
                                                    cpu_0_data_master_dbs_address,
                                                    cpu_0_data_master_dbs_write_16,
                                                    cpu_0_data_master_irq,

cpu_0_data_master_no_byte_enables_and_last_term,
                                                    cpu_0_data_master_readdata,
                                                    cpu_0_data_master_waitrequest
                                                 )
;

  output  [ 24: 0] cpu_0_data_master_address_to_slave;
  output  [  1: 0] cpu_0_data_master_dbs_address;
  output  [ 15: 0] cpu_0_data_master_dbs_write_16;
  output  [ 31: 0] cpu_0_data_master_irq;
  output           cpu_0_data_master_no_byte_enables_and_last_term;
  output  [ 31: 0] cpu_0_data_master_readdata;
  output           cpu_0_data_master_waitrequest;
  input   [ 15: 0] audio_controller_0_avalon_slave_0_readdata_from_sa;
  input            clk;
  input   [ 31: 0] command_0_avalon_slave_0_readdata_from_sa;
  input   [ 24: 0] cpu_0_data_master_address;
  input   [  1: 0] cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0;
  input   [  1: 0] cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0;
  input   [  1: 0] cpu_0_data_master_byteenable_sdram_0_s1;
  input   [  1: 0] cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0;
  input   [  1: 0] cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0;
  input            cpu_0_data_master_granted_audio_controller_0_avalon_slave_0;
  input            cpu_0_data_master_granted_command_0_avalon_slave_0;
  input            cpu_0_data_master_granted_cpu_0_jtag_debug_module;
  input            cpu_0_data_master_granted_interrupt_0_avalon_slave_0;
  input            cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave;
  input            cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0;
  input            cpu_0_data_master_granted_sdram_0_s1;
  input            cpu_0_data_master_granted_sram_mux_0_avalon_slave_0;
  input            cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0;
  input
```

```
cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0;
  input              cpu_0_data_master_qualified_request_command_0_avalon_slave_0;
  input              cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module;
  input              cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0;
  input              cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave;
  input
cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0;
  input              cpu_0_data_master_qualified_request_sdram_0_s1;
  input              cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0;
  input
cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0;
  input              cpu_0_data_master_read;
  input
cpu_0_data_master_read_data_valid_audio_controller_0_avalon_slave_0;
  input              cpu_0_data_master_read_data_valid_command_0_avalon_slave_0;
  input              cpu_0_data_master_read_data_valid_cpu_0_jtag_debug_module;
  input              cpu_0_data_master_read_data_valid_interrupt_0_avalon_slave_0;
  input              cpu_0_data_master_read_data_valid_jtag_uart_0_avalon_jtag_slave;
  input              cpu_0_data_master_read_data_valid_musiccontroller_0_avalon_slave_0;
  input              cpu_0_data_master_read_data_valid_sdram_0_s1;
  input              cpu_0_data_master_read_data_valid_sdram_0_s1_shift_register;
  input              cpu_0_data_master_read_data_valid_sram_mux_0_avalon_slave_0;
  input
cpu_0_data_master_read_data_valid_xycoord_interface_0_avalon_slave_0;
  input              cpu_0_data_master_requests_audio_controller_0_avalon_slave_0;
  input              cpu_0_data_master_requests_command_0_avalon_slave_0;
  input              cpu_0_data_master_requests_cpu_0_jtag_debug_module;
  input              cpu_0_data_master_requests_interrupt_0_avalon_slave_0;
  input              cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave;
  input              cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0;
  input              cpu_0_data_master_requests_sdram_0_s1;
  input              cpu_0_data_master_requests_sram_mux_0_avalon_slave_0;
  input              cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0;
  input              cpu_0_data_master_write;
  input   [ 31: 0] cpu_0_data_master_writedata;
  input   [ 31: 0] cpu_0_jtag_debug_module_readdata_from_sa;
  input              d1_audio_controller_0_avalon_slave_0_end_xfer;
  input              d1_command_0_avalon_slave_0_end_xfer;
  input              d1_cpu_0_jtag_debug_module_end_xfer;
  input              d1_interrupt_0_avalon_slave_0_end_xfer;
  input              d1_jtag_uart_0_avalon_jtag_slave_end_xfer;
  input              d1_musiccontroller_0_avalon_slave_0_end_xfer;
  input              d1_sdram_0_s1_end_xfer;
  input              d1_sram_mux_0_avalon_slave_0_end_xfer;
  input              d1_xycoord_interface_0_avalon_slave_0_end_xfer;
  input              interrupt_0_avalon_slave_0_irq_from_sa;
  input   [ 31: 0] interrupt_0_avalon_slave_0_readdata_from_sa;
  input              jtag_uart_0_avalon_jtag_slave_irq_from_sa;
  input   [ 31: 0] jtag_uart_0_avalon_jtag_slave_readdata_from_sa;
  input              jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa;
  input              musiccontroller_0_avalon_slave_0_irq_from_sa;
  input   [ 15: 0] musiccontroller_0_avalon_slave_0_readdata_from_sa;
  input              reset_n;
  input   [ 15: 0] sdram_0_s1_readdata_from_sa;
  input              sdram_0_s1_waitrequest_from_sa;
  input   [ 15: 0] sram_mux_0_avalon_slave_0_readdata_from_sa;
  input   [ 15: 0] xycoord_interface_0_avalon_slave_0_readdata_from_sa;
```

```
  wire  [ 24: 0] cpu_0_data_master_address_to_slave;
  reg   [  1: 0] cpu_0_data_master_dbs_address;
  wire  [  1: 0] cpu_0_data_master_dbs_increment;
  wire  [ 15: 0] cpu_0_data_master_dbs_write_16;
  wire  [ 31: 0] cpu_0_data_master_irq;
  reg            cpu_0_data_master_no_byte_enables_and_last_term;
  wire  [ 31: 0] cpu_0_data_master_readdata;
  wire           cpu_0_data_master_run;
  reg            cpu_0_data_master_waitrequest;
  reg   [ 15: 0] dbs_16_reg_segment_0;
  wire           dbs_count_enable;
  wire           dbs_counter_overflow;
  wire           last_dbs_term_and_run;
  wire  [  1: 0] next_dbs_address;
  wire  [ 15: 0] p1_dbs_16_reg_segment_0;
  wire  [ 31: 0] p1_registered_cpu_0_data_master_readdata;
  wire           pre_dbs_count_enable;
  wire           r_0;
  wire           r_1;
  wire           r_2;
  reg   [ 31: 0] registered_cpu_0_data_master_readdata;
  //r_0 master_run cascaded wait assignment, which is an e_assign
  assign r_0 = 1 & (cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0 |
(cpu_0_data_master_write
& !cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0 &
cpu_0_data_master_dbs_address[1]) |
~cpu_0_data_master_requests_audio_controller_0_avalon_slave_0) &
(cpu_0_data_master_granted_audio_controller_0_avalon_slave_0 |
~cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0) &
((~cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0 |
~cpu_0_data_master_read | (1 & 1 & (cpu_0_data_master_dbs_address[1]) &
cpu_0_data_master_read))) &
((~cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0 |
~cpu_0_data_master_write | (1 & (cpu_0_data_master_dbs_address[1]) &
cpu_0_data_master_write))) & 1 &
(cpu_0_data_master_qualified_request_command_0_avalon_slave_0 |
~cpu_0_data_master_requests_command_0_avalon_slave_0) &
(cpu_0_data_master_granted_command_0_avalon_slave_0 |
~cpu_0_data_master_qualified_request_command_0_avalon_slave_0) &
((~cpu_0_data_master_qualified_request_command_0_avalon_slave_0 |
~cpu_0_data_master_read | (1 & 1 & cpu_0_data_master_read))) &
((~cpu_0_data_master_qualified_request_command_0_avalon_slave_0 |
~cpu_0_data_master_write | (1 & cpu_0_data_master_write))) & 1 &
(cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module |
~cpu_0_data_master_requests_cpu_0_jtag_debug_module) &
(cpu_0_data_master_granted_cpu_0_jtag_debug_module |
~cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module) &
((~cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module |
~cpu_0_data_master_read | (1 & 1 & cpu_0_data_master_read))) &
((~cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module |
~cpu_0_data_master_write | (1 & cpu_0_data_master_write))) & 1 &
(cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0 |
~cpu_0_data_master_requests_interrupt_0_avalon_slave_0) &
((~cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0 |
~cpu_0_data_master_read | (1 & 1 & cpu_0_data_master_read))) &
((~cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0 |
~cpu_0_data_master_write | (1 & cpu_0_data_master_write))) & 1;
```

```
  //cascaded wait assignment, which is an e_assign
  assign cpu_0_data_master_run = r_0 & r_1 & r_2;

  //r_1 master_run cascaded wait assignment, which is an e_assign
  assign r_1 = (cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave |
~cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave) &
((~cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave |
~(cpu_0_data_master_read | cpu_0_data_master_write) | (1 &
~jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa & (cpu_0_data_master_read |
cpu_0_data_master_write)))) &
((~cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave |
~(cpu_0_data_master_read | cpu_0_data_master_write) | (1 &
~jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa & (cpu_0_data_master_read |
cpu_0_data_master_write)))) & 1 &
(cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0 |
(cpu_0_data_master_write
& !cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0 &
cpu_0_data_master_dbs_address[1]) |
~cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0) &
((~cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0 |
~cpu_0_data_master_read | (1 & 1 & (cpu_0_data_master_dbs_address[1]) &
cpu_0_data_master_read))) &
((~cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0 |
~cpu_0_data_master_write | (1 & (cpu_0_data_master_dbs_address[1]) &
cpu_0_data_master_write))) & 1 & (cpu_0_data_master_qualified_request_sdram_0_s1 |
(cpu_0_data_master_read_data_valid_sdram_0_s1 & cpu_0_data_master_dbs_address[1]) |
(cpu_0_data_master_write & !cpu_0_data_master_byteenable_sdram_0_s1 &
cpu_0_data_master_dbs_address[1]) | ~cpu_0_data_master_requests_sdram_0_s1) &
(cpu_0_data_master_granted_sdram_0_s1 |
~cpu_0_data_master_qualified_request_sdram_0_s1) &
((~cpu_0_data_master_qualified_request_sdram_0_s1 | ~cpu_0_data_master_read |
(cpu_0_data_master_read_data_valid_sdram_0_s1 & (cpu_0_data_master_dbs_address[1]) &
cpu_0_data_master_read))) & ((~cpu_0_data_master_qualified_request_sdram_0_s1 |
~cpu_0_data_master_write | (1 & ~sdram_0_s1_waitrequest_from_sa &
(cpu_0_data_master_dbs_address[1]) & cpu_0_data_master_write))) & 1 &
(cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0 |
(cpu_0_data_master_write & !cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0 &
cpu_0_data_master_dbs_address[1]) |
~cpu_0_data_master_requests_sram_mux_0_avalon_slave_0) &
(cpu_0_data_master_granted_sram_mux_0_avalon_slave_0 |
~cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0) &
((~cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0 |
~cpu_0_data_master_read | (1 & 1 & (cpu_0_data_master_dbs_address[1]) &
cpu_0_data_master_read))) &
((~cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0 |
~cpu_0_data_master_write | (1 & (cpu_0_data_master_dbs_address[1]) &
cpu_0_data_master_write))) & 1 &
(cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0 |
(cpu_0_data_master_write
& !cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0 &
cpu_0_data_master_dbs_address[1]) |
~cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0) &
(cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0 |
~cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0);

  //r_2 master_run cascaded wait assignment, which is an e_assign
  assign r_2 = ((~cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0 |
~cpu_0_data_master_read | (1 & 1 & (cpu_0_data_master_dbs_address[1]) &
```

```
cpu_0_data_master_read))) &
((~cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0 |
~cpu_0_data_master_write | (1 & (cpu_0_data_master_dbs_address[1]) &
cpu_0_data_master_write)));

  //optimize select-logic by passing only those address bits which matter.
  assign cpu_0_data_master_address_to_slave = cpu_0_data_master_address[24 : 0];

  //no_byte_enables_and_last_term, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          cpu_0_data_master_no_byte_enables_and_last_term <= 0;
      else
        cpu_0_data_master_no_byte_enables_and_last_term <= last_dbs_term_and_run;
    end


  //compute the last dbs term, which is an e_mux
  assign last_dbs_term_and_run =
(cpu_0_data_master_requests_audio_controller_0_avalon_slave_0)?
(((cpu_0_data_master_dbs_address == 2'b10) & cpu_0_data_master_write
& !cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0)) :
    (cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0)?
(((cpu_0_data_master_dbs_address == 2'b10) & cpu_0_data_master_write
& !cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0)) :
    (cpu_0_data_master_requests_sdram_0_s1)? (((cpu_0_data_master_dbs_address == 2'b10)
& cpu_0_data_master_write & !cpu_0_data_master_byteenable_sdram_0_s1)) :
    (cpu_0_data_master_requests_sram_mux_0_avalon_slave_0)?
(((cpu_0_data_master_dbs_address == 2'b10) & cpu_0_data_master_write
& !cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0)) :
    (((cpu_0_data_master_dbs_address == 2'b10) & cpu_0_data_master_write
& !cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0));

  //pre dbs count enable, which is an e_mux
  assign pre_dbs_count_enable = (((~cpu_0_data_master_no_byte_enables_and_last_term) &
cpu_0_data_master_requests_audio_controller_0_avalon_slave_0 & cpu_0_data_master_write
& !cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0)) |
    (cpu_0_data_master_granted_audio_controller_0_avalon_slave_0 &
cpu_0_data_master_read & 1 & 1 & ~d1_audio_controller_0_avalon_slave_0_end_xfer) |
    (cpu_0_data_master_granted_audio_controller_0_avalon_slave_0 &
cpu_0_data_master_write & 1 & 1) |
    (((~cpu_0_data_master_no_byte_enables_and_last_term) &
cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0 & cpu_0_data_master_write
& !cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0)) |
    (cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0 &
cpu_0_data_master_read & 1 & 1 & ~d1_musiccontroller_0_avalon_slave_0_end_xfer) |
    (cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0 &
cpu_0_data_master_write & 1 & 1) |
    (((~cpu_0_data_master_no_byte_enables_and_last_term) &
cpu_0_data_master_requests_sdram_0_s1 & cpu_0_data_master_write
& !cpu_0_data_master_byteenable_sdram_0_s1)) |
    cpu_0_data_master_read_data_valid_sdram_0_s1 |
    (cpu_0_data_master_granted_sdram_0_s1 & cpu_0_data_master_write & 1 & 1 &
~sdram_0_s1_waitrequest_from_sa) |
    (((~cpu_0_data_master_no_byte_enables_and_last_term) &
cpu_0_data_master_requests_sram_mux_0_avalon_slave_0 & cpu_0_data_master_write
& !cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0)) |
```

```
      (cpu_0_data_master_granted_sram_mux_0_avalon_slave_0 & cpu_0_data_master_read &
1 & 1 & ~d1_sram_mux_0_avalon_slave_0_end_xfer) |
      (cpu_0_data_master_granted_sram_mux_0_avalon_slave_0 & cpu_0_data_master_write &
1 & 1) |
      (((~cpu_0_data_master_no_byte_enables_and_last_term)                    &
cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0                  &
cpu_0_data_master_write
& !cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0)) |
      (cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0              &
cpu_0_data_master_read & 1 & 1 & ~d1_xycoord_interface_0_avalon_slave_0_end_xfer) |
      (cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0              &
cpu_0_data_master_write & 1 & 1);

   //input to dbs-16 stored 0, which is an e_mux
   assign                                  p1_dbs_16_reg_segment_0                =
(cpu_0_data_master_requests_audio_controller_0_avalon_slave_0)?
audio_controller_0_avalon_slave_0_readdata_from_sa :
      (cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0)?
musiccontroller_0_avalon_slave_0_readdata_from_sa :
      (cpu_0_data_master_requests_sdram_0_s1)? sdram_0_s1_readdata_from_sa :
      (cpu_0_data_master_requests_sram_mux_0_avalon_slave_0)?
sram_mux_0_avalon_slave_0_readdata_from_sa :
      xycoord_interface_0_avalon_slave_0_readdata_from_sa;

   //dbs register for dbs-16 segment 0, which is an e_register
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               dbs_16_reg_segment_0 <= 0;
         else if (dbs_count_enable & ((cpu_0_data_master_dbs_address[1]) == 0))
               dbs_16_reg_segment_0 <= p1_dbs_16_reg_segment_0;
      end


   //cpu_0/data_master readdata mux, which is an e_mux
   assign                      cpu_0_data_master_readdata                 =                ({32
{~cpu_0_data_master_requests_audio_controller_0_avalon_slave_0}}                          |
{audio_controller_0_avalon_slave_0_readdata_from_sa[15 : 0],
      dbs_16_reg_segment_0}) &
      ({32              {~cpu_0_data_master_requests_command_0_avalon_slave_0}}          |
command_0_avalon_slave_0_readdata_from_sa) &
      ({32               {~cpu_0_data_master_requests_cpu_0_jtag_debug_module}}          |
cpu_0_jtag_debug_module_readdata_from_sa) &
      ({32               {~cpu_0_data_master_requests_interrupt_0_avalon_slave_0}}       |
interrupt_0_avalon_slave_0_readdata_from_sa) &
      ({32             {~cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave}}      |
registered_cpu_0_data_master_readdata) &
      ({32           {~cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0}}     |
{musiccontroller_0_avalon_slave_0_readdata_from_sa[15 : 0],
      dbs_16_reg_segment_0}) &
      ({32                    {~cpu_0_data_master_requests_sdram_0_s1}}                  |
registered_cpu_0_data_master_readdata) &
      ({32               {~cpu_0_data_master_requests_sram_mux_0_avalon_slave_0}}       |
{sram_mux_0_avalon_slave_0_readdata_from_sa[15 : 0],
      dbs_16_reg_segment_0}) &
      ({32          {~cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0}}   |
{xycoord_interface_0_avalon_slave_0_readdata_from_sa[15 : 0],
      dbs_16_reg_segment_0});
```

```
  //mux write dbs 1, which is an e_mux
  assign cpu_0_data_master_dbs_write_16 = (cpu_0_data_master_dbs_address[1])?
cpu_0_data_master_writedata[31 : 16] :
    (~(cpu_0_data_master_dbs_address[1]))? cpu_0_data_master_writedata[15 : 0] :
    (cpu_0_data_master_dbs_address[1])? cpu_0_data_master_writedata[31 : 16] :
    (~(cpu_0_data_master_dbs_address[1]))? cpu_0_data_master_writedata[15 : 0] :
    (cpu_0_data_master_dbs_address[1])? cpu_0_data_master_writedata[31 : 16] :
    (~(cpu_0_data_master_dbs_address[1]))? cpu_0_data_master_writedata[15 : 0] :
    (cpu_0_data_master_dbs_address[1])? cpu_0_data_master_writedata[31 : 16] :
    (~(cpu_0_data_master_dbs_address[1]))? cpu_0_data_master_writedata[15 : 0] :
    (cpu_0_data_master_dbs_address[1])? cpu_0_data_master_writedata[31 : 16] :
    cpu_0_data_master_writedata[15 : 0];

  //actual waitrequest port, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          cpu_0_data_master_waitrequest <= ~0;
      else
        cpu_0_data_master_waitrequest <= ~((~(cpu_0_data_master_read |
cpu_0_data_master_write))? 0: (cpu_0_data_master_run & cpu_0_data_master_waitrequest));
    end


  //dbs count increment, which is an e_mux
  assign cpu_0_data_master_dbs_increment =
(cpu_0_data_master_requests_audio_controller_0_avalon_slave_0)? 2 :
    (cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0)? 2 :
    (cpu_0_data_master_requests_sdram_0_s1)? 2 :
    (cpu_0_data_master_requests_sram_mux_0_avalon_slave_0)? 2 :
    (cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0)? 2 :
    0;

  //dbs counter overflow, which is an e_assign
  assign dbs_counter_overflow = cpu_0_data_master_dbs_address[1]
& !(next_dbs_address[1]);

  //next master address, which is an e_assign
  assign next_dbs_address = cpu_0_data_master_dbs_address +
cpu_0_data_master_dbs_increment;

  //dbs count enable, which is an e_mux
  assign dbs_count_enable = pre_dbs_count_enable &
    (~(cpu_0_data_master_requests_audio_controller_0_avalon_slave_0 &
~cpu_0_data_master_waitrequest & cpu_0_data_master_write)) &
    (~(cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0 &
~cpu_0_data_master_waitrequest & cpu_0_data_master_write)) &
    (~(cpu_0_data_master_requests_sdram_0_s1 & ~cpu_0_data_master_waitrequest)) &
    (~(cpu_0_data_master_requests_sram_mux_0_avalon_slave_0 &
~cpu_0_data_master_waitrequest & cpu_0_data_master_write)) &
    (~(cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0 &
~cpu_0_data_master_waitrequest & cpu_0_data_master_write));

  //dbs counter, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
```

```
            cpu_0_data_master_dbs_address <= 0;
        else if (dbs_count_enable)
            cpu_0_data_master_dbs_address <= next_dbs_address;
    end


  //irq assign, which is an e_assign
  assign cpu_0_data_master_irq = {1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    1'b0,
    interrupt_0_avalon_slave_0_irq_from_sa,
    musiccontroller_0_avalon_slave_0_irq_from_sa,
    jtag_uart_0_avalon_jtag_slave_irq_from_sa};

  //unpredictable registered wait state incoming data, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          registered_cpu_0_data_master_readdata <= 0;
      else
        registered_cpu_0_data_master_readdata                                    <=
p1_registered_cpu_0_data_master_readdata;
    end


  //registered readdata mux, which is an e_mux
  assign                p1_registered_cpu_0_data_master_readdata              =              ({32
{~cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave}}                                  |
jtag_uart_0_avalon_jtag_slave_readdata_from_sa) &
    ({32 {~cpu_0_data_master_requests_sdram_0_s1}} | {sdram_0_s1_readdata_from_sa[15 :
0],
    dbs_16_reg_segment_0});
```

```
endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_instruction_master_arbitrator (
                                             // inputs:

audio_controller_0_avalon_slave_0_readdata_from_sa,
                                              clk,

command_0_avalon_slave_0_readdata_from_sa,
                                              cpu_0_instruction_master_address,

cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0,

cpu_0_instruction_master_granted_command_0_avalon_slave_0,

cpu_0_instruction_master_granted_cpu_0_jtag_debug_module,

cpu_0_instruction_master_granted_sdram_0_s1,

cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0,

cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0,

cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0,

cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0,

cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module,

cpu_0_instruction_master_qualified_request_sdram_0_s1,

cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0,

cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0,
                                              cpu_0_instruction_master_read,

cpu_0_instruction_master_read_data_valid_audio_controller_0_avalon_slave_0,

cpu_0_instruction_master_read_data_valid_command_0_avalon_slave_0,

cpu_0_instruction_master_read_data_valid_cpu_0_jtag_debug_module,

cpu_0_instruction_master_read_data_valid_sdram_0_s1,

cpu_0_instruction_master_read_data_valid_sdram_0_s1_shift_register,

cpu_0_instruction_master_read_data_valid_sram_mux_0_avalon_slave_0,
```

```
cpu_0_instruction_master_read_data_valid_xycoord_interface_0_avalon_slave_0,

cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0,

cpu_0_instruction_master_requests_command_0_avalon_slave_0,

cpu_0_instruction_master_requests_cpu_0_jtag_debug_module,

cpu_0_instruction_master_requests_sdram_0_s1,

cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0,

cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0,

cpu_0_jtag_debug_module_readdata_from_sa,

d1_audio_controller_0_avalon_slave_0_end_xfer,

d1_command_0_avalon_slave_0_end_xfer,

d1_cpu_0_jtag_debug_module_end_xfer,
                                                    d1_sdram_0_s1_end_xfer,

d1_sram_mux_0_avalon_slave_0_end_xfer,

d1_xycoord_interface_0_avalon_slave_0_end_xfer,
                                                    reset_n,
                                                    sdram_0_s1_readdata_from_sa,
                                                    sdram_0_s1_waitrequest_from_sa,

sram_mux_0_avalon_slave_0_readdata_from_sa,

xycoord_interface_0_avalon_slave_0_readdata_from_sa,

                                                  // outputs:

cpu_0_instruction_master_address_to_slave,

cpu_0_instruction_master_dbs_address,
                                                    cpu_0_instruction_master_readdata,
                                                    cpu_0_instruction_master_waitrequest
                                                )
;

  output  [ 24: 0] cpu_0_instruction_master_address_to_slave;
  output  [  1: 0] cpu_0_instruction_master_dbs_address;
  output  [ 31: 0] cpu_0_instruction_master_readdata;
  output           cpu_0_instruction_master_waitrequest;
  input   [ 15: 0] audio_controller_0_avalon_slave_0_readdata_from_sa;
  input            clk;
  input   [ 31: 0] command_0_avalon_slave_0_readdata_from_sa;
  input   [ 24: 0] cpu_0_instruction_master_address;
  input            cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0;
  input            cpu_0_instruction_master_granted_command_0_avalon_slave_0;
  input            cpu_0_instruction_master_granted_cpu_0_jtag_debug_module;
  input            cpu_0_instruction_master_granted_sdram_0_s1;
  input            cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0;
```

```
  input              cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0;
  input
cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0;
  input
cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0;
  input              cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module;
  input              cpu_0_instruction_master_qualified_request_sdram_0_s1;
  input
cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0;
  input
cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0;
  input              cpu_0_instruction_master_read;
  input
cpu_0_instruction_master_read_data_valid_audio_controller_0_avalon_slave_0;
  input              cpu_0_instruction_master_read_data_valid_command_0_avalon_slave_0;
  input              cpu_0_instruction_master_read_data_valid_cpu_0_jtag_debug_module;
  input              cpu_0_instruction_master_read_data_valid_sdram_0_s1;
  input              cpu_0_instruction_master_read_data_valid_sdram_0_s1_shift_register;
  input
cpu_0_instruction_master_read_data_valid_sram_mux_0_avalon_slave_0;
  input
cpu_0_instruction_master_read_data_valid_xycoord_interface_0_avalon_slave_0;
  input              cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0;
  input              cpu_0_instruction_master_requests_command_0_avalon_slave_0;
  input              cpu_0_instruction_master_requests_cpu_0_jtag_debug_module;
  input              cpu_0_instruction_master_requests_sdram_0_s1;
  input              cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0;
  input
cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0;
  input    [ 31: 0] cpu_0_jtag_debug_module_readdata_from_sa;
  input              d1_audio_controller_0_avalon_slave_0_end_xfer;
  input              d1_command_0_avalon_slave_0_end_xfer;
  input              d1_cpu_0_jtag_debug_module_end_xfer;
  input              d1_sdram_0_s1_end_xfer;
  input              d1_sram_mux_0_avalon_slave_0_end_xfer;
  input              d1_xycoord_interface_0_avalon_slave_0_end_xfer;
  input              reset_n;
  input    [ 15: 0] sdram_0_s1_readdata_from_sa;
  input              sdram_0_s1_waitrequest_from_sa;
  input    [ 15: 0] sram_mux_0_avalon_slave_0_readdata_from_sa;
  input    [ 15: 0] xycoord_interface_0_avalon_slave_0_readdata_from_sa;

  reg                active_and_waiting_last_time;
  reg      [ 24: 0] cpu_0_instruction_master_address_last_time;
  wire     [ 24: 0] cpu_0_instruction_master_address_to_slave;
  reg      [  1: 0] cpu_0_instruction_master_dbs_address;
  wire     [  1: 0] cpu_0_instruction_master_dbs_increment;
  reg                cpu_0_instruction_master_read_last_time;
  wire     [ 31: 0] cpu_0_instruction_master_readdata;
  wire               cpu_0_instruction_master_run;
  wire               cpu_0_instruction_master_waitrequest;
  reg      [ 15: 0] dbs_16_reg_segment_0;
  wire               dbs_count_enable;
  wire               dbs_counter_overflow;
  wire     [  1: 0] next_dbs_address;
  wire     [ 15: 0] p1_dbs_16_reg_segment_0;
  wire               pre_dbs_count_enable;
  wire               r_0;
```

```
  wire        r_1;
  wire        r_2;
  //r_0 master_run cascaded wait assignment, which is an e_assign
  assign r_0 = 1 &
(cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0 |
~cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0) &
(cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0 |
~cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0) &
((~cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0 |
~cpu_0_instruction_master_read | (1 & ~d1_audio_controller_0_avalon_slave_0_end_xfer &
(cpu_0_instruction_master_dbs_address[1]) & cpu_0_instruction_master_read))) & 1 &
(cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0 |
~cpu_0_instruction_master_requests_command_0_avalon_slave_0) &
(cpu_0_instruction_master_granted_command_0_avalon_slave_0 |
~cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0) &
((~cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0 |
~cpu_0_instruction_master_read | (1 & ~d1_command_0_avalon_slave_0_end_xfer &
cpu_0_instruction_master_read))) & 1 &
(cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module |
~cpu_0_instruction_master_requests_cpu_0_jtag_debug_module) &
(cpu_0_instruction_master_granted_cpu_0_jtag_debug_module |
~cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module) &
((~cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module |
~cpu_0_instruction_master_read | (1 & ~d1_cpu_0_jtag_debug_module_end_xfer &
cpu_0_instruction_master_read)));

  //cascaded wait assignment, which is an e_assign
  assign cpu_0_instruction_master_run = r_0 & r_1 & r_2;

  //r_1 master_run cascaded wait assignment, which is an e_assign
  assign r_1 = 1 & (cpu_0_instruction_master_qualified_request_sdram_0_s1 |
(cpu_0_instruction_master_read_data_valid_sdram_0_s1 &
cpu_0_instruction_master_dbs_address[1]) | ~cpu_0_instruction_master_requests_sdram_0_s1)
& (cpu_0_instruction_master_granted_sdram_0_s1 |
~cpu_0_instruction_master_qualified_request_sdram_0_s1) &
((~cpu_0_instruction_master_qualified_request_sdram_0_s1 | ~cpu_0_instruction_master_read
| (cpu_0_instruction_master_read_data_valid_sdram_0_s1 &
(cpu_0_instruction_master_dbs_address[1]) & cpu_0_instruction_master_read))) & 1 &
(cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0 |
~cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0) &
(cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0 |
~cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0) &
((~cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0 |
~cpu_0_instruction_master_read | (1 & ~d1_sram_mux_0_avalon_slave_0_end_xfer &
(cpu_0_instruction_master_dbs_address[1]) & cpu_0_instruction_master_read))) & 1 &
(cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0 |
~cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0);

  //r_2 master_run cascaded wait assignment, which is an e_assign
  assign r_2 = (cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0 |
~cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0) &
((~cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0 |
~cpu_0_instruction_master_read | (1 & ~d1_xycoord_interface_0_avalon_slave_0_end_xfer &
(cpu_0_instruction_master_dbs_address[1]) & cpu_0_instruction_master_read)));

  //optimize select-logic by passing only those address bits which matter.
  assign cpu_0_instruction_master_address_to_slave = cpu_0_instruction_master_address[24 :
0];
```

```
  //input to dbs-16 stored 0, which is an e_mux
  assign p1_dbs_16_reg_segment_0 =
(cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0)?
audio_controller_0_avalon_slave_0_readdata_from_sa :
    (cpu_0_instruction_master_requests_sdram_0_s1)? sdram_0_s1_readdata_from_sa :
    (cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0)?
sram_mux_0_avalon_slave_0_readdata_from_sa :
    xycoord_interface_0_avalon_slave_0_readdata_from_sa;

  //dbs register for dbs-16 segment 0, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          dbs_16_reg_segment_0 <= 0;
      else if (dbs_count_enable & ((cpu_0_instruction_master_dbs_address[1]) == 0))
          dbs_16_reg_segment_0 <= p1_dbs_16_reg_segment_0;
    end


  //cpu_0/instruction_master readdata mux, which is an e_mux
  assign cpu_0_instruction_master_readdata = ({32
{~cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0}} |
{audio_controller_0_avalon_slave_0_readdata_from_sa[15 : 0],
    dbs_16_reg_segment_0}) &
    ({32 {~cpu_0_instruction_master_requests_command_0_avalon_slave_0}} |
command_0_avalon_slave_0_readdata_from_sa) &
    ({32 {~cpu_0_instruction_master_requests_cpu_0_jtag_debug_module}} |
cpu_0_jtag_debug_module_readdata_from_sa) &
    ({32 {~cpu_0_instruction_master_requests_sdram_0_s1}} |
{sdram_0_s1_readdata_from_sa[15 : 0],
    dbs_16_reg_segment_0}) &
    ({32 {~cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0}} |
{sram_mux_0_avalon_slave_0_readdata_from_sa[15 : 0],
    dbs_16_reg_segment_0}) &
    ({32 {~cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0}} |
{xycoord_interface_0_avalon_slave_0_readdata_from_sa[15 : 0],
    dbs_16_reg_segment_0});

  //actual waitrequest port, which is an e_assign
  assign cpu_0_instruction_master_waitrequest = ~cpu_0_instruction_master_run;

  //dbs count increment, which is an e_mux
  assign cpu_0_instruction_master_dbs_increment =
(cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0)? 2 :
    (cpu_0_instruction_master_requests_sdram_0_s1)? 2 :
    (cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0)? 2 :
    (cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0)? 2 :
    0;

  //dbs counter overflow, which is an e_assign
  assign dbs_counter_overflow = cpu_0_instruction_master_dbs_address[1]
& !(next_dbs_address[1]);

  //next master address, which is an e_assign
  assign next_dbs_address = cpu_0_instruction_master_dbs_address +
cpu_0_instruction_master_dbs_increment;
```

```
  //dbs count enable, which is an e_mux
  assign dbs_count_enable = pre_dbs_count_enable;

  //dbs counter, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          cpu_0_instruction_master_dbs_address <= 0;
      else if (dbs_count_enable)
          cpu_0_instruction_master_dbs_address <= next_dbs_address;
    end


  //pre dbs count enable, which is an e_mux
  assign pre_dbs_count_enable =
(cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0 &
cpu_0_instruction_master_read & 1 & 1 & ~d1_audio_controller_0_avalon_slave_0_end_xfer) |
    cpu_0_instruction_master_read_data_valid_sdram_0_s1 |
    (cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0 &
cpu_0_instruction_master_read & 1 & 1 & ~d1_sram_mux_0_avalon_slave_0_end_xfer) |
    (cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0 &
cpu_0_instruction_master_read & 1 & 1 & ~d1_xycoord_interface_0_avalon_slave_0_end_xfer);


//synthesis translate_off
//////////////// SIMULATION-ONLY CONTENTS
  //cpu_0_instruction_master_address check against wait, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          cpu_0_instruction_master_address_last_time <= 0;
      else
        cpu_0_instruction_master_address_last_time <= cpu_0_instruction_master_address;
    end


  //cpu_0/instruction_master waited last time, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          active_and_waiting_last_time <= 0;
      else
        active_and_waiting_last_time <= cpu_0_instruction_master_waitrequest &
(cpu_0_instruction_master_read);
    end


  //cpu_0_instruction_master_address matches last port_name, which is an e_process
  always @(posedge clk)
    begin
      if (active_and_waiting_last_time & (cpu_0_instruction_master_address !=
cpu_0_instruction_master_address_last_time))
        begin
          $write("%0d ns: cpu_0_instruction_master_address did not heed wait!!!", $time);
          $stop;
        end
    end
```

```
  //cpu_0_instruction_master_read check against wait, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          cpu_0_instruction_master_read_last_time <= 0;
      else
        cpu_0_instruction_master_read_last_time <= cpu_0_instruction_master_read;
    end


  //cpu_0_instruction_master_read matches last port_name, which is an e_process
  always @(posedge clk)
    begin
      if (active_and_waiting_last_time & (cpu_0_instruction_master_read !=
cpu_0_instruction_master_read_last_time))
        begin
          $write("%0d ns: cpu_0_instruction_master_read did not heed wait!!!", $time);
          $stop;
        end
    end



//////////////// END SIMULATION-ONLY CONTENTS

//synthesis translate_on

endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module interrupt_0_avalon_slave_0_arbitrator (
                                               // inputs:
                                                 clk,

cpu_0_data_master_address_to_slave,
                                                 cpu_0_data_master_read,
                                                 cpu_0_data_master_waitrequest,
                                                 cpu_0_data_master_write,
                                                 cpu_0_data_master_writedata,
                                                 interrupt_0_avalon_slave_0_irq,

interrupt_0_avalon_slave_0_readdata,
                                                 reset_n,

                                               // outputs:

cpu_0_data_master_granted_interrupt_0_avalon_slave_0,

cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0,
```

```
cpu_0_data_master_read_data_valid_interrupt_0_avalon_slave_0,

cpu_0_data_master_requests_interrupt_0_avalon_slave_0,

d1_interrupt_0_avalon_slave_0_end_xfer,
                                                        interrupt_0_avalon_slave_0_address,

interrupt_0_avalon_slave_0_chipselect,

interrupt_0_avalon_slave_0_irq_from_sa,
                                                        interrupt_0_avalon_slave_0_read,

interrupt_0_avalon_slave_0_readdata_from_sa,
                                                        interrupt_0_avalon_slave_0_reset_n,
                                                        interrupt_0_avalon_slave_0_write,

interrupt_0_avalon_slave_0_writedata
                                                    )
;

  output           cpu_0_data_master_granted_interrupt_0_avalon_slave_0;
  output           cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0;
  output           cpu_0_data_master_read_data_valid_interrupt_0_avalon_slave_0;
  output           cpu_0_data_master_requests_interrupt_0_avalon_slave_0;
  output           d1_interrupt_0_avalon_slave_0_end_xfer;
  output   [  4: 0] interrupt_0_avalon_slave_0_address;
  output           interrupt_0_avalon_slave_0_chipselect;
  output           interrupt_0_avalon_slave_0_irq_from_sa;
  output           interrupt_0_avalon_slave_0_read;
  output   [ 31: 0] interrupt_0_avalon_slave_0_readdata_from_sa;
  output           interrupt_0_avalon_slave_0_reset_n;
  output           interrupt_0_avalon_slave_0_write;
  output   [ 31: 0] interrupt_0_avalon_slave_0_writedata;
  input            clk;
  input    [ 24: 0] cpu_0_data_master_address_to_slave;
  input            cpu_0_data_master_read;
  input            cpu_0_data_master_waitrequest;
  input            cpu_0_data_master_write;
  input    [ 31: 0] cpu_0_data_master_writedata;
  input            interrupt_0_avalon_slave_0_irq;
  input    [ 31: 0] interrupt_0_avalon_slave_0_readdata;
  input            reset_n;

  wire             cpu_0_data_master_arbiterlock;
  wire             cpu_0_data_master_arbiterlock2;
  wire             cpu_0_data_master_continuerequest;
  wire             cpu_0_data_master_granted_interrupt_0_avalon_slave_0;
  wire             cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0;
  wire             cpu_0_data_master_read_data_valid_interrupt_0_avalon_slave_0;
  wire             cpu_0_data_master_requests_interrupt_0_avalon_slave_0;
  wire             cpu_0_data_master_saved_grant_interrupt_0_avalon_slave_0;
  reg              d1_interrupt_0_avalon_slave_0_end_xfer;
  reg              d1_reasons_to_wait;
  reg              enable_nonzero_assertions;
  wire             end_xfer_arb_share_counter_term_interrupt_0_avalon_slave_0;
  wire             in_a_read_cycle;
  wire             in_a_write_cycle;
```

```
  wire       [  4: 0] interrupt_0_avalon_slave_0_address;
  wire                interrupt_0_avalon_slave_0_allgrants;
  wire                interrupt_0_avalon_slave_0_allow_new_arb_cycle;
  wire                interrupt_0_avalon_slave_0_any_bursting_master_saved_grant;
  wire                interrupt_0_avalon_slave_0_any_continuerequest;
  wire                interrupt_0_avalon_slave_0_arb_counter_enable;
  reg        [  1: 0] interrupt_0_avalon_slave_0_arb_share_counter;
  wire       [  1: 0] interrupt_0_avalon_slave_0_arb_share_counter_next_value;
  wire       [  1: 0] interrupt_0_avalon_slave_0_arb_share_set_values;
  wire                interrupt_0_avalon_slave_0_beginbursttransfer_internal;
  wire                interrupt_0_avalon_slave_0_begins_xfer;
  wire                interrupt_0_avalon_slave_0_chipselect;
  wire                interrupt_0_avalon_slave_0_end_xfer;
  wire                interrupt_0_avalon_slave_0_firsttransfer;
  wire                interrupt_0_avalon_slave_0_grant_vector;
  wire                interrupt_0_avalon_slave_0_in_a_read_cycle;
  wire                interrupt_0_avalon_slave_0_in_a_write_cycle;
  wire                interrupt_0_avalon_slave_0_irq_from_sa;
  wire                interrupt_0_avalon_slave_0_master_qreq_vector;
  wire                interrupt_0_avalon_slave_0_non_bursting_master_requests;
  wire                interrupt_0_avalon_slave_0_read;
  wire       [ 31: 0] interrupt_0_avalon_slave_0_readdata_from_sa;
  reg                 interrupt_0_avalon_slave_0_reg_firsttransfer;
  wire                interrupt_0_avalon_slave_0_reset_n;
  reg                 interrupt_0_avalon_slave_0_slavearbiterlockenable;
  wire                interrupt_0_avalon_slave_0_slavearbiterlockenable2;
  wire                interrupt_0_avalon_slave_0_unreg_firsttransfer;
  wire                interrupt_0_avalon_slave_0_waits_for_read;
  wire                interrupt_0_avalon_slave_0_waits_for_write;
  wire                interrupt_0_avalon_slave_0_write;
  wire       [ 31: 0] interrupt_0_avalon_slave_0_writedata;
  wire       [ 24: 0] shifted_address_to_interrupt_0_avalon_slave_0_from_cpu_0_data_master;
  wire                wait_for_interrupt_0_avalon_slave_0_counter;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_reasons_to_wait <= 0;
      else
        d1_reasons_to_wait <= ~interrupt_0_avalon_slave_0_end_xfer;
    end


  assign interrupt_0_avalon_slave_0_begins_xfer = ~d1_reasons_to_wait &
((cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0));
  //assign interrupt_0_avalon_slave_0_readdata_from_sa =
interrupt_0_avalon_slave_0_readdata so that symbol knows where to group signals which may
go to master only, which is an e_assign
  assign interrupt_0_avalon_slave_0_readdata_from_sa =
interrupt_0_avalon_slave_0_readdata;

  assign cpu_0_data_master_requests_interrupt_0_avalon_slave_0 =
({cpu_0_data_master_address_to_slave[24 : 7] , 7'b0} == 25'h0) & (cpu_0_data_master_read |
cpu_0_data_master_write);
  //interrupt_0_avalon_slave_0_arb_share_counter set values, which is an e_mux
  assign interrupt_0_avalon_slave_0_arb_share_set_values = 1;

  //interrupt_0_avalon_slave_0_non_bursting_master_requests mux, which is an e_mux
  assign interrupt_0_avalon_slave_0_non_bursting_master_requests =
```

```
cpu_0_data_master_requests_interrupt_0_avalon_slave_0;

  //interrupt_0_avalon_slave_0_any_bursting_master_saved_grant mux, which is an e_mux
  assign interrupt_0_avalon_slave_0_any_bursting_master_saved_grant = 0;

  //interrupt_0_avalon_slave_0_arb_share_counter_next_value assignment, which is an
e_assign
  assign interrupt_0_avalon_slave_0_arb_share_counter_next_value =
interrupt_0_avalon_slave_0_firsttransfer ? (interrupt_0_avalon_slave_0_arb_share_set_values -
1) : |interrupt_0_avalon_slave_0_arb_share_counter ?
(interrupt_0_avalon_slave_0_arb_share_counter - 1) : 0;

  //interrupt_0_avalon_slave_0_allgrants all slave grants, which is an e_mux
  assign interrupt_0_avalon_slave_0_allgrants = |interrupt_0_avalon_slave_0_grant_vector;

  //interrupt_0_avalon_slave_0_end_xfer assignment, which is an e_assign
  assign interrupt_0_avalon_slave_0_end_xfer = ~(interrupt_0_avalon_slave_0_waits_for_read
| interrupt_0_avalon_slave_0_waits_for_write);

  //end_xfer_arb_share_counter_term_interrupt_0_avalon_slave_0 arb share counter enable
term, which is an e_assign
  assign end_xfer_arb_share_counter_term_interrupt_0_avalon_slave_0 =
interrupt_0_avalon_slave_0_end_xfer &
(~interrupt_0_avalon_slave_0_any_bursting_master_saved_grant | in_a_read_cycle |
in_a_write_cycle);

  //interrupt_0_avalon_slave_0_arb_share_counter arbitration counter enable, which is an
e_assign
  assign interrupt_0_avalon_slave_0_arb_counter_enable =
(end_xfer_arb_share_counter_term_interrupt_0_avalon_slave_0 &
interrupt_0_avalon_slave_0_allgrants) |
(end_xfer_arb_share_counter_term_interrupt_0_avalon_slave_0 &
~interrupt_0_avalon_slave_0_non_bursting_master_requests);

  //interrupt_0_avalon_slave_0_arb_share_counter counter, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          interrupt_0_avalon_slave_0_arb_share_counter <= 0;
      else if (interrupt_0_avalon_slave_0_arb_counter_enable)
          interrupt_0_avalon_slave_0_arb_share_counter <=
interrupt_0_avalon_slave_0_arb_share_counter_next_value;
    end


  //interrupt_0_avalon_slave_0_slavearbiterlockenable slave enables arbiterlock, which is an
e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          interrupt_0_avalon_slave_0_slavearbiterlockenable <= 0;
      else if ((|interrupt_0_avalon_slave_0_master_qreq_vector &
end_xfer_arb_share_counter_term_interrupt_0_avalon_slave_0) |
(end_xfer_arb_share_counter_term_interrupt_0_avalon_slave_0 &
~interrupt_0_avalon_slave_0_non_bursting_master_requests))
          interrupt_0_avalon_slave_0_slavearbiterlockenable <=
|interrupt_0_avalon_slave_0_arb_share_counter_next_value;
    end
```

```
  //cpu_0/data_master interrupt_0/avalon_slave_0 arbiterlock, which is an e_assign
  assign cpu_0_data_master_arbiterlock = interrupt_0_avalon_slave_0_slavearbiterlockenable
& cpu_0_data_master_continuerequest;

  //interrupt_0_avalon_slave_0_slavearbiterlockenable2 slave enables arbiterlock2, which is an
e_assign
  assign interrupt_0_avalon_slave_0_slavearbiterlockenable2 =
|interrupt_0_avalon_slave_0_arb_share_counter_next_value;

  //cpu_0/data_master interrupt_0/avalon_slave_0 arbiterlock2, which is an e_assign
  assign cpu_0_data_master_arbiterlock2 =
interrupt_0_avalon_slave_0_slavearbiterlockenable2 & cpu_0_data_master_continuerequest;

  //interrupt_0_avalon_slave_0_any_continuerequest at least one master continues requesting,
which is an e_assign
  assign interrupt_0_avalon_slave_0_any_continuerequest = 1;

  //cpu_0_data_master_continuerequest continued request, which is an e_assign
  assign cpu_0_data_master_continuerequest = 1;

  assign cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0 =
cpu_0_data_master_requests_interrupt_0_avalon_slave_0 &
~(((~cpu_0_data_master_waitrequest) & cpu_0_data_master_write));
  //interrupt_0_avalon_slave_0_writedata mux, which is an e_mux
  assign interrupt_0_avalon_slave_0_writedata = cpu_0_data_master_writedata;

  //master is always granted when requested
  assign cpu_0_data_master_granted_interrupt_0_avalon_slave_0 =
cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0;

  //cpu_0/data_master saved-grant interrupt_0/avalon_slave_0, which is an e_assign
  assign cpu_0_data_master_saved_grant_interrupt_0_avalon_slave_0 =
cpu_0_data_master_requests_interrupt_0_avalon_slave_0;

  //allow new arb cycle for interrupt_0/avalon_slave_0, which is an e_assign
  assign interrupt_0_avalon_slave_0_allow_new_arb_cycle = 1;

  //placeholder chosen master
  assign interrupt_0_avalon_slave_0_grant_vector = 1;

  //placeholder vector of master qualified-requests
  assign interrupt_0_avalon_slave_0_master_qreq_vector = 1;

  //interrupt_0_avalon_slave_0_reset_n assignment, which is an e_assign
  assign interrupt_0_avalon_slave_0_reset_n = reset_n;

  assign interrupt_0_avalon_slave_0_chipselect =
cpu_0_data_master_granted_interrupt_0_avalon_slave_0;
  //interrupt_0_avalon_slave_0_firsttransfer first transaction, which is an e_assign
  assign interrupt_0_avalon_slave_0_firsttransfer = interrupt_0_avalon_slave_0_begins_xfer ?
interrupt_0_avalon_slave_0_unreg_firsttransfer : interrupt_0_avalon_slave_0_reg_firsttransfer;

  //interrupt_0_avalon_slave_0_unreg_firsttransfer first transaction, which is an e_assign
  assign interrupt_0_avalon_slave_0_unreg_firsttransfer =
~(interrupt_0_avalon_slave_0_slavearbiterlockenable &
interrupt_0_avalon_slave_0_any_continuerequest);
```

```
  //interrupt_0_avalon_slave_0_reg_firsttransfer first transaction, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          interrupt_0_avalon_slave_0_reg_firsttransfer <= 1'b1;
      else if (interrupt_0_avalon_slave_0_begins_xfer)
          interrupt_0_avalon_slave_0_reg_firsttransfer <=
interrupt_0_avalon_slave_0_unreg_firsttransfer;
    end


  //interrupt_0_avalon_slave_0_beginbursttransfer_internal begin burst transfer, which is an
e_assign
  assign interrupt_0_avalon_slave_0_beginbursttransfer_internal =
interrupt_0_avalon_slave_0_begins_xfer;

  //interrupt_0_avalon_slave_0_read assignment, which is an e_mux
  assign interrupt_0_avalon_slave_0_read =
cpu_0_data_master_granted_interrupt_0_avalon_slave_0 & cpu_0_data_master_read;

  //interrupt_0_avalon_slave_0_write assignment, which is an e_mux
  assign interrupt_0_avalon_slave_0_write =
cpu_0_data_master_granted_interrupt_0_avalon_slave_0 & cpu_0_data_master_write;

  assign shifted_address_to_interrupt_0_avalon_slave_0_from_cpu_0_data_master =
cpu_0_data_master_address_to_slave;
  //interrupt_0_avalon_slave_0_address mux, which is an e_mux
  assign interrupt_0_avalon_slave_0_address =
shifted_address_to_interrupt_0_avalon_slave_0_from_cpu_0_data_master >> 2;

  //d1_interrupt_0_avalon_slave_0_end_xfer register, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_interrupt_0_avalon_slave_0_end_xfer <= 1;
      else
        d1_interrupt_0_avalon_slave_0_end_xfer <= interrupt_0_avalon_slave_0_end_xfer;
    end


  //interrupt_0_avalon_slave_0_waits_for_read in a cycle, which is an e_mux
  assign interrupt_0_avalon_slave_0_waits_for_read =
interrupt_0_avalon_slave_0_in_a_read_cycle & interrupt_0_avalon_slave_0_begins_xfer;

  //interrupt_0_avalon_slave_0_in_a_read_cycle assignment, which is an e_assign
  assign interrupt_0_avalon_slave_0_in_a_read_cycle =
cpu_0_data_master_granted_interrupt_0_avalon_slave_0 & cpu_0_data_master_read;

  //in_a_read_cycle assignment, which is an e_mux
  assign in_a_read_cycle = interrupt_0_avalon_slave_0_in_a_read_cycle;

  //interrupt_0_avalon_slave_0_waits_for_write in a cycle, which is an e_mux
  assign interrupt_0_avalon_slave_0_waits_for_write =
interrupt_0_avalon_slave_0_in_a_write_cycle & 0;

  //interrupt_0_avalon_slave_0_in_a_write_cycle assignment, which is an e_assign
  assign interrupt_0_avalon_slave_0_in_a_write_cycle =
```

```
cpu_0_data_master_granted_interrupt_0_avalon_slave_0 & cpu_0_data_master_write;

  //in_a_write_cycle assignment, which is an e_mux
  assign in_a_write_cycle = interrupt_0_avalon_slave_0_in_a_write_cycle;

  assign wait_for_interrupt_0_avalon_slave_0_counter = 0;
  //assign interrupt_0_avalon_slave_0_irq_from_sa = interrupt_0_avalon_slave_0_irq so that symbol knows where to group signals which may go to master only, which is an e_assign
  assign interrupt_0_avalon_slave_0_irq_from_sa = interrupt_0_avalon_slave_0_irq;


//synthesis translate_off
//////////////// SIMULATION-ONLY CONTENTS
  //interrupt_0/avalon_slave_0 enable non-zero assertions, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          enable_nonzero_assertions <= 0;
      else
        enable_nonzero_assertions <= 1'b1;
    end



//////////////// END SIMULATION-ONLY CONTENTS

//synthesis translate_on

endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module jtag_uart_0_avalon_jtag_slave_arbitrator (
                                                  // inputs:
                                                    clk,

cpu_0_data_master_address_to_slave,
                                                    cpu_0_data_master_read,
                                                    cpu_0_data_master_waitrequest,
                                                    cpu_0_data_master_write,
                                                    cpu_0_data_master_writedata,

jtag_uart_0_avalon_jtag_slave_dataavailable,

jtag_uart_0_avalon_jtag_slave_irq,

jtag_uart_0_avalon_jtag_slave_readdata,

jtag_uart_0_avalon_jtag_slave_readyfordata,

jtag_uart_0_avalon_jtag_slave_waitrequest,
```

```
                                                                reset_n,

                                                               // outputs:

cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave,

cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave,

cpu_0_data_master_read_data_valid_jtag_uart_0_avalon_jtag_slave,

cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave,

d1_jtag_uart_0_avalon_jtag_slave_end_xfer,

jtag_uart_0_avalon_jtag_slave_address,

jtag_uart_0_avalon_jtag_slave_chipselect,

jtag_uart_0_avalon_jtag_slave_dataavailable_from_sa,

jtag_uart_0_avalon_jtag_slave_irq_from_sa,

jtag_uart_0_avalon_jtag_slave_read_n,

jtag_uart_0_avalon_jtag_slave_readdata_from_sa,

jtag_uart_0_avalon_jtag_slave_readyfordata_from_sa,

jtag_uart_0_avalon_jtag_slave_reset_n,

jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa,

jtag_uart_0_avalon_jtag_slave_write_n,

jtag_uart_0_avalon_jtag_slave_writedata
                                                                )
;

  output           cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave;
  output           cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave;
  output           cpu_0_data_master_read_data_valid_jtag_uart_0_avalon_jtag_slave;
  output           cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave;
  output           d1_jtag_uart_0_avalon_jtag_slave_end_xfer;
  output           jtag_uart_0_avalon_jtag_slave_address;
  output           jtag_uart_0_avalon_jtag_slave_chipselect;
  output           jtag_uart_0_avalon_jtag_slave_dataavailable_from_sa;
  output           jtag_uart_0_avalon_jtag_slave_irq_from_sa;
  output           jtag_uart_0_avalon_jtag_slave_read_n;
  output   [ 31: 0] jtag_uart_0_avalon_jtag_slave_readdata_from_sa;
  output           jtag_uart_0_avalon_jtag_slave_readyfordata_from_sa;
  output           jtag_uart_0_avalon_jtag_slave_reset_n;
  output           jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa;
  output           jtag_uart_0_avalon_jtag_slave_write_n;
  output   [ 31: 0] jtag_uart_0_avalon_jtag_slave_writedata;
  input            clk;
  input    [ 24: 0] cpu_0_data_master_address_to_slave;
  input            cpu_0_data_master_read;
  input            cpu_0_data_master_waitrequest;
```

```
input              cpu_0_data_master_write;
input  [ 31: 0] cpu_0_data_master_writedata;
input              jtag_uart_0_avalon_jtag_slave_dataavailable;
input              jtag_uart_0_avalon_jtag_slave_irq;
input  [ 31: 0] jtag_uart_0_avalon_jtag_slave_readdata;
input              jtag_uart_0_avalon_jtag_slave_readyfordata;
input              jtag_uart_0_avalon_jtag_slave_waitrequest;
input              reset_n;

wire               cpu_0_data_master_arbiterlock;
wire               cpu_0_data_master_arbiterlock2;
wire               cpu_0_data_master_continuerequest;
wire               cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave;
wire               cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave;
wire               cpu_0_data_master_read_data_valid_jtag_uart_0_avalon_jtag_slave;
wire               cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave;
wire               cpu_0_data_master_saved_grant_jtag_uart_0_avalon_jtag_slave;
reg                d1_jtag_uart_0_avalon_jtag_slave_end_xfer;
reg                d1_reasons_to_wait;
reg                enable_nonzero_assertions;
wire               end_xfer_arb_share_counter_term_jtag_uart_0_avalon_jtag_slave;
wire               in_a_read_cycle;
wire               in_a_write_cycle;
wire               jtag_uart_0_avalon_jtag_slave_address;
wire               jtag_uart_0_avalon_jtag_slave_allgrants;
wire               jtag_uart_0_avalon_jtag_slave_allow_new_arb_cycle;
wire               jtag_uart_0_avalon_jtag_slave_any_bursting_master_saved_grant;
wire               jtag_uart_0_avalon_jtag_slave_any_continuerequest;
wire               jtag_uart_0_avalon_jtag_slave_arb_counter_enable;
reg    [  1: 0] jtag_uart_0_avalon_jtag_slave_arb_share_counter;
wire   [  1: 0] jtag_uart_0_avalon_jtag_slave_arb_share_counter_next_value;
wire   [  1: 0] jtag_uart_0_avalon_jtag_slave_arb_share_set_values;
wire               jtag_uart_0_avalon_jtag_slave_beginbursttransfer_internal;
wire               jtag_uart_0_avalon_jtag_slave_begins_xfer;
wire               jtag_uart_0_avalon_jtag_slave_chipselect;
wire               jtag_uart_0_avalon_jtag_slave_dataavailable_from_sa;
wire               jtag_uart_0_avalon_jtag_slave_end_xfer;
wire               jtag_uart_0_avalon_jtag_slave_firsttransfer;
wire               jtag_uart_0_avalon_jtag_slave_grant_vector;
wire               jtag_uart_0_avalon_jtag_slave_in_a_read_cycle;
wire               jtag_uart_0_avalon_jtag_slave_in_a_write_cycle;
wire               jtag_uart_0_avalon_jtag_slave_irq_from_sa;
wire               jtag_uart_0_avalon_jtag_slave_master_qreq_vector;
wire               jtag_uart_0_avalon_jtag_slave_non_bursting_master_requests;
wire               jtag_uart_0_avalon_jtag_slave_read_n;
wire   [ 31: 0] jtag_uart_0_avalon_jtag_slave_readdata_from_sa;
wire               jtag_uart_0_avalon_jtag_slave_readyfordata_from_sa;
reg                jtag_uart_0_avalon_jtag_slave_reg_firsttransfer;
wire               jtag_uart_0_avalon_jtag_slave_reset_n;
reg                jtag_uart_0_avalon_jtag_slave_slavearbiterlockenable;
wire               jtag_uart_0_avalon_jtag_slave_slavearbiterlockenable2;
wire               jtag_uart_0_avalon_jtag_slave_unreg_firsttransfer;
wire               jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa;
wire               jtag_uart_0_avalon_jtag_slave_waits_for_read;
wire               jtag_uart_0_avalon_jtag_slave_waits_for_write;
wire               jtag_uart_0_avalon_jtag_slave_write_n;
wire   [ 31: 0] jtag_uart_0_avalon_jtag_slave_writedata;
wire                                                    [  24:  0]
```

```
shifted_address_to_jtag_uart_0_avalon_jtag_slave_from_cpu_0_data_master;
  wire                    wait_for_jtag_uart_0_avalon_jtag_slave_counter;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_reasons_to_wait <= 0;
      else
        d1_reasons_to_wait <= ~jtag_uart_0_avalon_jtag_slave_end_xfer;
    end


  assign jtag_uart_0_avalon_jtag_slave_begins_xfer = ~d1_reasons_to_wait &
((cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave));
  //assign                    jtag_uart_0_avalon_jtag_slave_readdata_from_sa                    =
jtag_uart_0_avalon_jtag_slave_readdata so that symbol knows where to group signals which
may go to master only, which is an e_assign
  assign                    jtag_uart_0_avalon_jtag_slave_readdata_from_sa                    =
jtag_uart_0_avalon_jtag_slave_readdata;

  assign                cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave                =
({cpu_0_data_master_address_to_slave[24    :    3]    ,    3'b0}    ==    25'h1001180)    &
(cpu_0_data_master_read | cpu_0_data_master_write);
  //assign                    jtag_uart_0_avalon_jtag_slave_dataavailable_from_sa                    =
jtag_uart_0_avalon_jtag_slave_dataavailable so that symbol knows where to group signals which
may go to master only, which is an e_assign
  assign                    jtag_uart_0_avalon_jtag_slave_dataavailable_from_sa                    =
jtag_uart_0_avalon_jtag_slave_dataavailable;

  //assign                    jtag_uart_0_avalon_jtag_slave_readyfordata_from_sa                    =
jtag_uart_0_avalon_jtag_slave_readyfordata so that symbol knows where to group signals which
may go to master only, which is an e_assign
  assign                    jtag_uart_0_avalon_jtag_slave_readyfordata_from_sa                    =
jtag_uart_0_avalon_jtag_slave_readyfordata;

  //assign                    jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa                    =
jtag_uart_0_avalon_jtag_slave_waitrequest so that symbol knows where to group signals which
may go to master only, which is an e_assign
  assign                    jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa                    =
jtag_uart_0_avalon_jtag_slave_waitrequest;

  //jtag_uart_0_avalon_jtag_slave_arb_share_counter set values, which is an e_mux
  assign jtag_uart_0_avalon_jtag_slave_arb_share_set_values = 1;

  //jtag_uart_0_avalon_jtag_slave_non_bursting_master_requests mux, which is an e_mux
  assign                jtag_uart_0_avalon_jtag_slave_non_bursting_master_requests                =
cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave;

  //jtag_uart_0_avalon_jtag_slave_any_bursting_master_saved_grant mux, which is an e_mux
  assign jtag_uart_0_avalon_jtag_slave_any_bursting_master_saved_grant = 0;

  //jtag_uart_0_avalon_jtag_slave_arb_share_counter_next_value assignment, which is an
e_assign
  assign                jtag_uart_0_avalon_jtag_slave_arb_share_counter_next_value                =
jtag_uart_0_avalon_jtag_slave_firsttransfer                                                     ?
(jtag_uart_0_avalon_jtag_slave_arb_share_set_values                -                1)          :
|jtag_uart_0_avalon_jtag_slave_arb_share_counter                                               ?
(jtag_uart_0_avalon_jtag_slave_arb_share_counter - 1) : 0;
```

```
  //jtag_uart_0_avalon_jtag_slave_allgrants all slave grants, which is an e_mux
  assign jtag_uart_0_avalon_jtag_slave_allgrants =
|jtag_uart_0_avalon_jtag_slave_grant_vector;

  //jtag_uart_0_avalon_jtag_slave_end_xfer assignment, which is an e_assign
  assign jtag_uart_0_avalon_jtag_slave_end_xfer =
~(jtag_uart_0_avalon_jtag_slave_waits_for_read |
jtag_uart_0_avalon_jtag_slave_waits_for_write);

  //end_xfer_arb_share_counter_term_jtag_uart_0_avalon_jtag_slave arb share counter
enable term, which is an e_assign
  assign end_xfer_arb_share_counter_term_jtag_uart_0_avalon_jtag_slave =
jtag_uart_0_avalon_jtag_slave_end_xfer &
(~jtag_uart_0_avalon_jtag_slave_any_bursting_master_saved_grant | in_a_read_cycle |
in_a_write_cycle);

  //jtag_uart_0_avalon_jtag_slave_arb_share_counter arbitration counter enable, which is an
e_assign
  assign jtag_uart_0_avalon_jtag_slave_arb_counter_enable =
(end_xfer_arb_share_counter_term_jtag_uart_0_avalon_jtag_slave &
jtag_uart_0_avalon_jtag_slave_allgrants) |
(end_xfer_arb_share_counter_term_jtag_uart_0_avalon_jtag_slave &
~jtag_uart_0_avalon_jtag_slave_non_bursting_master_requests);

  //jtag_uart_0_avalon_jtag_slave_arb_share_counter counter, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          jtag_uart_0_avalon_jtag_slave_arb_share_counter <= 0;
      else if (jtag_uart_0_avalon_jtag_slave_arb_counter_enable)
          jtag_uart_0_avalon_jtag_slave_arb_share_counter <=
jtag_uart_0_avalon_jtag_slave_arb_share_counter_next_value;
    end


  //jtag_uart_0_avalon_jtag_slave_slavearbiterlockenable slave enables arbiterlock, which is an
e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          jtag_uart_0_avalon_jtag_slave_slavearbiterlockenable <= 0;
      else if (((|jtag_uart_0_avalon_jtag_slave_master_qreq_vector &
end_xfer_arb_share_counter_term_jtag_uart_0_avalon_jtag_slave) |
(end_xfer_arb_share_counter_term_jtag_uart_0_avalon_jtag_slave &
~jtag_uart_0_avalon_jtag_slave_non_bursting_master_requests))
          jtag_uart_0_avalon_jtag_slave_slavearbiterlockenable <=
|jtag_uart_0_avalon_jtag_slave_arb_share_counter_next_value;
    end


  //cpu_0/data_master jtag_uart_0/avalon_jtag_slave arbiterlock, which is an e_assign
  assign cpu_0_data_master_arbiterlock =
jtag_uart_0_avalon_jtag_slave_slavearbiterlockenable & cpu_0_data_master_continuerequest;

  //jtag_uart_0_avalon_jtag_slave_slavearbiterlockenable2 slave enables arbiterlock2, which is
an e_assign
  assign jtag_uart_0_avalon_jtag_slave_slavearbiterlockenable2 =
|jtag_uart_0_avalon_jtag_slave_arb_share_counter_next_value;
```

```
  //cpu_0/data_master jtag_uart_0/avalon_jtag_slave arbiterlock2, which is an e_assign
  assign cpu_0_data_master_arbiterlock2 = jtag_uart_0_avalon_jtag_slave_slavearbiterlockenable2 & cpu_0_data_master_continuerequest;

  //jtag_uart_0_avalon_jtag_slave_any_continuerequest at least one master continues requesting, which is an e_assign
  assign jtag_uart_0_avalon_jtag_slave_any_continuerequest = 1;

  //cpu_0_data_master_continuerequest continued request, which is an e_assign
  assign cpu_0_data_master_continuerequest = 1;

  assign cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave = cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave & ~((cpu_0_data_master_read & (~cpu_0_data_master_waitrequest)) | ((~cpu_0_data_master_waitrequest) & cpu_0_data_master_write));
  //jtag_uart_0_avalon_jtag_slave_writedata mux, which is an e_mux
  assign jtag_uart_0_avalon_jtag_slave_writedata = cpu_0_data_master_writedata;

  //master is always granted when requested
  assign cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave = cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave;

  //cpu_0/data_master saved-grant jtag_uart_0/avalon_jtag_slave, which is an e_assign
  assign cpu_0_data_master_saved_grant_jtag_uart_0_avalon_jtag_slave = cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave;

  //allow new arb cycle for jtag_uart_0/avalon_jtag_slave, which is an e_assign
  assign jtag_uart_0_avalon_jtag_slave_allow_new_arb_cycle = 1;

  //placeholder chosen master
  assign jtag_uart_0_avalon_jtag_slave_grant_vector = 1;

  //placeholder vector of master qualified-requests
  assign jtag_uart_0_avalon_jtag_slave_master_qreq_vector = 1;

  //jtag_uart_0_avalon_jtag_slave_reset_n assignment, which is an e_assign
  assign jtag_uart_0_avalon_jtag_slave_reset_n = reset_n;

  assign jtag_uart_0_avalon_jtag_slave_chipselect = cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave;
  //jtag_uart_0_avalon_jtag_slave_firsttransfer first transaction, which is an e_assign
  assign jtag_uart_0_avalon_jtag_slave_firsttransfer = jtag_uart_0_avalon_jtag_slave_begins_xfer ? jtag_uart_0_avalon_jtag_slave_unreg_firsttransfer : jtag_uart_0_avalon_jtag_slave_reg_firsttransfer;

  //jtag_uart_0_avalon_jtag_slave_unreg_firsttransfer first transaction, which is an e_assign
  assign jtag_uart_0_avalon_jtag_slave_unreg_firsttransfer = ~(jtag_uart_0_avalon_jtag_slave_slavearbiterlockenable & jtag_uart_0_avalon_jtag_slave_any_continuerequest);

  //jtag_uart_0_avalon_jtag_slave_reg_firsttransfer first transaction, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          jtag_uart_0_avalon_jtag_slave_reg_firsttransfer <= 1'b1;
      else if (jtag_uart_0_avalon_jtag_slave_begins_xfer)
          jtag_uart_0_avalon_jtag_slave_reg_firsttransfer <=
```

```
jtag_uart_0_avalon_jtag_slave_unreg_firsttransfer;
      end


   //jtag_uart_0_avalon_jtag_slave_beginbursttransfer_internal begin burst transfer, which is an
e_assign
   assign                jtag_uart_0_avalon_jtag_slave_beginbursttransfer_internal                =
jtag_uart_0_avalon_jtag_slave_begins_xfer;

   //~jtag_uart_0_avalon_jtag_slave_read_n assignment, which is an e_mux
   assign                                jtag_uart_0_avalon_jtag_slave_read_n                     =
~(cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave & cpu_0_data_master_read);

   //~jtag_uart_0_avalon_jtag_slave_write_n assignment, which is an e_mux
   assign                                jtag_uart_0_avalon_jtag_slave_write_n                    =
~(cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave & cpu_0_data_master_write);

   assign      shifted_address_to_jtag_uart_0_avalon_jtag_slave_from_cpu_0_data_master      =
cpu_0_data_master_address_to_slave;
   //jtag_uart_0_avalon_jtag_slave_address mux, which is an e_mux
   assign                                jtag_uart_0_avalon_jtag_slave_address                    =
shifted_address_to_jtag_uart_0_avalon_jtag_slave_from_cpu_0_data_master >> 2;

   //d1_jtag_uart_0_avalon_jtag_slave_end_xfer register, which is an e_register
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               d1_jtag_uart_0_avalon_jtag_slave_end_xfer <= 1;
         else
            d1_jtag_uart_0_avalon_jtag_slave_end_xfer                                          <=
jtag_uart_0_avalon_jtag_slave_end_xfer;
      end


   //jtag_uart_0_avalon_jtag_slave_waits_for_read in a cycle, which is an e_mux
   assign                                jtag_uart_0_avalon_jtag_slave_waits_for_read             =
jtag_uart_0_avalon_jtag_slave_in_a_read_cycle                                                      &
jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa;

   //jtag_uart_0_avalon_jtag_slave_in_a_read_cycle assignment, which is an e_assign
   assign                                jtag_uart_0_avalon_jtag_slave_in_a_read_cycle             =
cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave & cpu_0_data_master_read;

   //in_a_read_cycle assignment, which is an e_mux
   assign in_a_read_cycle = jtag_uart_0_avalon_jtag_slave_in_a_read_cycle;

   //jtag_uart_0_avalon_jtag_slave_waits_for_write in a cycle, which is an e_mux
   assign                                jtag_uart_0_avalon_jtag_slave_waits_for_write            =
jtag_uart_0_avalon_jtag_slave_in_a_write_cycle                                                     &
jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa;

   //jtag_uart_0_avalon_jtag_slave_in_a_write_cycle assignment, which is an e_assign
   assign                                jtag_uart_0_avalon_jtag_slave_in_a_write_cycle            =
cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave & cpu_0_data_master_write;

   //in_a_write_cycle assignment, which is an e_mux
   assign in_a_write_cycle = jtag_uart_0_avalon_jtag_slave_in_a_write_cycle;
```

```
  assign wait_for_jtag_uart_0_avalon_jtag_slave_counter = 0;
  //assign  jtag_uart_0_avalon_jtag_slave_irq_from_sa  =  jtag_uart_0_avalon_jtag_slave_irq  so
that symbol knows where to group signals which may go to master only, which is an e_assign
  assign jtag_uart_0_avalon_jtag_slave_irq_from_sa = jtag_uart_0_avalon_jtag_slave_irq;


//synthesis translate_off
//////////////// SIMULATION-ONLY CONTENTS
  //jtag_uart_0/avalon_jtag_slave enable non-zero assertions, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          enable_nonzero_assertions <= 0;
      else
        enable_nonzero_assertions <= 1'b1;
    end



//////////////// END SIMULATION-ONLY CONTENTS

//synthesis translate_on

endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module musiccontroller_0_avalon_slave_0_arbitrator (
                                                     // inputs:
                                                      clk,

cpu_0_data_master_address_to_slave,

cpu_0_data_master_byteenable,

cpu_0_data_master_dbs_address,

cpu_0_data_master_dbs_write_16,

cpu_0_data_master_no_byte_enables_and_last_term,
                                                      cpu_0_data_master_read,

cpu_0_data_master_waitrequest,
                                                      cpu_0_data_master_write,

musiccontroller_0_avalon_slave_0_irq,

musiccontroller_0_avalon_slave_0_readdata,
                                                      reset_n,

                                                     // outputs:
```

```
cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0,

cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0,

cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0,

cpu_0_data_master_read_data_valid_musiccontroller_0_avalon_slave_0,

cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0,

d1_musiccontroller_0_avalon_slave_0_end_xfer,

musiccontroller_0_avalon_slave_0_address,

musiccontroller_0_avalon_slave_0_chipselect,

musiccontroller_0_avalon_slave_0_irq_from_sa,

musiccontroller_0_avalon_slave_0_read,

musiccontroller_0_avalon_slave_0_readdata_from_sa,

musiccontroller_0_avalon_slave_0_reset_n,

musiccontroller_0_avalon_slave_0_write,

musiccontroller_0_avalon_slave_0_writedata
                                                                )
;

   output    [    1: 0] cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0;
   output                cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0;
   output
cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0;
   output                cpu_0_data_master_read_data_valid_musiccontroller_0_avalon_slave_0;
   output                cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0;
   output                d1_musiccontroller_0_avalon_slave_0_end_xfer;
   output    [ 16: 0] musiccontroller_0_avalon_slave_0_address;
   output                musiccontroller_0_avalon_slave_0_chipselect;
   output                musiccontroller_0_avalon_slave_0_irq_from_sa;
   output                musiccontroller_0_avalon_slave_0_read;
   output    [ 15: 0] musiccontroller_0_avalon_slave_0_readdata_from_sa;
   output                musiccontroller_0_avalon_slave_0_reset_n;
   output                musiccontroller_0_avalon_slave_0_write;
   output    [ 15: 0] musiccontroller_0_avalon_slave_0_writedata;
   input                 clk;
   input     [ 24: 0] cpu_0_data_master_address_to_slave;
   input     [    3: 0] cpu_0_data_master_byteenable;
   input     [    1: 0] cpu_0_data_master_dbs_address;
   input     [ 15: 0] cpu_0_data_master_dbs_write_16;
   input                 cpu_0_data_master_no_byte_enables_and_last_term;
   input                 cpu_0_data_master_read;
   input                 cpu_0_data_master_waitrequest;
   input                 cpu_0_data_master_write;
   input                 musiccontroller_0_avalon_slave_0_irq;
   input     [ 15: 0] musiccontroller_0_avalon_slave_0_readdata;
   input                 reset_n;
```

```
  wire                cpu_0_data_master_arbiterlock;
  wire                cpu_0_data_master_arbiterlock2;
  wire    [  1: 0] cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0;
  wire                                                [                1:                0]
cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0_segment_0;
  wire                                                [                1:                0]
cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0_segment_1;
  wire                cpu_0_data_master_continuerequest;
  wire                cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0;
  wire
cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0;
  wire                cpu_0_data_master_read_data_valid_musiccontroller_0_avalon_slave_0;
  wire                cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0;
  wire                cpu_0_data_master_saved_grant_musiccontroller_0_avalon_slave_0;
  reg                 d1_musiccontroller_0_avalon_slave_0_end_xfer;
  reg                 d1_reasons_to_wait;
  reg                 enable_nonzero_assertions;
  wire                end_xfer_arb_share_counter_term_musiccontroller_0_avalon_slave_0;
  wire                in_a_read_cycle;
  wire                in_a_write_cycle;
  wire    [ 16: 0] musiccontroller_0_avalon_slave_0_address;
  wire                musiccontroller_0_avalon_slave_0_allgrants;
  wire                musiccontroller_0_avalon_slave_0_allow_new_arb_cycle;
  wire                musiccontroller_0_avalon_slave_0_any_bursting_master_saved_grant;
  wire                musiccontroller_0_avalon_slave_0_any_continuerequest;
  wire                musiccontroller_0_avalon_slave_0_arb_counter_enable;
  reg     [  1: 0] musiccontroller_0_avalon_slave_0_arb_share_counter;
  wire    [  1: 0] musiccontroller_0_avalon_slave_0_arb_share_counter_next_value;
  wire    [  1: 0] musiccontroller_0_avalon_slave_0_arb_share_set_values;
  wire                musiccontroller_0_avalon_slave_0_beginbursttransfer_internal;
  wire                musiccontroller_0_avalon_slave_0_begins_xfer;
  wire                musiccontroller_0_avalon_slave_0_chipselect;
  wire                musiccontroller_0_avalon_slave_0_end_xfer;
  wire                musiccontroller_0_avalon_slave_0_firsttransfer;
  wire                musiccontroller_0_avalon_slave_0_grant_vector;
  wire                musiccontroller_0_avalon_slave_0_in_a_read_cycle;
  wire                musiccontroller_0_avalon_slave_0_in_a_write_cycle;
  wire                musiccontroller_0_avalon_slave_0_irq_from_sa;
  wire                musiccontroller_0_avalon_slave_0_master_qreq_vector;
  wire                musiccontroller_0_avalon_slave_0_non_bursting_master_requests;
  wire                musiccontroller_0_avalon_slave_0_read;
  wire    [ 15: 0] musiccontroller_0_avalon_slave_0_readdata_from_sa;
  reg                 musiccontroller_0_avalon_slave_0_reg_firsttransfer;
  wire                musiccontroller_0_avalon_slave_0_reset_n;
  reg                 musiccontroller_0_avalon_slave_0_slavearbiterlockenable;
  wire                musiccontroller_0_avalon_slave_0_slavearbiterlockenable2;
  wire                musiccontroller_0_avalon_slave_0_unreg_firsttransfer;
  wire                musiccontroller_0_avalon_slave_0_waits_for_read;
  wire                musiccontroller_0_avalon_slave_0_waits_for_write;
  wire                musiccontroller_0_avalon_slave_0_write;
  wire    [ 15: 0] musiccontroller_0_avalon_slave_0_writedata;
  wire                                                [               24:                0]
shifted_address_to_musiccontroller_0_avalon_slave_0_from_cpu_0_data_master;
  wire                wait_for_musiccontroller_0_avalon_slave_0_counter;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
```

```
            d1_reasons_to_wait <= 0;
        else
          d1_reasons_to_wait <= ~musiccontroller_0_avalon_slave_0_end_xfer;
      end


  assign musiccontroller_0_avalon_slave_0_begins_xfer = ~d1_reasons_to_wait & ((cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0));
  //assign musiccontroller_0_avalon_slave_0_readdata_from_sa = musiccontroller_0_avalon_slave_0_readdata so that symbol knows where to group signals which may go to master only, which is an e_assign
  assign musiccontroller_0_avalon_slave_0_readdata_from_sa = musiccontroller_0_avalon_slave_0_readdata;

  assign cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0 = ({cpu_0_data_master_address_to_slave[24 : 18] , 18'b0} == 25'h40000) & (cpu_0_data_master_read | cpu_0_data_master_write);
  //musiccontroller_0_avalon_slave_0_arb_share_counter set values, which is an e_mux
  assign musiccontroller_0_avalon_slave_0_arb_share_set_values = (cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0)? 2 :
    1;

  //musiccontroller_0_avalon_slave_0_non_bursting_master_requests mux, which is an e_mux
  assign musiccontroller_0_avalon_slave_0_non_bursting_master_requests = cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0;

  //musiccontroller_0_avalon_slave_0_any_bursting_master_saved_grant mux, which is an e_mux
  assign musiccontroller_0_avalon_slave_0_any_bursting_master_saved_grant = 0;

  //musiccontroller_0_avalon_slave_0_arb_share_counter_next_value assignment, which is an e_assign
  assign musiccontroller_0_avalon_slave_0_arb_share_counter_next_value = musiccontroller_0_avalon_slave_0_firsttransfer ? (musiccontroller_0_avalon_slave_0_arb_share_set_values - 1) : |musiccontroller_0_avalon_slave_0_arb_share_counter ? (musiccontroller_0_avalon_slave_0_arb_share_counter - 1) : 0;

  //musiccontroller_0_avalon_slave_0_allgrants all slave grants, which is an e_mux
  assign musiccontroller_0_avalon_slave_0_allgrants = |musiccontroller_0_avalon_slave_0_grant_vector;

  //musiccontroller_0_avalon_slave_0_end_xfer assignment, which is an e_assign
  assign musiccontroller_0_avalon_slave_0_end_xfer = ~(musiccontroller_0_avalon_slave_0_waits_for_read | musiccontroller_0_avalon_slave_0_waits_for_write);

  //end_xfer_arb_share_counter_term_musiccontroller_0_avalon_slave_0 arb share counter enable term, which is an e_assign
  assign end_xfer_arb_share_counter_term_musiccontroller_0_avalon_slave_0 = musiccontroller_0_avalon_slave_0_end_xfer & (~musiccontroller_0_avalon_slave_0_any_bursting_master_saved_grant | in_a_read_cycle | in_a_write_cycle);

  //musiccontroller_0_avalon_slave_0_arb_share_counter arbitration counter enable, which is an e_assign
  assign musiccontroller_0_avalon_slave_0_arb_counter_enable = (end_xfer_arb_share_counter_term_musiccontroller_0_avalon_slave_0 &
```

```
musiccontroller_0_avalon_slave_0_allgrants)                                    |
(end_xfer_arb_share_counter_term_musiccontroller_0_avalon_slave_0              &
~musiccontroller_0_avalon_slave_0_non_bursting_master_requests);

  //musiccontroller_0_avalon_slave_0_arb_share_counter counter, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          musiccontroller_0_avalon_slave_0_arb_share_counter <= 0;
      else if (musiccontroller_0_avalon_slave_0_arb_counter_enable)
          musiccontroller_0_avalon_slave_0_arb_share_counter                   <=
musiccontroller_0_avalon_slave_0_arb_share_counter_next_value;
    end


  //musiccontroller_0_avalon_slave_0_slavearbiterlockenable slave enables arbiterlock, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          musiccontroller_0_avalon_slave_0_slavearbiterlockenable <= 0;
      else if (({|musiccontroller_0_avalon_slave_0_master_qreq_vector &
end_xfer_arb_share_counter_term_musiccontroller_0_avalon_slave_0)              |
(end_xfer_arb_share_counter_term_musiccontroller_0_avalon_slave_0              &
~musiccontroller_0_avalon_slave_0_non_bursting_master_requests))
          musiccontroller_0_avalon_slave_0_slavearbiterlockenable              <=
|musiccontroller_0_avalon_slave_0_arb_share_counter_next_value;
    end


  //cpu_0/data_master musiccontroller_0/avalon_slave_0 arbiterlock, which is an e_assign
  assign                                cpu_0_data_master_arbiterlock          =
musiccontroller_0_avalon_slave_0_slavearbiterlockenable                        &
cpu_0_data_master_continuerequest;

  //musiccontroller_0_avalon_slave_0_slavearbiterlockenable2 slave enables arbiterlock2, which is an e_assign
  assign                musiccontroller_0_avalon_slave_0_slavearbiterlockenable2 =
|musiccontroller_0_avalon_slave_0_arb_share_counter_next_value;

  //cpu_0/data_master musiccontroller_0/avalon_slave_0 arbiterlock2, which is an e_assign
  assign                               cpu_0_data_master_arbiterlock2          =
musiccontroller_0_avalon_slave_0_slavearbiterlockenable2                       &
cpu_0_data_master_continuerequest;

  //musiccontroller_0_avalon_slave_0_any_continuerequest at least one master continues requesting, which is an e_assign
  assign musiccontroller_0_avalon_slave_0_any_continuerequest = 1;

  //cpu_0_data_master_continuerequest continued request, which is an e_assign
  assign cpu_0_data_master_continuerequest = 1;

  assign        cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0 =
cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0                    &
~(((~cpu_0_data_master_waitrequest   |   cpu_0_data_master_no_byte_enables_and_last_term
|               !cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0)          &
cpu_0_data_master_write));
  //musiccontroller_0_avalon_slave_0_writedata mux, which is an e_mux
```

```
  assign musiccontroller_0_avalon_slave_0_writedata = cpu_0_data_master_dbs_write_16;

  //master is always granted when requested
  assign cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0 = cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0;

  //cpu_0/data_master saved-grant musiccontroller_0/avalon_slave_0, which is an e_assign
  assign cpu_0_data_master_saved_grant_musiccontroller_0_avalon_slave_0 = cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0;

  //allow new arb cycle for musiccontroller_0/avalon_slave_0, which is an e_assign
  assign musiccontroller_0_avalon_slave_0_allow_new_arb_cycle = 1;

  //placeholder chosen master
  assign musiccontroller_0_avalon_slave_0_grant_vector = 1;

  //placeholder vector of master qualified-requests
  assign musiccontroller_0_avalon_slave_0_master_qreq_vector = 1;

  //musiccontroller_0_avalon_slave_0_reset_n assignment, which is an e_assign
  assign musiccontroller_0_avalon_slave_0_reset_n = reset_n;

  assign musiccontroller_0_avalon_slave_0_chipselect = cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0;
  //musiccontroller_0_avalon_slave_0_firsttransfer first transaction, which is an e_assign
  assign musiccontroller_0_avalon_slave_0_firsttransfer = musiccontroller_0_avalon_slave_0_begins_xfer ? musiccontroller_0_avalon_slave_0_unreg_firsttransfer : musiccontroller_0_avalon_slave_0_reg_firsttransfer;

  //musiccontroller_0_avalon_slave_0_unreg_firsttransfer first transaction, which is an e_assign
  assign musiccontroller_0_avalon_slave_0_unreg_firsttransfer = ~(musiccontroller_0_avalon_slave_0_slavearbiterlockenable & musiccontroller_0_avalon_slave_0_any_continuerequest);

  //musiccontroller_0_avalon_slave_0_reg_firsttransfer first transaction, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          musiccontroller_0_avalon_slave_0_reg_firsttransfer <= 1'b1;
      else if (musiccontroller_0_avalon_slave_0_begins_xfer)
          musiccontroller_0_avalon_slave_0_reg_firsttransfer <= musiccontroller_0_avalon_slave_0_unreg_firsttransfer;
    end


  //musiccontroller_0_avalon_slave_0_beginbursttransfer_internal begin burst transfer, which is an e_assign
  assign musiccontroller_0_avalon_slave_0_beginbursttransfer_internal = musiccontroller_0_avalon_slave_0_begins_xfer;

  //musiccontroller_0_avalon_slave_0_read assignment, which is an e_mux
  assign musiccontroller_0_avalon_slave_0_read = cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0 & cpu_0_data_master_read;

  //musiccontroller_0_avalon_slave_0_write assignment, which is an e_mux
  assign musiccontroller_0_avalon_slave_0_write = cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0 & cpu_0_data_master_write;
```

```
  assign shifted_address_to_musiccontroller_0_avalon_slave_0_from_cpu_0_data_master =
{cpu_0_data_master_address_to_slave >> 2,
    cpu_0_data_master_dbs_address[1],
    {1 {1'b0}}};

  //musiccontroller_0_avalon_slave_0_address mux, which is an e_mux
  assign musiccontroller_0_avalon_slave_0_address =
shifted_address_to_musiccontroller_0_avalon_slave_0_from_cpu_0_data_master >> 1;

  //d1_musiccontroller_0_avalon_slave_0_end_xfer register, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_musiccontroller_0_avalon_slave_0_end_xfer <= 1;
      else
        d1_musiccontroller_0_avalon_slave_0_end_xfer <=
musiccontroller_0_avalon_slave_0_end_xfer;
    end


  //musiccontroller_0_avalon_slave_0_waits_for_read in a cycle, which is an e_mux
  assign musiccontroller_0_avalon_slave_0_waits_for_read =
musiccontroller_0_avalon_slave_0_in_a_read_cycle &
musiccontroller_0_avalon_slave_0_begins_xfer;

  //musiccontroller_0_avalon_slave_0_in_a_read_cycle assignment, which is an e_assign
  assign musiccontroller_0_avalon_slave_0_in_a_read_cycle =
cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0 & cpu_0_data_master_read;

  //in_a_read_cycle assignment, which is an e_mux
  assign in_a_read_cycle = musiccontroller_0_avalon_slave_0_in_a_read_cycle;

  //musiccontroller_0_avalon_slave_0_waits_for_write in a cycle, which is an e_mux
  assign musiccontroller_0_avalon_slave_0_waits_for_write =
musiccontroller_0_avalon_slave_0_in_a_write_cycle & 0;

  //musiccontroller_0_avalon_slave_0_in_a_write_cycle assignment, which is an e_assign
  assign musiccontroller_0_avalon_slave_0_in_a_write_cycle =
cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0 & cpu_0_data_master_write;

  //in_a_write_cycle assignment, which is an e_mux
  assign in_a_write_cycle = musiccontroller_0_avalon_slave_0_in_a_write_cycle;

  assign wait_for_musiccontroller_0_avalon_slave_0_counter = 0;
  assign {cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0_segment_1,
cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0_segment_0} =
cpu_0_data_master_byteenable;
  assign cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0 =
((cpu_0_data_master_dbs_address[1] == 0))?
cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0_segment_0 :
    cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0_segment_1;

  //assign musiccontroller_0_avalon_slave_0_irq_from_sa =
musiccontroller_0_avalon_slave_0_irq so that symbol knows where to group signals which may
go to master only, which is an e_assign
  assign musiccontroller_0_avalon_slave_0_irq_from_sa =
musiccontroller_0_avalon_slave_0_irq;
```

```
//synthesis translate_off
//////////////// SIMULATION-ONLY CONTENTS
   //musiccontroller_0/avalon_slave_0 enable non-zero assertions, which is an e_register
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               enable_nonzero_assertions <= 0;
         else
            enable_nonzero_assertions <= 1'b1;
      end



//////////////// END SIMULATION-ONLY CONTENTS

//synthesis translate_on

endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module rdv_fifo_for_cpu_0_data_master_to_sdram_0_s1_module (
                                                             // inputs:
                                                               clear_fifo,
                                                               clk,
                                                               data_in,
                                                               read,
                                                               reset_n,
                                                               sync_reset,
                                                               write,

                                                             // outputs:
                                                               data_out,
                                                               empty,

fifo_contains_ones_n,
                                                               full
                                                            )
;

   output           data_out;
   output           empty;
   output           fifo_contains_ones_n;
   output           full;
   input            clear_fifo;
   input            clk;
   input            data_in;
   input            read;
   input            reset_n;
```

```
input                   sync_reset;
input                   write;

wire                    data_out;
wire                    empty;
reg                     fifo_contains_ones_n;
wire                    full;
reg                     full_0;
reg                     full_1;
reg                     full_2;
reg                     full_3;
reg                     full_4;
reg                     full_5;
reg                     full_6;
wire                    full_7;
reg       [   3: 0] how_many_ones;
wire      [   3: 0] one_count_minus_one;
wire      [   3: 0] one_count_plus_one;
wire                    p0_full_0;
wire                    p0_stage_0;
wire                    p1_full_1;
wire                    p1_stage_1;
wire                    p2_full_2;
wire                    p2_stage_2;
wire                    p3_full_3;
wire                    p3_stage_3;
wire                    p4_full_4;
wire                    p4_stage_4;
wire                    p5_full_5;
wire                    p5_stage_5;
wire                    p6_full_6;
wire                    p6_stage_6;
reg                     stage_0;
reg                     stage_1;
reg                     stage_2;
reg                     stage_3;
reg                     stage_4;
reg                     stage_5;
reg                     stage_6;
wire      [   3: 0] updated_one_count;
assign data_out = stage_0;
assign full = full_6;
assign empty = !full_0;
assign full_7 = 0;
//data_6, which is an e_mux
assign p6_stage_6 = ((full_7 & ~clear_fifo) == 0)? data_in :
   data_in;

//data_reg_6, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            stage_6 <= 0;
      else if (clear_fifo | sync_reset | read | (write & !full_6))
            if (sync_reset & full_6 & !((full_7 == 0) & read & write))
                  stage_6 <= 0;
            else
               stage_6 <= p6_stage_6;
```

```
    end


//control_6, which is an e_mux
assign p6_full_6 = ((read & !write) == 0)? full_5 :
    0;

//control_reg_6, which is an e_register
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            full_6 <= 0;
        else if (clear_fifo | (read ^ write) | (write & !full_0))
            if (clear_fifo)
                full_6 <= 0;
            else
                full_6 <= p6_full_6;
    end


//data_5, which is an e_mux
assign p5_stage_5 = ((full_6 & ~clear_fifo) == 0)? data_in :
    stage_6;

//data_reg_5, which is an e_register
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            stage_5 <= 0;
        else if (clear_fifo | sync_reset | read | (write & !full_5))
            if (sync_reset & full_5 & !((full_6 == 0) & read & write))
                stage_5 <= 0;
            else
                stage_5 <= p5_stage_5;
    end


//control_5, which is an e_mux
assign p5_full_5 = ((read & !write) == 0)? full_4 :
    full_6;

//control_reg_5, which is an e_register
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            full_5 <= 0;
        else if (clear_fifo | (read ^ write) | (write & !full_0))
            if (clear_fifo)
                full_5 <= 0;
            else
                full_5 <= p5_full_5;
    end


//data_4, which is an e_mux
assign p4_stage_4 = ((full_5 & ~clear_fifo) == 0)? data_in :
    stage_5;
```

```
//data_reg_4, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            stage_4 <= 0;
      else if (clear_fifo | sync_reset | read | (write & !full_4))
            if (sync_reset & full_4 & !((full_5 == 0) & read & write))
                  stage_4 <= 0;
            else
               stage_4 <= p4_stage_4;
   end


//control_4, which is an e_mux
assign p4_full_4 = ((read & !write) == 0)? full_3 :
   full_5;

//control_reg_4, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            full_4 <= 0;
      else if (clear_fifo | (read ^ write) | (write & !full_0))
            if (clear_fifo)
                  full_4 <= 0;
            else
               full_4 <= p4_full_4;
   end


//data_3, which is an e_mux
assign p3_stage_3 = ((full_4 & ~clear_fifo) == 0)? data_in :
   stage_4;

//data_reg_3, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            stage_3 <= 0;
      else if (clear_fifo | sync_reset | read | (write & !full_3))
            if (sync_reset & full_3 & !((full_4 == 0) & read & write))
                  stage_3 <= 0;
            else
               stage_3 <= p3_stage_3;
   end


//control_3, which is an e_mux
assign p3_full_3 = ((read & !write) == 0)? full_2 :
   full_4;

//control_reg_3, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            full_3 <= 0;
      else if (clear_fifo | (read ^ write) | (write & !full_0))
            if (clear_fifo)
```

```
                full_3 <= 0;
            else
                full_3 <= p3_full_3;
    end


//data_2, which is an e_mux
assign p2_stage_2 = ((full_3 & ~clear_fifo) == 0)? data_in :
    stage_3;

//data_reg_2, which is an e_register
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            stage_2 <= 0;
        else if (clear_fifo | sync_reset | read | (write & !full_2))
            if (sync_reset & full_2 & !((full_3 == 0) & read & write))
                stage_2 <= 0;
            else
                stage_2 <= p2_stage_2;
    end


//control_2, which is an e_mux
assign p2_full_2 = ((read & !write) == 0)? full_1 :
    full_3;

//control_reg_2, which is an e_register
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            full_2 <= 0;
        else if (clear_fifo | (read ^ write) | (write & !full_0))
            if (clear_fifo)
                full_2 <= 0;
            else
                full_2 <= p2_full_2;
    end


//data_1, which is an e_mux
assign p1_stage_1 = ((full_2 & ~clear_fifo) == 0)? data_in :
    stage_2;

//data_reg_1, which is an e_register
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            stage_1 <= 0;
        else if (clear_fifo | sync_reset | read | (write & !full_1))
            if (sync_reset & full_1 & !((full_2 == 0) & read & write))
                stage_1 <= 0;
            else
                stage_1 <= p1_stage_1;
    end


//control_1, which is an e_mux
```

```
assign p1_full_1 = ((read & !write) == 0)? full_0 :
   full_2;

//control_reg_1, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            full_1 <= 0;
      else if (clear_fifo | (read ^ write) | (write & !full_0))
            if (clear_fifo)
                  full_1 <= 0;
            else
               full_1 <= p1_full_1;
   end


//data_0, which is an e_mux
assign p0_stage_0 = ((full_1 & ~clear_fifo) == 0)? data_in :
   stage_1;

//data_reg_0, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            stage_0 <= 0;
      else if (clear_fifo | sync_reset | read | (write & !full_0))
            if (sync_reset & full_0 & !((full_1 == 0) & read & write))
                  stage_0 <= 0;
            else
               stage_0 <= p0_stage_0;
   end


//control_0, which is an e_mux
assign p0_full_0 = ((read & !write) == 0)? 1 :
   full_1;

//control_reg_0, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            full_0 <= 0;
      else if (clear_fifo | (read ^ write) | (write & !full_0))
            if (clear_fifo & ~write)
                  full_0 <= 0;
            else
               full_0 <= p0_full_0;
   end


assign one_count_plus_one = how_many_ones + 1;
assign one_count_minus_one = how_many_ones - 1;
//updated_one_count, which is an e_mux
assign updated_one_count = ((((clear_fifo | sync_reset) & !write)))? 0 :
   ((((clear_fifo | sync_reset) & write)))? |data_in :
   ((read & (|data_in) & write & (|stage_0)))? how_many_ones :
   ((write & (|data_in)))? one_count_plus_one :
   ((read & (|stage_0)))? one_count_minus_one :
```

```
    how_many_ones;

  //counts how many ones in the data pipeline, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          how_many_ones <= 0;
      else if (clear_fifo | sync_reset | read | write)
          how_many_ones <= updated_one_count;
    end


  //this fifo contains ones in the data pipeline, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          fifo_contains_ones_n <= 1;
      else if (clear_fifo | sync_reset | read | write)
          fifo_contains_ones_n <= ~(|updated_one_count);
    end



endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module rdv_fifo_for_cpu_0_instruction_master_to_sdram_0_s1_module (
                                                                    // inputs:
                                                                      clear_fifo,
                                                                      clk,
                                                                      data_in,
                                                                      read,
                                                                      reset_n,
                                                                      sync_reset,
                                                                      write,

                                                                    // outputs:
                                                                      data_out,
                                                                      empty,

fifo_contains_ones_n,

                                                                      full
                                                                   )
;

  output           data_out;
  output           empty;
  output           fifo_contains_ones_n;
  output           full;
  input            clear_fifo;
```

```
input                   clk;
input                   data_in;
input                   read;
input                   reset_n;
input                   sync_reset;
input                   write;

wire                    data_out;
wire                    empty;
reg                     fifo_contains_ones_n;
wire                    full;
reg                     full_0;
reg                     full_1;
reg                     full_2;
reg                     full_3;
reg                     full_4;
reg                     full_5;
reg                     full_6;
wire                    full_7;
reg         [   3: 0] how_many_ones;
wire        [   3: 0] one_count_minus_one;
wire        [   3: 0] one_count_plus_one;
wire                    p0_full_0;
wire                    p0_stage_0;
wire                    p1_full_1;
wire                    p1_stage_1;
wire                    p2_full_2;
wire                    p2_stage_2;
wire                    p3_full_3;
wire                    p3_stage_3;
wire                    p4_full_4;
wire                    p4_stage_4;
wire                    p5_full_5;
wire                    p5_stage_5;
wire                    p6_full_6;
wire                    p6_stage_6;
reg                     stage_0;
reg                     stage_1;
reg                     stage_2;
reg                     stage_3;
reg                     stage_4;
reg                     stage_5;
reg                     stage_6;
wire        [   3: 0] updated_one_count;
assign data_out = stage_0;
assign full = full_6;
assign empty = !full_0;
assign full_7 = 0;
//data_6, which is an e_mux
assign p6_stage_6 = ((full_7 & ~clear_fifo) == 0)? data_in :
  data_in;

//data_reg_6, which is an e_register
always @(posedge clk or negedge reset_n)
  begin
    if (reset_n == 0)
        stage_6 <= 0;
    else if (clear_fifo | sync_reset | read | (write & !full_6))
```

```
            if (sync_reset & full_6 & !((full_7 == 0) & read & write))
                stage_6 <= 0;
            else
              stage_6 <= p6_stage_6;
   end


//control_6, which is an e_mux
assign p6_full_6 = ((read & !write) == 0)? full_5 :
   0;

//control_reg_6, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            full_6 <= 0;
      else if (clear_fifo | (read ^ write) | (write & !full_0))
            if (clear_fifo)
                full_6 <= 0;
            else
              full_6 <= p6_full_6;
   end


//data_5, which is an e_mux
assign p5_stage_5 = ((full_6 & ~clear_fifo) == 0)? data_in :
   stage_6;

//data_reg_5, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            stage_5 <= 0;
      else if (clear_fifo | sync_reset | read | (write & !full_5))
            if (sync_reset & full_5 & !((full_6 == 0) & read & write))
                stage_5 <= 0;
            else
              stage_5 <= p5_stage_5;
   end


//control_5, which is an e_mux
assign p5_full_5 = ((read & !write) == 0)? full_4 :
   full_6;

//control_reg_5, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            full_5 <= 0;
      else if (clear_fifo | (read ^ write) | (write & !full_0))
            if (clear_fifo)
                full_5 <= 0;
            else
              full_5 <= p5_full_5;
   end
```

```
//data_4, which is an e_mux
assign p4_stage_4 = ((full_5 & ~clear_fifo) == 0)? data_in :
   stage_5;

//data_reg_4, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            stage_4 <= 0;
      else if (clear_fifo | sync_reset | read | (write & !full_4))
            if (sync_reset & full_4 & !((full_5 == 0) & read & write))
                  stage_4 <= 0;
            else
               stage_4 <= p4_stage_4;
   end


//control_4, which is an e_mux
assign p4_full_4 = ((read & !write) == 0)? full_3 :
   full_5;

//control_reg_4, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            full_4 <= 0;
      else if (clear_fifo | (read ^ write) | (write & !full_0))
            if (clear_fifo)
                  full_4 <= 0;
            else
               full_4 <= p4_full_4;
   end


//data_3, which is an e_mux
assign p3_stage_3 = ((full_4 & ~clear_fifo) == 0)? data_in :
   stage_4;

//data_reg_3, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            stage_3 <= 0;
      else if (clear_fifo | sync_reset | read | (write & !full_3))
            if (sync_reset & full_3 & !((full_4 == 0) & read & write))
                  stage_3 <= 0;
            else
               stage_3 <= p3_stage_3;
   end


//control_3, which is an e_mux
assign p3_full_3 = ((read & !write) == 0)? full_2 :
   full_4;

//control_reg_3, which is an e_register
always @(posedge clk or negedge reset_n)
   begin
```

```
    if (reset_n == 0)
        full_3 <= 0;
    else if (clear_fifo | (read ^ write) | (write & !full_0))
        if (clear_fifo)
            full_3 <= 0;
        else
          full_3 <= p3_full_3;
  end


//data_2, which is an e_mux
assign p2_stage_2 = ((full_3 & ~clear_fifo) == 0)? data_in :
  stage_3;

//data_reg_2, which is an e_register
always @(posedge clk or negedge reset_n)
  begin
    if (reset_n == 0)
        stage_2 <= 0;
    else if (clear_fifo | sync_reset | read | (write & !full_2))
        if (sync_reset & full_2 & !((full_3 == 0) & read & write))
            stage_2 <= 0;
        else
          stage_2 <= p2_stage_2;
  end


//control_2, which is an e_mux
assign p2_full_2 = ((read & !write) == 0)? full_1 :
  full_3;

//control_reg_2, which is an e_register
always @(posedge clk or negedge reset_n)
  begin
    if (reset_n == 0)
        full_2 <= 0;
    else if (clear_fifo | (read ^ write) | (write & !full_0))
        if (clear_fifo)
            full_2 <= 0;
        else
          full_2 <= p2_full_2;
  end


//data_1, which is an e_mux
assign p1_stage_1 = ((full_2 & ~clear_fifo) == 0)? data_in :
  stage_2;

//data_reg_1, which is an e_register
always @(posedge clk or negedge reset_n)
  begin
    if (reset_n == 0)
        stage_1 <= 0;
    else if (clear_fifo | sync_reset | read | (write & !full_1))
        if (sync_reset & full_1 & !((full_2 == 0) & read & write))
            stage_1 <= 0;
        else
          stage_1 <= p1_stage_1;
```

```
    end


//control_1, which is an e_mux
assign p1_full_1 = ((read & !write) == 0)? full_0 :
    full_2;

//control_reg_1, which is an e_register
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            full_1 <= 0;
        else if (clear_fifo | (read ^ write) | (write & !full_0))
            if (clear_fifo)
                full_1 <= 0;
            else
                full_1 <= p1_full_1;
    end


//data_0, which is an e_mux
assign p0_stage_0 = ((full_1 & ~clear_fifo) == 0)? data_in :
    stage_1;

//data_reg_0, which is an e_register
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            stage_0 <= 0;
        else if (clear_fifo | sync_reset | read | (write & !full_0))
            if (sync_reset & full_0 & !((full_1 == 0) & read & write))
                stage_0 <= 0;
            else
                stage_0 <= p0_stage_0;
    end


//control_0, which is an e_mux
assign p0_full_0 = ((read & !write) == 0)? 1 :
    full_1;

//control_reg_0, which is an e_register
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            full_0 <= 0;
        else if (clear_fifo | (read ^ write) | (write & !full_0))
            if (clear_fifo & ~write)
                full_0 <= 0;
            else
                full_0 <= p0_full_0;
    end


assign one_count_plus_one = how_many_ones + 1;
assign one_count_minus_one = how_many_ones - 1;
//updated_one_count, which is an e_mux
assign updated_one_count = ((((clear_fifo | sync_reset) & !write)))? 0 :
```

```
    ((((clear_fifo | sync_reset) & write)))? |data_in :
    ((read & (|data_in) & write & (|stage_0)))? how_many_ones :
    ((write & (|data_in)))? one_count_plus_one :
    ((read & (|stage_0)))? one_count_minus_one :
    how_many_ones;

  //counts how many ones in the data pipeline, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          how_many_ones <= 0;
      else if (clear_fifo | sync_reset | read | write)
          how_many_ones <= updated_one_count;
    end


  //this fifo contains ones in the data pipeline, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          fifo_contains_ones_n <= 1;
      else if (clear_fifo | sync_reset | read | write)
          fifo_contains_ones_n <= ~(|updated_one_count);
    end



endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module sdram_0_s1_arbitrator (
                               // inputs:
                                 clk,
                                 cpu_0_data_master_address_to_slave,
                                 cpu_0_data_master_byteenable,
                                 cpu_0_data_master_dbs_address,
                                 cpu_0_data_master_dbs_write_16,
                                 cpu_0_data_master_no_byte_enables_and_last_term,
                                 cpu_0_data_master_read,
                                 cpu_0_data_master_waitrequest,
                                 cpu_0_data_master_write,
                                 cpu_0_instruction_master_address_to_slave,
                                 cpu_0_instruction_master_dbs_address,
                                 cpu_0_instruction_master_read,
                                 reset_n,
                                 sdram_0_s1_readdata,
                                 sdram_0_s1_readdatavalid,
                                 sdram_0_s1_waitrequest,

                               // outputs:
```

```
                                        cpu_0_data_master_byteenable_sdram_0_s1,
                                        cpu_0_data_master_granted_sdram_0_s1,
                                        cpu_0_data_master_qualified_request_sdram_0_s1,
                                        cpu_0_data_master_read_data_valid_sdram_0_s1,

cpu_0_data_master_read_data_valid_sdram_0_s1_shift_register,
                                        cpu_0_data_master_requests_sdram_0_s1,
                                        cpu_0_instruction_master_granted_sdram_0_s1,

cpu_0_instruction_master_qualified_request_sdram_0_s1,
                                        cpu_0_instruction_master_read_data_valid_sdram_0_s1,

cpu_0_instruction_master_read_data_valid_sdram_0_s1_shift_register,
                                        cpu_0_instruction_master_requests_sdram_0_s1,
                                        d1_sdram_0_s1_end_xfer,
                                        sdram_0_s1_address,
                                        sdram_0_s1_byteenable_n,
                                        sdram_0_s1_chipselect,
                                        sdram_0_s1_read_n,
                                        sdram_0_s1_readdata_from_sa,
                                        sdram_0_s1_reset_n,
                                        sdram_0_s1_waitrequest_from_sa,
                                        sdram_0_s1_write_n,
                                        sdram_0_s1_writedata
                                    )
;

  output  [  1: 0] cpu_0_data_master_byteenable_sdram_0_s1;
  output           cpu_0_data_master_granted_sdram_0_s1;
  output           cpu_0_data_master_qualified_request_sdram_0_s1;
  output           cpu_0_data_master_read_data_valid_sdram_0_s1;
  output           cpu_0_data_master_read_data_valid_sdram_0_s1_shift_register;
  output           cpu_0_data_master_requests_sdram_0_s1;
  output           cpu_0_instruction_master_granted_sdram_0_s1;
  output           cpu_0_instruction_master_qualified_request_sdram_0_s1;
  output           cpu_0_instruction_master_read_data_valid_sdram_0_s1;
  output           cpu_0_instruction_master_read_data_valid_sdram_0_s1_shift_register;
  output           cpu_0_instruction_master_requests_sdram_0_s1;
  output           d1_sdram_0_s1_end_xfer;
  output  [ 21: 0] sdram_0_s1_address;
  output  [  1: 0] sdram_0_s1_byteenable_n;
  output           sdram_0_s1_chipselect;
  output           sdram_0_s1_read_n;
  output  [ 15: 0] sdram_0_s1_readdata_from_sa;
  output           sdram_0_s1_reset_n;
  output           sdram_0_s1_waitrequest_from_sa;
  output           sdram_0_s1_write_n;
  output  [ 15: 0] sdram_0_s1_writedata;
  input            clk;
  input   [ 24: 0] cpu_0_data_master_address_to_slave;
  input   [  3: 0] cpu_0_data_master_byteenable;
  input   [  1: 0] cpu_0_data_master_dbs_address;
  input   [ 15: 0] cpu_0_data_master_dbs_write_16;
  input            cpu_0_data_master_no_byte_enables_and_last_term;
  input            cpu_0_data_master_read;
  input            cpu_0_data_master_waitrequest;
  input            cpu_0_data_master_write;
  input   [ 24: 0] cpu_0_instruction_master_address_to_slave;
```

```
input     [  1: 0] cpu_0_instruction_master_dbs_address;
input              cpu_0_instruction_master_read;
input              reset_n;
input     [ 15: 0] sdram_0_s1_readdata;
input              sdram_0_s1_readdatavalid;
input              sdram_0_s1_waitrequest;

wire               cpu_0_data_master_arbiterlock;
wire               cpu_0_data_master_arbiterlock2;
wire      [  1: 0] cpu_0_data_master_byteenable_sdram_0_s1;
wire      [  1: 0] cpu_0_data_master_byteenable_sdram_0_s1_segment_0;
wire      [  1: 0] cpu_0_data_master_byteenable_sdram_0_s1_segment_1;
wire               cpu_0_data_master_continuerequest;
wire               cpu_0_data_master_granted_sdram_0_s1;
wire               cpu_0_data_master_qualified_request_sdram_0_s1;
wire               cpu_0_data_master_rdv_fifo_empty_sdram_0_s1;
wire               cpu_0_data_master_rdv_fifo_output_from_sdram_0_s1;
wire               cpu_0_data_master_read_data_valid_sdram_0_s1;
wire               cpu_0_data_master_read_data_valid_sdram_0_s1_shift_register;
wire               cpu_0_data_master_requests_sdram_0_s1;
wire               cpu_0_data_master_saved_grant_sdram_0_s1;
wire               cpu_0_instruction_master_arbiterlock;
wire               cpu_0_instruction_master_arbiterlock2;
wire               cpu_0_instruction_master_continuerequest;
wire               cpu_0_instruction_master_granted_sdram_0_s1;
wire               cpu_0_instruction_master_qualified_request_sdram_0_s1;
wire               cpu_0_instruction_master_rdv_fifo_empty_sdram_0_s1;
wire               cpu_0_instruction_master_rdv_fifo_output_from_sdram_0_s1;
wire               cpu_0_instruction_master_read_data_valid_sdram_0_s1;
wire               cpu_0_instruction_master_read_data_valid_sdram_0_s1_shift_register;
wire               cpu_0_instruction_master_requests_sdram_0_s1;
wire               cpu_0_instruction_master_saved_grant_sdram_0_s1;
reg                d1_reasons_to_wait;
reg                d1_sdram_0_s1_end_xfer;
reg                enable_nonzero_assertions;
wire               end_xfer_arb_share_counter_term_sdram_0_s1;
wire               in_a_read_cycle;
wire               in_a_write_cycle;
reg                last_cycle_cpu_0_data_master_granted_slave_sdram_0_s1;
reg                last_cycle_cpu_0_instruction_master_granted_slave_sdram_0_s1;
wire      [ 21: 0] sdram_0_s1_address;
wire               sdram_0_s1_allgrants;
wire               sdram_0_s1_allow_new_arb_cycle;
wire               sdram_0_s1_any_bursting_master_saved_grant;
wire               sdram_0_s1_any_continuerequest;
reg       [  1: 0] sdram_0_s1_arb_addend;
wire               sdram_0_s1_arb_counter_enable;
reg       [  1: 0] sdram_0_s1_arb_share_counter;
wire      [  1: 0] sdram_0_s1_arb_share_counter_next_value;
wire      [  1: 0] sdram_0_s1_arb_share_set_values;
wire      [  1: 0] sdram_0_s1_arb_winner;
wire               sdram_0_s1_arbitration_holdoff_internal;
wire               sdram_0_s1_beginbursttransfer_internal;
wire               sdram_0_s1_begins_xfer;
wire      [  1: 0] sdram_0_s1_byteenable_n;
wire               sdram_0_s1_chipselect;
wire      [  3: 0] sdram_0_s1_chosen_master_double_vector;
wire      [  1: 0] sdram_0_s1_chosen_master_rot_left;
```

```
  wire                    sdram_0_s1_end_xfer;
  wire                    sdram_0_s1_firsttransfer;
  wire      [  1: 0] sdram_0_s1_grant_vector;
  wire                    sdram_0_s1_in_a_read_cycle;
  wire                    sdram_0_s1_in_a_write_cycle;
  wire      [  1: 0] sdram_0_s1_master_qreq_vector;
  wire                    sdram_0_s1_move_on_to_next_transaction;
  wire                    sdram_0_s1_non_bursting_master_requests;
  wire                    sdram_0_s1_read_n;
  wire      [ 15: 0] sdram_0_s1_readdata_from_sa;
  wire                    sdram_0_s1_readdatavalid_from_sa;
  reg                     sdram_0_s1_reg_firsttransfer;
  wire                    sdram_0_s1_reset_n;
  reg       [  1: 0] sdram_0_s1_saved_chosen_master_vector;
  reg                     sdram_0_s1_slavearbiterlockenable;
  wire                    sdram_0_s1_slavearbiterlockenable2;
  wire                    sdram_0_s1_unreg_firsttransfer;
  wire                    sdram_0_s1_waitrequest_from_sa;
  wire                    sdram_0_s1_waits_for_read;
  wire                    sdram_0_s1_waits_for_write;
  wire                    sdram_0_s1_write_n;
  wire      [ 15: 0] sdram_0_s1_writedata;
  wire      [ 24: 0] shifted_address_to_sdram_0_s1_from_cpu_0_data_master;
  wire      [ 24: 0] shifted_address_to_sdram_0_s1_from_cpu_0_instruction_master;
  wire                    wait_for_sdram_0_s1_counter;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_reasons_to_wait <= 0;
      else
        d1_reasons_to_wait <= ~sdram_0_s1_end_xfer;
    end


  assign sdram_0_s1_begins_xfer = ~d1_reasons_to_wait &
((cpu_0_data_master_qualified_request_sdram_0_s1 |
cpu_0_instruction_master_qualified_request_sdram_0_s1));
  //assign sdram_0_s1_readdata_from_sa = sdram_0_s1_readdata so that symbol knows where
to group signals which may go to master only, which is an e_assign
  assign sdram_0_s1_readdata_from_sa = sdram_0_s1_readdata;

  assign cpu_0_data_master_requests_sdram_0_s1 =
({cpu_0_data_master_address_to_slave[24 : 23] , 23'b0} == 25'h800000) &
(cpu_0_data_master_read | cpu_0_data_master_write);
  //assign sdram_0_s1_waitrequest_from_sa = sdram_0_s1_waitrequest so that symbol knows
where to group signals which may go to master only, which is an e_assign
  assign sdram_0_s1_waitrequest_from_sa = sdram_0_s1_waitrequest;

  //assign sdram_0_s1_readdatavalid_from_sa = sdram_0_s1_readdatavalid so that symbol
knows where to group signals which may go to master only, which is an e_assign
  assign sdram_0_s1_readdatavalid_from_sa = sdram_0_s1_readdatavalid;

  //sdram_0_s1_arb_share_counter set values, which is an e_mux
  assign sdram_0_s1_arb_share_set_values = (cpu_0_data_master_granted_sdram_0_s1)? 2 :
    (cpu_0_instruction_master_granted_sdram_0_s1)? 2 :
    (cpu_0_data_master_granted_sdram_0_s1)? 2 :
    (cpu_0_instruction_master_granted_sdram_0_s1)? 2 :
    1;
```

```
  //sdram_0_s1_non_bursting_master_requests mux, which is an e_mux
  assign sdram_0_s1_non_bursting_master_requests =
cpu_0_data_master_requests_sdram_0_s1 |
    cpu_0_instruction_master_requests_sdram_0_s1 |
    cpu_0_data_master_requests_sdram_0_s1 |
    cpu_0_instruction_master_requests_sdram_0_s1;

  //sdram_0_s1_any_bursting_master_saved_grant mux, which is an e_mux
  assign sdram_0_s1_any_bursting_master_saved_grant = 0;

  //sdram_0_s1_arb_share_counter_next_value assignment, which is an e_assign
  assign sdram_0_s1_arb_share_counter_next_value = sdram_0_s1_firsttransfer ?
(sdram_0_s1_arb_share_set_values - 1) : |sdram_0_s1_arb_share_counter ?
(sdram_0_s1_arb_share_counter - 1) : 0;

  //sdram_0_s1_allgrants all slave grants, which is an e_mux
  assign sdram_0_s1_allgrants = (|sdram_0_s1_grant_vector) |
    (|sdram_0_s1_grant_vector) |
    (|sdram_0_s1_grant_vector) |
    (|sdram_0_s1_grant_vector);

  //sdram_0_s1_end_xfer assignment, which is an e_assign
  assign sdram_0_s1_end_xfer = ~(sdram_0_s1_waits_for_read | sdram_0_s1_waits_for_write);

  //end_xfer_arb_share_counter_term_sdram_0_s1 arb share counter enable term, which is an
e_assign
  assign end_xfer_arb_share_counter_term_sdram_0_s1 = sdram_0_s1_end_xfer &
(~sdram_0_s1_any_bursting_master_saved_grant | in_a_read_cycle | in_a_write_cycle);

  //sdram_0_s1_arb_share_counter arbitration counter enable, which is an e_assign
  assign sdram_0_s1_arb_counter_enable = (end_xfer_arb_share_counter_term_sdram_0_s1 &
sdram_0_s1_allgrants) | (end_xfer_arb_share_counter_term_sdram_0_s1 &
~sdram_0_s1_non_bursting_master_requests);

  //sdram_0_s1_arb_share_counter counter, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          sdram_0_s1_arb_share_counter <= 0;
      else if (sdram_0_s1_arb_counter_enable)
          sdram_0_s1_arb_share_counter <= sdram_0_s1_arb_share_counter_next_value;
    end


  //sdram_0_s1_slavearbiterlockenable slave enables arbiterlock, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          sdram_0_s1_slavearbiterlockenable <= 0;
      else if ((|sdram_0_s1_master_qreq_vector &
end_xfer_arb_share_counter_term_sdram_0_s1) |
(end_xfer_arb_share_counter_term_sdram_0_s1 &
~sdram_0_s1_non_bursting_master_requests))
          sdram_0_s1_slavearbiterlockenable <=
|sdram_0_s1_arb_share_counter_next_value;
    end
```

```
  //cpu_0/data_master sdram_0/s1 arbiterlock, which is an e_assign
  assign cpu_0_data_master_arbiterlock = sdram_0_s1_slavearbiterlockenable & cpu_0_data_master_continuerequest;

  //sdram_0_s1_slavearbiterlockenable2 slave enables arbiterlock2, which is an e_assign
  assign sdram_0_s1_slavearbiterlockenable2 = |sdram_0_s1_arb_share_counter_next_value;

  //cpu_0/data_master sdram_0/s1 arbiterlock2, which is an e_assign
  assign cpu_0_data_master_arbiterlock2 = sdram_0_s1_slavearbiterlockenable2 & cpu_0_data_master_continuerequest;

  //cpu_0/instruction_master sdram_0/s1 arbiterlock, which is an e_assign
  assign cpu_0_instruction_master_arbiterlock = sdram_0_s1_slavearbiterlockenable & cpu_0_instruction_master_continuerequest;

  //cpu_0/instruction_master sdram_0/s1 arbiterlock2, which is an e_assign
  assign cpu_0_instruction_master_arbiterlock2 = sdram_0_s1_slavearbiterlockenable2 & cpu_0_instruction_master_continuerequest;

  //cpu_0/instruction_master granted sdram_0/s1 last time, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          last_cycle_cpu_0_instruction_master_granted_slave_sdram_0_s1 <= 0;
      else
        last_cycle_cpu_0_instruction_master_granted_slave_sdram_0_s1 <= cpu_0_instruction_master_saved_grant_sdram_0_s1 ? 1 : (sdram_0_s1_arbitration_holdoff_internal | ~cpu_0_instruction_master_requests_sdram_0_s1) ? 0 : last_cycle_cpu_0_instruction_master_granted_slave_sdram_0_s1;
    end


  //cpu_0_instruction_master_continuerequest continued request, which is an e_mux
  assign cpu_0_instruction_master_continuerequest = last_cycle_cpu_0_instruction_master_granted_slave_sdram_0_s1 & cpu_0_instruction_master_requests_sdram_0_s1;

  //sdram_0_s1_any_continuerequest at least one master continues requesting, which is an e_mux
  assign sdram_0_s1_any_continuerequest = cpu_0_instruction_master_continuerequest |
    cpu_0_data_master_continuerequest;

  assign cpu_0_data_master_qualified_request_sdram_0_s1 = cpu_0_data_master_requests_sdram_0_s1 & ~((cpu_0_data_master_read & (~cpu_0_data_master_waitrequest | (|cpu_0_data_master_read_data_valid_sdram_0_s1_shift_register))) | ((~cpu_0_data_master_waitrequest | cpu_0_data_master_no_byte_enables_and_last_term | !cpu_0_data_master_byteenable_sdram_0_s1) & cpu_0_data_master_write) | cpu_0_instruction_master_arbiterlock);
  //unique name for sdram_0_s1_move_on_to_next_transaction, which is an e_assign
  assign sdram_0_s1_move_on_to_next_transaction = sdram_0_s1_readdatavalid_from_sa;

  //rdv_fifo_for_cpu_0_data_master_to_sdram_0_s1, which is an e_fifo_with_registered_outputs
  rdv_fifo_for_cpu_0_data_master_to_sdram_0_s1_module rdv_fifo_for_cpu_0_data_master_to_sdram_0_s1
    (
```

```
        .clear_fifo               (1'b0),
        .clk                      (clk),
        .data_in                  (cpu_0_data_master_granted_sdram_0_s1),
        .data_out                 (cpu_0_data_master_rdv_fifo_output_from_sdram_0_s1),
        .empty                    (),
        .fifo_contains_ones_n (cpu_0_data_master_rdv_fifo_empty_sdram_0_s1),
        .full                     (),
        .read                     (sdram_0_s1_move_on_to_next_transaction),
        .reset_n                  (reset_n),
        .sync_reset               (1'b0),
        .write                    (in_a_read_cycle & ~sdram_0_s1_waits_for_read)
      );

  assign cpu_0_data_master_read_data_valid_sdram_0_s1_shift_register =
~cpu_0_data_master_rdv_fifo_empty_sdram_0_s1;
  //local readdatavalid cpu_0_data_master_read_data_valid_sdram_0_s1, which is an e_mux
  assign cpu_0_data_master_read_data_valid_sdram_0_s1 =
(sdram_0_s1_readdatavalid_from_sa & cpu_0_data_master_rdv_fifo_output_from_sdram_0_s1)
& ~ cpu_0_data_master_rdv_fifo_empty_sdram_0_s1;

  //sdram_0_s1_writedata mux, which is an e_mux
  assign sdram_0_s1_writedata = cpu_0_data_master_dbs_write_16;

  assign cpu_0_instruction_master_requests_sdram_0_s1 =
(({cpu_0_instruction_master_address_to_slave[24 : 23] , 23'b0} == 25'h800000) &
(cpu_0_instruction_master_read)) & cpu_0_instruction_master_read;
  //cpu_0/data_master granted sdram_0/s1 last time, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          last_cycle_cpu_0_data_master_granted_slave_sdram_0_s1 <= 0;
      else
        last_cycle_cpu_0_data_master_granted_slave_sdram_0_s1 <=
cpu_0_data_master_saved_grant_sdram_0_s1 ? 1 : (sdram_0_s1_arbitration_holdoff_internal |
~cpu_0_data_master_requests_sdram_0_s1) ? 0 :
last_cycle_cpu_0_data_master_granted_slave_sdram_0_s1;
    end


  //cpu_0_data_master_continuerequest continued request, which is an e_mux
  assign cpu_0_data_master_continuerequest =
last_cycle_cpu_0_data_master_granted_slave_sdram_0_s1 &
cpu_0_data_master_requests_sdram_0_s1;

  assign cpu_0_instruction_master_qualified_request_sdram_0_s1 =
cpu_0_instruction_master_requests_sdram_0_s1 & ~((cpu_0_instruction_master_read &
((|cpu_0_instruction_master_read_data_valid_sdram_0_s1_shift_register))) |
cpu_0_data_master_arbiterlock);
  //rdv_fifo_for_cpu_0_instruction_master_to_sdram_0_s1, which is an
e_fifo_with_registered_outputs
  rdv_fifo_for_cpu_0_instruction_master_to_sdram_0_s1_module
rdv_fifo_for_cpu_0_instruction_master_to_sdram_0_s1
    (
      .clear_fifo               (1'b0),
      .clk                      (clk),
      .data_in                  (cpu_0_instruction_master_granted_sdram_0_s1),
      .data_out
(cpu_0_instruction_master_rdv_fifo_output_from_sdram_0_s1),
```

```
        .empty                  (),
        .fifo_contains_ones_n (cpu_0_instruction_master_rdv_fifo_empty_sdram_0_s1),
        .full                   (),
        .read                   (sdram_0_s1_move_on_to_next_transaction),
        .reset_n                (reset_n),
        .sync_reset             (1'b0),
        .write                  (in_a_read_cycle & ~sdram_0_s1_waits_for_read)
      );

  assign cpu_0_instruction_master_read_data_valid_sdram_0_s1_shift_register = ~cpu_0_instruction_master_rdv_fifo_empty_sdram_0_s1;
  //local readdatavalid cpu_0_instruction_master_read_data_valid_sdram_0_s1, which is an e_mux
  assign cpu_0_instruction_master_read_data_valid_sdram_0_s1 = (sdram_0_s1_readdatavalid_from_sa & cpu_0_instruction_master_rdv_fifo_output_from_sdram_0_s1) & ~ cpu_0_instruction_master_rdv_fifo_empty_sdram_0_s1;

  //allow new arb cycle for sdram_0/s1, which is an e_assign
  assign sdram_0_s1_allow_new_arb_cycle = ~cpu_0_data_master_arbiterlock & ~cpu_0_instruction_master_arbiterlock;

  //cpu_0/instruction_master assignment into master qualified-requests vector for sdram_0/s1, which is an e_assign
  assign sdram_0_s1_master_qreq_vector[0] = cpu_0_instruction_master_qualified_request_sdram_0_s1;

  //cpu_0/instruction_master grant sdram_0/s1, which is an e_assign
  assign cpu_0_instruction_master_granted_sdram_0_s1 = sdram_0_s1_grant_vector[0];

  //cpu_0/instruction_master saved-grant sdram_0/s1, which is an e_assign
  assign cpu_0_instruction_master_saved_grant_sdram_0_s1 = sdram_0_s1_arb_winner[0] && cpu_0_instruction_master_requests_sdram_0_s1;

  //cpu_0/data_master assignment into master qualified-requests vector for sdram_0/s1, which is an e_assign
  assign sdram_0_s1_master_qreq_vector[1] = cpu_0_data_master_qualified_request_sdram_0_s1;

  //cpu_0/data_master grant sdram_0/s1, which is an e_assign
  assign cpu_0_data_master_granted_sdram_0_s1 = sdram_0_s1_grant_vector[1];

  //cpu_0/data_master saved-grant sdram_0/s1, which is an e_assign
  assign cpu_0_data_master_saved_grant_sdram_0_s1 = sdram_0_s1_arb_winner[1] && cpu_0_data_master_requests_sdram_0_s1;

  //sdram_0/s1 chosen-master double-vector, which is an e_assign
  assign sdram_0_s1_chosen_master_double_vector = {sdram_0_s1_master_qreq_vector, sdram_0_s1_master_qreq_vector} & ({~sdram_0_s1_master_qreq_vector, ~sdram_0_s1_master_qreq_vector} + sdram_0_s1_arb_addend);

  //stable onehot encoding of arb winner
  assign sdram_0_s1_arb_winner = (sdram_0_s1_allow_new_arb_cycle & | sdram_0_s1_grant_vector) ? sdram_0_s1_grant_vector : sdram_0_s1_saved_chosen_master_vector;

  //saved sdram_0_s1_grant_vector, which is an e_register
  always @(posedge clk or negedge reset_n)
```

```
      begin
        if (reset_n == 0)
            sdram_0_s1_saved_chosen_master_vector <= 0;
        else if (sdram_0_s1_allow_new_arb_cycle)
            sdram_0_s1_saved_chosen_master_vector <= |sdram_0_s1_grant_vector ?
sdram_0_s1_grant_vector : sdram_0_s1_saved_chosen_master_vector;
      end


   //onehot encoding of chosen master
   assign sdram_0_s1_grant_vector = {(sdram_0_s1_chosen_master_double_vector[1] |
sdram_0_s1_chosen_master_double_vector[3]),
      (sdram_0_s1_chosen_master_double_vector[0] |
sdram_0_s1_chosen_master_double_vector[2])};

   //sdram_0/s1 chosen master rotated left, which is an e_assign
   assign sdram_0_s1_chosen_master_rot_left = (sdram_0_s1_arb_winner << 1) ?
(sdram_0_s1_arb_winner << 1) : 1;

   //sdram_0/s1's addend for next-master-grant
   always @(posedge clk or negedge reset_n)
      begin
        if (reset_n == 0)
            sdram_0_s1_arb_addend <= 1;
        else if (|sdram_0_s1_grant_vector)
            sdram_0_s1_arb_addend <= sdram_0_s1_end_xfer?
sdram_0_s1_chosen_master_rot_left : sdram_0_s1_grant_vector;
      end


   //sdram_0_s1_reset_n assignment, which is an e_assign
   assign sdram_0_s1_reset_n = reset_n;

   assign sdram_0_s1_chipselect = cpu_0_data_master_granted_sdram_0_s1 |
cpu_0_instruction_master_granted_sdram_0_s1;
   //sdram_0_s1_firsttransfer first transaction, which is an e_assign
   assign sdram_0_s1_firsttransfer = sdram_0_s1_begins_xfer ? sdram_0_s1_unreg_firsttransfer :
sdram_0_s1_reg_firsttransfer;

   //sdram_0_s1_unreg_firsttransfer first transaction, which is an e_assign
   assign sdram_0_s1_unreg_firsttransfer = ~(sdram_0_s1_slavearbiterlockenable &
sdram_0_s1_any_continuerequest);

   //sdram_0_s1_reg_firsttransfer first transaction, which is an e_register
   always @(posedge clk or negedge reset_n)
      begin
        if (reset_n == 0)
            sdram_0_s1_reg_firsttransfer <= 1'b1;
        else if (sdram_0_s1_begins_xfer)
            sdram_0_s1_reg_firsttransfer <= sdram_0_s1_unreg_firsttransfer;
      end


   //sdram_0_s1_beginbursttransfer_internal begin burst transfer, which is an e_assign
   assign sdram_0_s1_beginbursttransfer_internal = sdram_0_s1_begins_xfer;

   //sdram_0_s1_arbitration_holdoff_internal arbitration_holdoff, which is an e_assign
   assign sdram_0_s1_arbitration_holdoff_internal = sdram_0_s1_begins_xfer &
```

```
sdram_0_s1_firsttransfer;

  //~sdram_0_s1_read_n assignment, which is an e_mux
  assign sdram_0_s1_read_n = ~((cpu_0_data_master_granted_sdram_0_s1 & cpu_0_data_master_read) | (cpu_0_instruction_master_granted_sdram_0_s1 & cpu_0_instruction_master_read));

  //~sdram_0_s1_write_n assignment, which is an e_mux
  assign sdram_0_s1_write_n = ~(cpu_0_data_master_granted_sdram_0_s1 & cpu_0_data_master_write);

  assign shifted_address_to_sdram_0_s1_from_cpu_0_data_master = {cpu_0_data_master_address_to_slave >> 2,
    cpu_0_data_master_dbs_address[1],
    {1 {1'b0}}};

  //sdram_0_s1_address mux, which is an e_mux
  assign sdram_0_s1_address = (cpu_0_data_master_granted_sdram_0_s1)? (shifted_address_to_sdram_0_s1_from_cpu_0_data_master >> 1) :
    (shifted_address_to_sdram_0_s1_from_cpu_0_instruction_master >> 1);

  assign shifted_address_to_sdram_0_s1_from_cpu_0_instruction_master = {cpu_0_instruction_master_address_to_slave >> 2,
    cpu_0_instruction_master_dbs_address[1],
    {1 {1'b0}}};

  //d1_sdram_0_s1_end_xfer register, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_sdram_0_s1_end_xfer <= 1;
      else
        d1_sdram_0_s1_end_xfer <= sdram_0_s1_end_xfer;
    end


  //sdram_0_s1_waits_for_read in a cycle, which is an e_mux
  assign sdram_0_s1_waits_for_read = sdram_0_s1_in_a_read_cycle & sdram_0_s1_waitrequest_from_sa;

  //sdram_0_s1_in_a_read_cycle assignment, which is an e_assign
  assign sdram_0_s1_in_a_read_cycle = (cpu_0_data_master_granted_sdram_0_s1 & cpu_0_data_master_read) | (cpu_0_instruction_master_granted_sdram_0_s1 & cpu_0_instruction_master_read);

  //in_a_read_cycle assignment, which is an e_mux
  assign in_a_read_cycle = sdram_0_s1_in_a_read_cycle;

  //sdram_0_s1_waits_for_write in a cycle, which is an e_mux
  assign sdram_0_s1_waits_for_write = sdram_0_s1_in_a_write_cycle & sdram_0_s1_waitrequest_from_sa;

  //sdram_0_s1_in_a_write_cycle assignment, which is an e_assign
  assign sdram_0_s1_in_a_write_cycle = cpu_0_data_master_granted_sdram_0_s1 & cpu_0_data_master_write;

  //in_a_write_cycle assignment, which is an e_mux
  assign in_a_write_cycle = sdram_0_s1_in_a_write_cycle;
```

```
  assign wait_for_sdram_0_s1_counter = 0;
  //~sdram_0_s1_byteenable_n byte enable port mux, which is an e_mux
  assign sdram_0_s1_byteenable_n = ~((cpu_0_data_master_granted_sdram_0_s1)?
cpu_0_data_master_byteenable_sdram_0_s1 :
    -1);

  assign {cpu_0_data_master_byteenable_sdram_0_s1_segment_1,
cpu_0_data_master_byteenable_sdram_0_s1_segment_0} = cpu_0_data_master_byteenable;
  assign cpu_0_data_master_byteenable_sdram_0_s1 = ((cpu_0_data_master_dbs_address[1]
== 0))? cpu_0_data_master_byteenable_sdram_0_s1_segment_0 :
    cpu_0_data_master_byteenable_sdram_0_s1_segment_1;


//synthesis translate_off
//////////////// SIMULATION-ONLY CONTENTS
  //sdram_0/s1 enable non-zero assertions, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          enable_nonzero_assertions <= 0;
      else
        enable_nonzero_assertions <= 1'b1;
    end


  //grant signals are active simultaneously, which is an e_process
  always @(posedge clk)
    begin
      if (cpu_0_data_master_granted_sdram_0_s1 +
cpu_0_instruction_master_granted_sdram_0_s1 > 1)
        begin
          $write("%0d ns: > 1 of grant signals are active simultaneously", $time);
          $stop;
        end
    end


  //saved_grant signals are active simultaneously, which is an e_process
  always @(posedge clk)
    begin
      if (cpu_0_data_master_saved_grant_sdram_0_s1 +
cpu_0_instruction_master_saved_grant_sdram_0_s1 > 1)
        begin
          $write("%0d ns: > 1 of saved_grant signals are active simultaneously", $time);
          $stop;
        end
    end



//////////////// END SIMULATION-ONLY CONTENTS

//synthesis translate_on

endmodule
```

```
// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module sram_mux_0_avalon_slave_0_arbitrator (
                                              // inputs:
                                               clk,
                                               cpu_0_data_master_address_to_slave,
                                               cpu_0_data_master_byteenable,
                                               cpu_0_data_master_dbs_address,
                                               cpu_0_data_master_dbs_write_16,

cpu_0_data_master_no_byte_enables_and_last_term,
                                               cpu_0_data_master_read,
                                               cpu_0_data_master_waitrequest,
                                               cpu_0_data_master_write,

cpu_0_instruction_master_address_to_slave,

cpu_0_instruction_master_dbs_address,
                                               cpu_0_instruction_master_read,
                                               reset_n,

sram_mux_0_avalon_slave_0_readdata,

                                              // outputs:

cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0,

cpu_0_data_master_granted_sram_mux_0_avalon_slave_0,

cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0,

cpu_0_data_master_read_data_valid_sram_mux_0_avalon_slave_0,

cpu_0_data_master_requests_sram_mux_0_avalon_slave_0,

cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0,

cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0,

cpu_0_instruction_master_read_data_valid_sram_mux_0_avalon_slave_0,

cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0,

d1_sram_mux_0_avalon_slave_0_end_xfer,
                                               sram_mux_0_avalon_slave_0_address,
                                               sram_mux_0_avalon_slave_0_read,

sram_mux_0_avalon_slave_0_readdata_from_sa,
                                               sram_mux_0_avalon_slave_0_write,

sram_mux_0_avalon_slave_0_writedata
                                             )
```

```
;

   output    [  1: 0] cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0;
   output             cpu_0_data_master_granted_sram_mux_0_avalon_slave_0;
   output             cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0;
   output             cpu_0_data_master_read_data_valid_sram_mux_0_avalon_slave_0;
   output             cpu_0_data_master_requests_sram_mux_0_avalon_slave_0;
   output             cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0;
   output
cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0;
   output
cpu_0_instruction_master_read_data_valid_sram_mux_0_avalon_slave_0;
   output             cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0;
   output             d1_sram_mux_0_avalon_slave_0_end_xfer;
   output   [ 17: 0] sram_mux_0_avalon_slave_0_address;
   output             sram_mux_0_avalon_slave_0_read;
   output   [ 15: 0] sram_mux_0_avalon_slave_0_readdata_from_sa;
   output             sram_mux_0_avalon_slave_0_write;
   output   [ 15: 0] sram_mux_0_avalon_slave_0_writedata;
   input              clk;
   input    [ 24: 0] cpu_0_data_master_address_to_slave;
   input    [  3: 0] cpu_0_data_master_byteenable;
   input    [  1: 0] cpu_0_data_master_dbs_address;
   input    [ 15: 0] cpu_0_data_master_dbs_write_16;
   input             cpu_0_data_master_no_byte_enables_and_last_term;
   input             cpu_0_data_master_read;
   input             cpu_0_data_master_waitrequest;
   input             cpu_0_data_master_write;
   input    [ 24: 0] cpu_0_instruction_master_address_to_slave;
   input    [  1: 0] cpu_0_instruction_master_dbs_address;
   input             cpu_0_instruction_master_read;
   input             reset_n;
   input    [ 15: 0] sram_mux_0_avalon_slave_0_readdata;

   wire              cpu_0_data_master_arbiterlock;
   wire              cpu_0_data_master_arbiterlock2;
   wire     [  1: 0] cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0;
   wire     [  1: 0] cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0_segment_0;
   wire     [  1: 0] cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0_segment_1;
   wire              cpu_0_data_master_continuerequest;
   wire              cpu_0_data_master_granted_sram_mux_0_avalon_slave_0;
   wire              cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0;
   wire              cpu_0_data_master_read_data_valid_sram_mux_0_avalon_slave_0;
   wire              cpu_0_data_master_requests_sram_mux_0_avalon_slave_0;
   wire              cpu_0_data_master_saved_grant_sram_mux_0_avalon_slave_0;
   wire              cpu_0_instruction_master_arbiterlock;
   wire              cpu_0_instruction_master_arbiterlock2;
   wire              cpu_0_instruction_master_continuerequest;
   wire              cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0;
   wire
cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0;
   wire
cpu_0_instruction_master_read_data_valid_sram_mux_0_avalon_slave_0;
   wire              cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0;
   wire              cpu_0_instruction_master_saved_grant_sram_mux_0_avalon_slave_0;
   reg               d1_reasons_to_wait;
   reg               d1_sram_mux_0_avalon_slave_0_end_xfer;
   reg               enable_nonzero_assertions;
```

```
  wire        end_xfer_arb_share_counter_term_sram_mux_0_avalon_slave_0;
  wire        in_a_read_cycle;
  wire        in_a_write_cycle;
  reg
last_cycle_cpu_0_data_master_granted_slave_sram_mux_0_avalon_slave_0;
  reg
last_cycle_cpu_0_instruction_master_granted_slave_sram_mux_0_avalon_slave_0;
  wire                                                [ 24: 0]
shifted_address_to_sram_mux_0_avalon_slave_0_from_cpu_0_data_master;
  wire                                                [ 24: 0]
shifted_address_to_sram_mux_0_avalon_slave_0_from_cpu_0_instruction_master;
  wire      [ 17: 0] sram_mux_0_avalon_slave_0_address;
  wire        sram_mux_0_avalon_slave_0_allgrants;
  wire        sram_mux_0_avalon_slave_0_allow_new_arb_cycle;
  wire        sram_mux_0_avalon_slave_0_any_bursting_master_saved_grant;
  wire        sram_mux_0_avalon_slave_0_any_continuerequest;
  reg       [  1: 0] sram_mux_0_avalon_slave_0_arb_addend;
  wire        sram_mux_0_avalon_slave_0_arb_counter_enable;
  reg       [  1: 0] sram_mux_0_avalon_slave_0_arb_share_counter;
  wire      [  1: 0] sram_mux_0_avalon_slave_0_arb_share_counter_next_value;
  wire      [  1: 0] sram_mux_0_avalon_slave_0_arb_share_set_values;
  wire      [  1: 0] sram_mux_0_avalon_slave_0_arb_winner;
  wire        sram_mux_0_avalon_slave_0_arbitration_holdoff_internal;
  wire        sram_mux_0_avalon_slave_0_beginbursttransfer_internal;
  wire        sram_mux_0_avalon_slave_0_begins_xfer;
  wire      [  3: 0] sram_mux_0_avalon_slave_0_chosen_master_double_vector;
  wire      [  1: 0] sram_mux_0_avalon_slave_0_chosen_master_rot_left;
  wire        sram_mux_0_avalon_slave_0_end_xfer;
  wire        sram_mux_0_avalon_slave_0_firsttransfer;
  wire      [  1: 0] sram_mux_0_avalon_slave_0_grant_vector;
  wire        sram_mux_0_avalon_slave_0_in_a_read_cycle;
  wire        sram_mux_0_avalon_slave_0_in_a_write_cycle;
  wire      [  1: 0] sram_mux_0_avalon_slave_0_master_qreq_vector;
  wire        sram_mux_0_avalon_slave_0_non_bursting_master_requests;
  wire        sram_mux_0_avalon_slave_0_read;
  wire      [ 15: 0] sram_mux_0_avalon_slave_0_readdata_from_sa;
  reg         sram_mux_0_avalon_slave_0_reg_firsttransfer;
  reg       [  1: 0] sram_mux_0_avalon_slave_0_saved_chosen_master_vector;
  reg         sram_mux_0_avalon_slave_0_slavearbiterlockenable;
  wire        sram_mux_0_avalon_slave_0_slavearbiterlockenable2;
  wire        sram_mux_0_avalon_slave_0_unreg_firsttransfer;
  wire        sram_mux_0_avalon_slave_0_waits_for_read;
  wire        sram_mux_0_avalon_slave_0_waits_for_write;
  wire        sram_mux_0_avalon_slave_0_write;
  wire      [ 15: 0] sram_mux_0_avalon_slave_0_writedata;
  wire        wait_for_sram_mux_0_avalon_slave_0_counter;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_reasons_to_wait <= 0;
      else
        d1_reasons_to_wait <= ~sram_mux_0_avalon_slave_0_end_xfer;
    end


  assign      sram_mux_0_avalon_slave_0_begins_xfer      =      ~d1_reasons_to_wait      &
((cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0                          |
cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0));
```

```
  //assign sram_mux_0_avalon_slave_0_readdata_from_sa = sram_mux_0_avalon_slave_0_readdata so that symbol knows where to group signals which may go to master only, which is an e_assign
  assign sram_mux_0_avalon_slave_0_readdata_from_sa = sram_mux_0_avalon_slave_0_readdata;

  assign cpu_0_data_master_requests_sram_mux_0_avalon_slave_0 = ({cpu_0_data_master_address_to_slave[24 : 19] , 19'b0} == 25'h100000) & (cpu_0_data_master_read | cpu_0_data_master_write);
  //sram_mux_0_avalon_slave_0_arb_share_counter set values, which is an e_mux
  assign sram_mux_0_avalon_slave_0_arb_share_set_values = (cpu_0_data_master_granted_sram_mux_0_avalon_slave_0)? 2 :
    (cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0)? 2 :
    (cpu_0_data_master_granted_sram_mux_0_avalon_slave_0)? 2 :
    (cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0)? 2 :
    1;

  //sram_mux_0_avalon_slave_0_non_bursting_master_requests mux, which is an e_mux
  assign sram_mux_0_avalon_slave_0_non_bursting_master_requests = cpu_0_data_master_requests_sram_mux_0_avalon_slave_0 |
    cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0 |
    cpu_0_data_master_requests_sram_mux_0_avalon_slave_0 |
    cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0;

  //sram_mux_0_avalon_slave_0_any_bursting_master_saved_grant mux, which is an e_mux
  assign sram_mux_0_avalon_slave_0_any_bursting_master_saved_grant = 0;

  //sram_mux_0_avalon_slave_0_arb_share_counter_next_value assignment, which is an e_assign
  assign sram_mux_0_avalon_slave_0_arb_share_counter_next_value = sram_mux_0_avalon_slave_0_firsttransfer ? (sram_mux_0_avalon_slave_0_arb_share_set_values - 1) : |sram_mux_0_avalon_slave_0_arb_share_counter ? (sram_mux_0_avalon_slave_0_arb_share_counter - 1) : 0;

  //sram_mux_0_avalon_slave_0_allgrants all slave grants, which is an e_mux
  assign sram_mux_0_avalon_slave_0_allgrants = (|sram_mux_0_avalon_slave_0_grant_vector) |
    (|sram_mux_0_avalon_slave_0_grant_vector) |
    (|sram_mux_0_avalon_slave_0_grant_vector) |
    (|sram_mux_0_avalon_slave_0_grant_vector);

  //sram_mux_0_avalon_slave_0_end_xfer assignment, which is an e_assign
  assign sram_mux_0_avalon_slave_0_end_xfer = ~(sram_mux_0_avalon_slave_0_waits_for_read | sram_mux_0_avalon_slave_0_waits_for_write);

  //end_xfer_arb_share_counter_term_sram_mux_0_avalon_slave_0 arb share counter enable term, which is an e_assign
  assign end_xfer_arb_share_counter_term_sram_mux_0_avalon_slave_0 = sram_mux_0_avalon_slave_0_end_xfer & (~sram_mux_0_avalon_slave_0_any_bursting_master_saved_grant | in_a_read_cycle | in_a_write_cycle);

  //sram_mux_0_avalon_slave_0_arb_share_counter arbitration counter enable, which is an e_assign
  assign sram_mux_0_avalon_slave_0_arb_counter_enable = (end_xfer_arb_share_counter_term_sram_mux_0_avalon_slave_0 &
```

```
sram_mux_0_avalon_slave_0_allgrants)                                                    |
(end_xfer_arb_share_counter_term_sram_mux_0_avalon_slave_0                              &
~sram_mux_0_avalon_slave_0_non_bursting_master_requests);

  //sram_mux_0_avalon_slave_0_arb_share_counter counter, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          sram_mux_0_avalon_slave_0_arb_share_counter <= 0;
      else if (sram_mux_0_avalon_slave_0_arb_counter_enable)
          sram_mux_0_avalon_slave_0_arb_share_counter                                   <=
sram_mux_0_avalon_slave_0_arb_share_counter_next_value;
    end


  //sram_mux_0_avalon_slave_0_slavearbiterlockenable slave enables arbiterlock, which is an
e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          sram_mux_0_avalon_slave_0_slavearbiterlockenable <= 0;
      else if ((|sram_mux_0_avalon_slave_0_master_qreq_vector                           &
end_xfer_arb_share_counter_term_sram_mux_0_avalon_slave_0)                              |
(end_xfer_arb_share_counter_term_sram_mux_0_avalon_slave_0                              &
~sram_mux_0_avalon_slave_0_non_bursting_master_requests))
          sram_mux_0_avalon_slave_0_slavearbiterlockenable                              <=
|sram_mux_0_avalon_slave_0_arb_share_counter_next_value;
    end


  //cpu_0/data_master sram_mux_0/avalon_slave_0 arbiterlock, which is an e_assign
  assign cpu_0_data_master_arbiterlock = sram_mux_0_avalon_slave_0_slavearbiterlockenable
& cpu_0_data_master_continuerequest;

  //sram_mux_0_avalon_slave_0_slavearbiterlockenable2 slave enables arbiterlock2, which is
an e_assign
  assign                    sram_mux_0_avalon_slave_0_slavearbiterlockenable2            =
|sram_mux_0_avalon_slave_0_arb_share_counter_next_value;

  //cpu_0/data_master sram_mux_0/avalon_slave_0 arbiterlock2, which is an e_assign
  assign                              cpu_0_data_master_arbiterlock2                    =
sram_mux_0_avalon_slave_0_slavearbiterlockenable2 & cpu_0_data_master_continuerequest;

  //cpu_0/instruction_master sram_mux_0/avalon_slave_0 arbiterlock, which is an e_assign
  assign                            cpu_0_instruction_master_arbiterlock              =
sram_mux_0_avalon_slave_0_slavearbiterlockenable                                        &
cpu_0_instruction_master_continuerequest;

  //cpu_0/instruction_master sram_mux_0/avalon_slave_0 arbiterlock2, which is an e_assign
  assign                            cpu_0_instruction_master_arbiterlock2             =
sram_mux_0_avalon_slave_0_slavearbiterlockenable2                                       &
cpu_0_instruction_master_continuerequest;

  //cpu_0/instruction_master granted sram_mux_0/avalon_slave_0 last time, which is an
e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
```

```
            last_cycle_cpu_0_instruction_master_granted_slave_sram_mux_0_avalon_slave_0
<= 0;
        else
          last_cycle_cpu_0_instruction_master_granted_slave_sram_mux_0_avalon_slave_0 <=
cpu_0_instruction_master_saved_grant_sram_mux_0_avalon_slave_0 ? 1 :
(sram_mux_0_avalon_slave_0_arbitration_holdoff_internal |
~cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0) ? 0 :
last_cycle_cpu_0_instruction_master_granted_slave_sram_mux_0_avalon_slave_0;
      end


  //cpu_0_instruction_master_continuerequest continued request, which is an e_mux
  assign cpu_0_instruction_master_continuerequest =
last_cycle_cpu_0_instruction_master_granted_slave_sram_mux_0_avalon_slave_0 &
cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0;

  //sram_mux_0_avalon_slave_0_any_continuerequest at least one master continues
requesting, which is an e_mux
  assign sram_mux_0_avalon_slave_0_any_continuerequest =
cpu_0_instruction_master_continuerequest |
      cpu_0_data_master_continuerequest;

  assign cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0 =
cpu_0_data_master_requests_sram_mux_0_avalon_slave_0 &
~(((~cpu_0_data_master_waitrequest | cpu_0_data_master_no_byte_enables_and_last_term
| !cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0) & cpu_0_data_master_write)
| cpu_0_instruction_master_arbiterlock);
  //sram_mux_0_avalon_slave_0_writedata mux, which is an e_mux
  assign sram_mux_0_avalon_slave_0_writedata = cpu_0_data_master_dbs_write_16;

  assign cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0 =
(({cpu_0_instruction_master_address_to_slave[24 : 19] , 19'b0} == 25'h100000) &
(cpu_0_instruction_master_read)) & cpu_0_instruction_master_read;
  //cpu_0/data_master granted sram_mux_0/avalon_slave_0 last time, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          last_cycle_cpu_0_data_master_granted_slave_sram_mux_0_avalon_slave_0 <= 0;
      else
        last_cycle_cpu_0_data_master_granted_slave_sram_mux_0_avalon_slave_0 <=
cpu_0_data_master_saved_grant_sram_mux_0_avalon_slave_0 ? 1 :
(sram_mux_0_avalon_slave_0_arbitration_holdoff_internal |
~cpu_0_data_master_requests_sram_mux_0_avalon_slave_0) ? 0 :
last_cycle_cpu_0_data_master_granted_slave_sram_mux_0_avalon_slave_0;
      end


  //cpu_0_data_master_continuerequest continued request, which is an e_mux
  assign cpu_0_data_master_continuerequest =
last_cycle_cpu_0_data_master_granted_slave_sram_mux_0_avalon_slave_0 &
cpu_0_data_master_requests_sram_mux_0_avalon_slave_0;

  assign cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0 =
cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0 &
~(cpu_0_data_master_arbiterlock);
  //allow new arb cycle for sram_mux_0/avalon_slave_0, which is an e_assign
  assign sram_mux_0_avalon_slave_0_allow_new_arb_cycle = ~cpu_0_data_master_arbiterlock
& ~cpu_0_instruction_master_arbiterlock;
```

```
  //cpu_0/instruction_master assignment into master qualified-requests vector for sram_mux_0/avalon_slave_0, which is an e_assign
  assign sram_mux_0_avalon_slave_0_master_qreq_vector[0] = cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0;

  //cpu_0/instruction_master grant sram_mux_0/avalon_slave_0, which is an e_assign
  assign cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0 = sram_mux_0_avalon_slave_0_grant_vector[0];

  //cpu_0/instruction_master saved-grant sram_mux_0/avalon_slave_0, which is an e_assign
  assign cpu_0_instruction_master_saved_grant_sram_mux_0_avalon_slave_0 = sram_mux_0_avalon_slave_0_arb_winner[0] && cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0;

  //cpu_0/data_master assignment into master qualified-requests vector for sram_mux_0/avalon_slave_0, which is an e_assign
  assign sram_mux_0_avalon_slave_0_master_qreq_vector[1] = cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0;

  //cpu_0/data_master grant sram_mux_0/avalon_slave_0, which is an e_assign
  assign cpu_0_data_master_granted_sram_mux_0_avalon_slave_0 = sram_mux_0_avalon_slave_0_grant_vector[1];

  //cpu_0/data_master saved-grant sram_mux_0/avalon_slave_0, which is an e_assign
  assign cpu_0_data_master_saved_grant_sram_mux_0_avalon_slave_0 = sram_mux_0_avalon_slave_0_arb_winner[1] && cpu_0_data_master_requests_sram_mux_0_avalon_slave_0;

  //sram_mux_0/avalon_slave_0 chosen-master double-vector, which is an e_assign
  assign sram_mux_0_avalon_slave_0_chosen_master_double_vector = {sram_mux_0_avalon_slave_0_master_qreq_vector,
sram_mux_0_avalon_slave_0_master_qreq_vector} & ({~sram_mux_0_avalon_slave_0_master_qreq_vector,
~sram_mux_0_avalon_slave_0_master_qreq_vector} + sram_mux_0_avalon_slave_0_arb_addend);

  //stable onehot encoding of arb winner
  assign sram_mux_0_avalon_slave_0_arb_winner = (sram_mux_0_avalon_slave_0_allow_new_arb_cycle & | sram_mux_0_avalon_slave_0_grant_vector) ? sram_mux_0_avalon_slave_0_grant_vector : sram_mux_0_avalon_slave_0_saved_chosen_master_vector;

  //saved sram_mux_0_avalon_slave_0_grant_vector, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          sram_mux_0_avalon_slave_0_saved_chosen_master_vector <= 0;
      else if (sram_mux_0_avalon_slave_0_allow_new_arb_cycle)
          sram_mux_0_avalon_slave_0_saved_chosen_master_vector <= |sram_mux_0_avalon_slave_0_grant_vector ? sram_mux_0_avalon_slave_0_grant_vector : sram_mux_0_avalon_slave_0_saved_chosen_master_vector;
    end


  //onehot encoding of chosen master
  assign sram_mux_0_avalon_slave_0_grant_vector = {(sram_mux_0_avalon_slave_0_chosen_master_double_vector[1] |
```

```
sram_mux_0_avalon_slave_0_chosen_master_double_vector[3]),
      (sram_mux_0_avalon_slave_0_chosen_master_double_vector[0]                    |
sram_mux_0_avalon_slave_0_chosen_master_double_vector[2])};

   //sram_mux_0/avalon_slave_0 chosen master rotated left, which is an e_assign
   assign                  sram_mux_0_avalon_slave_0_chosen_master_rot_left                =
(sram_mux_0_avalon_slave_0_arb_winner << 1) ? (sram_mux_0_avalon_slave_0_arb_winner <<
1) : 1;

   //sram_mux_0/avalon_slave_0's addend for next-master-grant
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               sram_mux_0_avalon_slave_0_arb_addend <= 1;
         else if (|sram_mux_0_avalon_slave_0_grant_vector)
               sram_mux_0_avalon_slave_0_arb_addend                                    <=
sram_mux_0_avalon_slave_0_end_xfer? sram_mux_0_avalon_slave_0_chosen_master_rot_left :
sram_mux_0_avalon_slave_0_grant_vector;
      end


   //sram_mux_0_avalon_slave_0_firsttransfer first transaction, which is an e_assign
   assign sram_mux_0_avalon_slave_0_firsttransfer = sram_mux_0_avalon_slave_0_begins_xfer ?
sram_mux_0_avalon_slave_0_unreg_firsttransfer                                          :
sram_mux_0_avalon_slave_0_reg_firsttransfer;

   //sram_mux_0_avalon_slave_0_unreg_firsttransfer first transaction, which is an e_assign
   assign                  sram_mux_0_avalon_slave_0_unreg_firsttransfer                =
~(sram_mux_0_avalon_slave_0_slavearbiterlockenable                                     &
sram_mux_0_avalon_slave_0_any_continuerequest);

   //sram_mux_0_avalon_slave_0_reg_firsttransfer first transaction, which is an e_register
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               sram_mux_0_avalon_slave_0_reg_firsttransfer <= 1'b1;
         else if (sram_mux_0_avalon_slave_0_begins_xfer)
               sram_mux_0_avalon_slave_0_reg_firsttransfer                             <=
sram_mux_0_avalon_slave_0_unreg_firsttransfer;
      end


   //sram_mux_0_avalon_slave_0_beginbursttransfer_internal begin burst transfer, which is an
e_assign
   assign                  sram_mux_0_avalon_slave_0_beginbursttransfer_internal          =
sram_mux_0_avalon_slave_0_begins_xfer;

   //sram_mux_0_avalon_slave_0_arbitration_holdoff_internal arbitration_holdoff, which is an
e_assign
   assign                  sram_mux_0_avalon_slave_0_arbitration_holdoff_internal         =
sram_mux_0_avalon_slave_0_begins_xfer & sram_mux_0_avalon_slave_0_firsttransfer;

   //sram_mux_0_avalon_slave_0_read assignment, which is an e_mux
   assign                  sram_mux_0_avalon_slave_0_read                                 =
(cpu_0_data_master_granted_sram_mux_0_avalon_slave_0   &   cpu_0_data_master_read)   |
(cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0                            &
cpu_0_instruction_master_read);
```

```
  //sram_mux_0_avalon_slave_0_write assignment, which is an e_mux
  assign sram_mux_0_avalon_slave_0_write = cpu_0_data_master_granted_sram_mux_0_avalon_slave_0 & cpu_0_data_master_write;

  assign shifted_address_to_sram_mux_0_avalon_slave_0_from_cpu_0_data_master = {cpu_0_data_master_address_to_slave >> 2,
      cpu_0_data_master_dbs_address[1],
      {1 {1'b0}}};

  //sram_mux_0_avalon_slave_0_address mux, which is an e_mux
  assign sram_mux_0_avalon_slave_0_address = (cpu_0_data_master_granted_sram_mux_0_avalon_slave_0)?
(shifted_address_to_sram_mux_0_avalon_slave_0_from_cpu_0_data_master >> 1) :
      (shifted_address_to_sram_mux_0_avalon_slave_0_from_cpu_0_instruction_master >> 1);

  assign shifted_address_to_sram_mux_0_avalon_slave_0_from_cpu_0_instruction_master = {cpu_0_instruction_master_address_to_slave >> 2,
      cpu_0_instruction_master_dbs_address[1],
      {1 {1'b0}}};

  //d1_sram_mux_0_avalon_slave_0_end_xfer register, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_sram_mux_0_avalon_slave_0_end_xfer <= 1;
      else
        d1_sram_mux_0_avalon_slave_0_end_xfer <= sram_mux_0_avalon_slave_0_end_xfer;
    end


  //sram_mux_0_avalon_slave_0_waits_for_read in a cycle, which is an e_mux
  assign sram_mux_0_avalon_slave_0_waits_for_read = sram_mux_0_avalon_slave_0_in_a_read_cycle & sram_mux_0_avalon_slave_0_begins_xfer;

  //sram_mux_0_avalon_slave_0_in_a_read_cycle assignment, which is an e_assign
  assign sram_mux_0_avalon_slave_0_in_a_read_cycle = (cpu_0_data_master_granted_sram_mux_0_avalon_slave_0 & cpu_0_data_master_read) |
(cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0 & cpu_0_instruction_master_read);

  //in_a_read_cycle assignment, which is an e_mux
  assign in_a_read_cycle = sram_mux_0_avalon_slave_0_in_a_read_cycle;

  //sram_mux_0_avalon_slave_0_waits_for_write in a cycle, which is an e_mux
  assign sram_mux_0_avalon_slave_0_waits_for_write = sram_mux_0_avalon_slave_0_in_a_write_cycle & 0;

  //sram_mux_0_avalon_slave_0_in_a_write_cycle assignment, which is an e_assign
  assign sram_mux_0_avalon_slave_0_in_a_write_cycle = cpu_0_data_master_granted_sram_mux_0_avalon_slave_0 & cpu_0_data_master_write;

  //in_a_write_cycle assignment, which is an e_mux
  assign in_a_write_cycle = sram_mux_0_avalon_slave_0_in_a_write_cycle;

  assign wait_for_sram_mux_0_avalon_slave_0_counter = 0;
  assign {cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0_segment_1,
cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0_segment_0} = cpu_0_data_master_byteenable;
```

```
  assign cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0 =
((cpu_0_data_master_dbs_address[1] == 0))?
cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0_segment_0 :
    cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0_segment_1;


//synthesis translate_off
//////////////// SIMULATION-ONLY CONTENTS
  //sram_mux_0/avalon_slave_0 enable non-zero assertions, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          enable_nonzero_assertions <= 0;
      else
        enable_nonzero_assertions <= 1'b1;
    end


  //grant signals are active simultaneously, which is an e_process
  always @(posedge clk)
    begin
      if (cpu_0_data_master_granted_sram_mux_0_avalon_slave_0 +
cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0 > 1)
        begin
          $write("%0d ns: > 1 of grant signals are active simultaneously", $time);
          $stop;
        end
    end


  //saved_grant signals are active simultaneously, which is an e_process
  always @(posedge clk)
    begin
      if (cpu_0_data_master_saved_grant_sram_mux_0_avalon_slave_0 +
cpu_0_instruction_master_saved_grant_sram_mux_0_avalon_slave_0 > 1)
        begin
          $write("%0d ns: > 1 of saved_grant signals are active simultaneously", $time);
          $stop;
        end
    end



//////////////// END SIMULATION-ONLY CONTENTS

//synthesis translate_on

endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030
```

```
module xycoord_interface_0_avalon_slave_0_arbitrator (
                                                        // inputs:
                                                          clk,

cpu_0_data_master_address_to_slave,

cpu_0_data_master_byteenable,

cpu_0_data_master_dbs_address,

cpu_0_data_master_dbs_write_16,

cpu_0_data_master_no_byte_enables_and_last_term,
                                                          cpu_0_data_master_read,

cpu_0_data_master_waitrequest,
                                                          cpu_0_data_master_write,

cpu_0_instruction_master_address_to_slave,

cpu_0_instruction_master_dbs_address,

cpu_0_instruction_master_read,
                                                          reset_n,

xycoord_interface_0_avalon_slave_0_readdata,

                                                        // outputs:

cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0,

cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0,

cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0,

cpu_0_data_master_read_data_valid_xycoord_interface_0_avalon_slave_0,

cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0,

cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0,

cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0,

cpu_0_instruction_master_read_data_valid_xycoord_interface_0_avalon_slave_0,

cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0,

d1_xycoord_interface_0_avalon_slave_0_end_xfer,

xycoord_interface_0_avalon_slave_0_address,

xycoord_interface_0_avalon_slave_0_chipselect,

xycoord_interface_0_avalon_slave_0_read,

xycoord_interface_0_avalon_slave_0_readdata_from_sa,

xycoord_interface_0_avalon_slave_0_reset_n,
```

```
xycoord_interface_0_avalon_slave_0_write,

xycoord_interface_0_avalon_slave_0_writedata
                                                                )
;

   output    [    1: 0] cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0;
   output                cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0;
   output
cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0;
   output
cpu_0_data_master_read_data_valid_xycoord_interface_0_avalon_slave_0;
   output                cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0;
   output
cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0;
   output
cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0;
   output
cpu_0_instruction_master_read_data_valid_xycoord_interface_0_avalon_slave_0;
   output
cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0;
   output                d1_xycoord_interface_0_avalon_slave_0_end_xfer;
   output    [    4: 0] xycoord_interface_0_avalon_slave_0_address;
   output                xycoord_interface_0_avalon_slave_0_chipselect;
   output                xycoord_interface_0_avalon_slave_0_read;
   output    [ 15: 0] xycoord_interface_0_avalon_slave_0_readdata_from_sa;
   output                xycoord_interface_0_avalon_slave_0_reset_n;
   output                xycoord_interface_0_avalon_slave_0_write;
   output    [ 15: 0] xycoord_interface_0_avalon_slave_0_writedata;
   input                 clk;
   input     [ 24: 0] cpu_0_data_master_address_to_slave;
   input     [    3: 0] cpu_0_data_master_byteenable;
   input     [    1: 0] cpu_0_data_master_dbs_address;
   input     [ 15: 0] cpu_0_data_master_dbs_write_16;
   input                 cpu_0_data_master_no_byte_enables_and_last_term;
   input                 cpu_0_data_master_read;
   input                 cpu_0_data_master_waitrequest;
   input                 cpu_0_data_master_write;
   input     [ 24: 0] cpu_0_instruction_master_address_to_slave;
   input     [    1: 0] cpu_0_instruction_master_dbs_address;
   input                 cpu_0_instruction_master_read;
   input                 reset_n;
   input     [ 15: 0] xycoord_interface_0_avalon_slave_0_readdata;

   wire                  cpu_0_data_master_arbiterlock;
   wire                  cpu_0_data_master_arbiterlock2;
   wire      [    1: 0] cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0;
   wire                                                  [                    1:                0]
cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0_segment_0;
   wire                                                  [                    1:                0]
cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0_segment_1;
   wire                  cpu_0_data_master_continuerequest;
   wire                  cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0;
   wire
cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0;
   wire
cpu_0_data_master_read_data_valid_xycoord_interface_0_avalon_slave_0;
```

```
  wire            cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0;
  wire            cpu_0_data_master_saved_grant_xycoord_interface_0_avalon_slave_0;
  wire            cpu_0_instruction_master_arbiterlock;
  wire            cpu_0_instruction_master_arbiterlock2;
  wire            cpu_0_instruction_master_continuerequest;
  wire
cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0;
  wire
cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0;
  wire
cpu_0_instruction_master_read_data_valid_xycoord_interface_0_avalon_slave_0;
  wire
cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0;
  wire
cpu_0_instruction_master_saved_grant_xycoord_interface_0_avalon_slave_0;
  reg             d1_reasons_to_wait;
  reg             d1_xycoord_interface_0_avalon_slave_0_end_xfer;
  reg             enable_nonzero_assertions;
  wire
end_xfer_arb_share_counter_term_xycoord_interface_0_avalon_slave_0;
  wire            in_a_read_cycle;
  wire            in_a_write_cycle;
  reg
last_cycle_cpu_0_data_master_granted_slave_xycoord_interface_0_avalon_slave_0;
  reg
last_cycle_cpu_0_instruction_master_granted_slave_xycoord_interface_0_avalon_slave_0;
  wire                                                [ 24: 0]
shifted_address_to_xycoord_interface_0_avalon_slave_0_from_cpu_0_data_master;
  wire                                                [ 24: 0]
shifted_address_to_xycoord_interface_0_avalon_slave_0_from_cpu_0_instruction_master;
  wire            wait_for_xycoord_interface_0_avalon_slave_0_counter;
  wire    [  4: 0] xycoord_interface_0_avalon_slave_0_address;
  wire            xycoord_interface_0_avalon_slave_0_allgrants;
  wire            xycoord_interface_0_avalon_slave_0_allow_new_arb_cycle;
  wire            xycoord_interface_0_avalon_slave_0_any_bursting_master_saved_grant;
  wire            xycoord_interface_0_avalon_slave_0_any_continuerequest;
  reg     [  1: 0] xycoord_interface_0_avalon_slave_0_arb_addend;
  wire            xycoord_interface_0_avalon_slave_0_arb_counter_enable;
  reg     [  1: 0] xycoord_interface_0_avalon_slave_0_arb_share_counter;
  wire    [  1: 0] xycoord_interface_0_avalon_slave_0_arb_share_counter_next_value;
  wire    [  1: 0] xycoord_interface_0_avalon_slave_0_arb_share_set_values;
  wire    [  1: 0] xycoord_interface_0_avalon_slave_0_arb_winner;
  wire            xycoord_interface_0_avalon_slave_0_arbitration_holdoff_internal;
  wire            xycoord_interface_0_avalon_slave_0_beginbursttransfer_internal;
  wire            xycoord_interface_0_avalon_slave_0_begins_xfer;
  wire            xycoord_interface_0_avalon_slave_0_chipselect;
  wire    [  3: 0] xycoord_interface_0_avalon_slave_0_chosen_master_double_vector;
  wire    [  1: 0] xycoord_interface_0_avalon_slave_0_chosen_master_rot_left;
  wire            xycoord_interface_0_avalon_slave_0_end_xfer;
  wire            xycoord_interface_0_avalon_slave_0_firsttransfer;
  wire    [  1: 0] xycoord_interface_0_avalon_slave_0_grant_vector;
  wire            xycoord_interface_0_avalon_slave_0_in_a_read_cycle;
  wire            xycoord_interface_0_avalon_slave_0_in_a_write_cycle;
  wire    [  1: 0] xycoord_interface_0_avalon_slave_0_master_qreq_vector;
  wire            xycoord_interface_0_avalon_slave_0_non_bursting_master_requests;
  wire            xycoord_interface_0_avalon_slave_0_read;
  wire    [ 15: 0] xycoord_interface_0_avalon_slave_0_readdata_from_sa;
  reg             xycoord_interface_0_avalon_slave_0_reg_firsttransfer;
```

```
  wire                    xycoord_interface_0_avalon_slave_0_reset_n;
  reg       [  1: 0] xycoord_interface_0_avalon_slave_0_saved_chosen_master_vector;
  reg                     xycoord_interface_0_avalon_slave_0_slavearbiterlockenable;
  wire                    xycoord_interface_0_avalon_slave_0_slavearbiterlockenable2;
  wire                    xycoord_interface_0_avalon_slave_0_unreg_firsttransfer;
  wire                    xycoord_interface_0_avalon_slave_0_waits_for_read;
  wire                    xycoord_interface_0_avalon_slave_0_waits_for_write;
  wire                    xycoord_interface_0_avalon_slave_0_write;
  wire      [ 15: 0] xycoord_interface_0_avalon_slave_0_writedata;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_reasons_to_wait <= 0;
      else
        d1_reasons_to_wait <= ~xycoord_interface_0_avalon_slave_0_end_xfer;
    end


  assign xycoord_interface_0_avalon_slave_0_begins_xfer = ~d1_reasons_to_wait &
((cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0 |
cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0));
  //assign xycoord_interface_0_avalon_slave_0_readdata_from_sa =
xycoord_interface_0_avalon_slave_0_readdata so that symbol knows where to group signals
which may go to master only, which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_readdata_from_sa =
xycoord_interface_0_avalon_slave_0_readdata;

  assign cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0 =
({cpu_0_data_master_address_to_slave[24 : 6] , 6'b0} == 25'h80) & (cpu_0_data_master_read |
cpu_0_data_master_write);
  //xycoord_interface_0_avalon_slave_0_arb_share_counter set values, which is an e_mux
  assign xycoord_interface_0_avalon_slave_0_arb_share_set_values =
(cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0)? 2 :
    (cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0)? 2 :
    (cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0)? 2 :
    (cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0)? 2 :
    1;

  //xycoord_interface_0_avalon_slave_0_non_bursting_master_requests mux, which is an
e_mux
  assign xycoord_interface_0_avalon_slave_0_non_bursting_master_requests =
cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0 |
    cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0 |
    cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0 |
    cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0;

  //xycoord_interface_0_avalon_slave_0_any_bursting_master_saved_grant mux, which is an
e_mux
  assign xycoord_interface_0_avalon_slave_0_any_bursting_master_saved_grant = 0;

  //xycoord_interface_0_avalon_slave_0_arb_share_counter_next_value assignment, which is
an e_assign
  assign xycoord_interface_0_avalon_slave_0_arb_share_counter_next_value =
xycoord_interface_0_avalon_slave_0_firsttransfer ?
(xycoord_interface_0_avalon_slave_0_arb_share_set_values - 1) :
|xycoord_interface_0_avalon_slave_0_arb_share_counter ?
(xycoord_interface_0_avalon_slave_0_arb_share_counter - 1) : 0;
```

```
  //xycoord_interface_0_avalon_slave_0_allgrants all slave grants, which is an e_mux
  assign xycoord_interface_0_avalon_slave_0_allgrants =
(|xycoord_interface_0_avalon_slave_0_grant_vector) |
    (|xycoord_interface_0_avalon_slave_0_grant_vector) |
    (|xycoord_interface_0_avalon_slave_0_grant_vector) |
    (|xycoord_interface_0_avalon_slave_0_grant_vector);

  //xycoord_interface_0_avalon_slave_0_end_xfer assignment, which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_end_xfer =
~(xycoord_interface_0_avalon_slave_0_waits_for_read |
xycoord_interface_0_avalon_slave_0_waits_for_write);

  //end_xfer_arb_share_counter_term_xycoord_interface_0_avalon_slave_0 arb share counter
enable term, which is an e_assign
  assign end_xfer_arb_share_counter_term_xycoord_interface_0_avalon_slave_0 =
xycoord_interface_0_avalon_slave_0_end_xfer &
(~xycoord_interface_0_avalon_slave_0_any_bursting_master_saved_grant | in_a_read_cycle |
in_a_write_cycle);

  //xycoord_interface_0_avalon_slave_0_arb_share_counter arbitration counter enable, which
is an e_assign
  assign xycoord_interface_0_avalon_slave_0_arb_counter_enable =
(end_xfer_arb_share_counter_term_xycoord_interface_0_avalon_slave_0 &
xycoord_interface_0_avalon_slave_0_allgrants) |
(end_xfer_arb_share_counter_term_xycoord_interface_0_avalon_slave_0 &
~xycoord_interface_0_avalon_slave_0_non_bursting_master_requests);

  //xycoord_interface_0_avalon_slave_0_arb_share_counter counter, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          xycoord_interface_0_avalon_slave_0_arb_share_counter <= 0;
      else if (xycoord_interface_0_avalon_slave_0_arb_counter_enable)
          xycoord_interface_0_avalon_slave_0_arb_share_counter <=
xycoord_interface_0_avalon_slave_0_arb_share_counter_next_value;
    end


  //xycoord_interface_0_avalon_slave_0_slavearbiterlockenable slave enables arbiterlock,
which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          xycoord_interface_0_avalon_slave_0_slavearbiterlockenable <= 0;
      else if ((|xycoord_interface_0_avalon_slave_0_master_qreq_vector &
end_xfer_arb_share_counter_term_xycoord_interface_0_avalon_slave_0) |
(end_xfer_arb_share_counter_term_xycoord_interface_0_avalon_slave_0 &
~xycoord_interface_0_avalon_slave_0_non_bursting_master_requests))
          xycoord_interface_0_avalon_slave_0_slavearbiterlockenable <=
|xycoord_interface_0_avalon_slave_0_arb_share_counter_next_value;
    end


  //cpu_0/data_master xycoord_interface_0/avalon_slave_0 arbiterlock, which is an e_assign
  assign cpu_0_data_master_arbiterlock =
xycoord_interface_0_avalon_slave_0_slavearbiterlockenable &
cpu_0_data_master_continuerequest;
```

```
  //xycoord_interface_0_avalon_slave_0_slavearbiterlockenable2 slave enables arbiterlock2, which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_slavearbiterlockenable2 = |xycoord_interface_0_avalon_slave_0_arb_share_counter_next_value;

  //cpu_0/data_master xycoord_interface_0/avalon_slave_0 arbiterlock2, which is an e_assign
  assign cpu_0_data_master_arbiterlock2 = xycoord_interface_0_avalon_slave_0_slavearbiterlockenable2 & cpu_0_data_master_continuerequest;

  //cpu_0/instruction_master xycoord_interface_0/avalon_slave_0 arbiterlock, which is an e_assign
  assign cpu_0_instruction_master_arbiterlock = xycoord_interface_0_avalon_slave_0_slavearbiterlockenable & cpu_0_instruction_master_continuerequest;

  //cpu_0/instruction_master xycoord_interface_0/avalon_slave_0 arbiterlock2, which is an e_assign
  assign cpu_0_instruction_master_arbiterlock2 = xycoord_interface_0_avalon_slave_0_slavearbiterlockenable2 & cpu_0_instruction_master_continuerequest;

  //cpu_0/instruction_master granted xycoord_interface_0/avalon_slave_0 last time, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)

last_cycle_cpu_0_instruction_master_granted_slave_xycoord_interface_0_avalon_slave_0 <= 0;
      else

last_cycle_cpu_0_instruction_master_granted_slave_xycoord_interface_0_avalon_slave_0 <= cpu_0_instruction_master_saved_grant_xycoord_interface_0_avalon_slave_0 ? 1 : (xycoord_interface_0_avalon_slave_0_arbitration_holdoff_internal | ~cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0) ? 0 : last_cycle_cpu_0_instruction_master_granted_slave_xycoord_interface_0_avalon_slave_0;
    end


  //cpu_0_instruction_master_continuerequest continued request, which is an e_mux
  assign cpu_0_instruction_master_continuerequest = last_cycle_cpu_0_instruction_master_granted_slave_xycoord_interface_0_avalon_slave_0 & cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0;

  //xycoord_interface_0_avalon_slave_0_any_continuerequest at least one master continues requesting, which is an e_mux
  assign xycoord_interface_0_avalon_slave_0_any_continuerequest = cpu_0_instruction_master_continuerequest |
    cpu_0_data_master_continuerequest;

  assign cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0 = cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0 & ~(((~cpu_0_data_master_waitrequest | cpu_0_data_master_no_byte_enables_and_last_term | !cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0) & cpu_0_data_master_write) | cpu_0_instruction_master_arbiterlock);
  //xycoord_interface_0_avalon_slave_0_writedata mux, which is an e_mux
  assign xycoord_interface_0_avalon_slave_0_writedata = cpu_0_data_master_dbs_write_16;
```

```
  assign cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0 = (({cpu_0_instruction_master_address_to_slave[24 : 6] , 6'b0} == 25'h80) & (cpu_0_instruction_master_read)) & cpu_0_instruction_master_read;
  //cpu_0/data_master granted xycoord_interface_0/avalon_slave_0 last time, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          last_cycle_cpu_0_data_master_granted_slave_xycoord_interface_0_avalon_slave_0 <= 0;
      else
        last_cycle_cpu_0_data_master_granted_slave_xycoord_interface_0_avalon_slave_0 <= cpu_0_data_master_saved_grant_xycoord_interface_0_avalon_slave_0 ? 1 : (xycoord_interface_0_avalon_slave_0_arbitration_holdoff_internal | ~cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0) ? 0 : last_cycle_cpu_0_data_master_granted_slave_xycoord_interface_0_avalon_slave_0;
    end


  //cpu_0_data_master_continuerequest continued request, which is an e_mux
  assign cpu_0_data_master_continuerequest = last_cycle_cpu_0_data_master_granted_slave_xycoord_interface_0_avalon_slave_0 & cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0;

  assign cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0 = cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0 & ~(cpu_0_data_master_arbiterlock);
  //allow new arb cycle for xycoord_interface_0/avalon_slave_0, which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_allow_new_arb_cycle = ~cpu_0_data_master_arbiterlock & ~cpu_0_instruction_master_arbiterlock;

  //cpu_0/instruction_master assignment into master qualified-requests vector for xycoord_interface_0/avalon_slave_0, which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_master_qreq_vector[0] = cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0;

  //cpu_0/instruction_master grant xycoord_interface_0/avalon_slave_0, which is an e_assign
  assign cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0 = xycoord_interface_0_avalon_slave_0_grant_vector[0];

  //cpu_0/instruction_master saved-grant xycoord_interface_0/avalon_slave_0, which is an e_assign
  assign cpu_0_instruction_master_saved_grant_xycoord_interface_0_avalon_slave_0 = xycoord_interface_0_avalon_slave_0_arb_winner[0] && cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0;

  //cpu_0/data_master assignment into master qualified-requests vector for xycoord_interface_0/avalon_slave_0, which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_master_qreq_vector[1] = cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0;

  //cpu_0/data_master grant xycoord_interface_0/avalon_slave_0, which is an e_assign
  assign cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0 = xycoord_interface_0_avalon_slave_0_grant_vector[1];

  //cpu_0/data_master saved-grant xycoord_interface_0/avalon_slave_0, which is an e_assign
  assign cpu_0_data_master_saved_grant_xycoord_interface_0_avalon_slave_0 = xycoord_interface_0_avalon_slave_0_arb_winner[1] &&
```

```
cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0;

  //xycoord_interface_0/avalon_slave_0 chosen-master double-vector, which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_chosen_master_double_vector =
{xycoord_interface_0_avalon_slave_0_master_qreq_vector,
xycoord_interface_0_avalon_slave_0_master_qreq_vector} &
({~xycoord_interface_0_avalon_slave_0_master_qreq_vector,
~xycoord_interface_0_avalon_slave_0_master_qreq_vector} +
xycoord_interface_0_avalon_slave_0_arb_addend);

  //stable onehot encoding of arb winner
  assign xycoord_interface_0_avalon_slave_0_arb_winner =
(xycoord_interface_0_avalon_slave_0_allow_new_arb_cycle & |
xycoord_interface_0_avalon_slave_0_grant_vector) ?
xycoord_interface_0_avalon_slave_0_grant_vector :
xycoord_interface_0_avalon_slave_0_saved_chosen_master_vector;

  //saved xycoord_interface_0_avalon_slave_0_grant_vector, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          xycoord_interface_0_avalon_slave_0_saved_chosen_master_vector <= 0;
      else if (xycoord_interface_0_avalon_slave_0_allow_new_arb_cycle)
          xycoord_interface_0_avalon_slave_0_saved_chosen_master_vector <=
|xycoord_interface_0_avalon_slave_0_grant_vector ?
xycoord_interface_0_avalon_slave_0_grant_vector :
xycoord_interface_0_avalon_slave_0_saved_chosen_master_vector;
    end


  //onehot encoding of chosen master
  assign xycoord_interface_0_avalon_slave_0_grant_vector =
{(xycoord_interface_0_avalon_slave_0_chosen_master_double_vector[1] |
xycoord_interface_0_avalon_slave_0_chosen_master_double_vector[3]),
    (xycoord_interface_0_avalon_slave_0_chosen_master_double_vector[0] |
xycoord_interface_0_avalon_slave_0_chosen_master_double_vector[2])};

  //xycoord_interface_0/avalon_slave_0 chosen master rotated left, which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_chosen_master_rot_left =
(xycoord_interface_0_avalon_slave_0_arb_winner << 1) ?
(xycoord_interface_0_avalon_slave_0_arb_winner << 1) : 1;

  //xycoord_interface_0/avalon_slave_0's addend for next-master-grant
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          xycoord_interface_0_avalon_slave_0_arb_addend <= 1;
      else if (|xycoord_interface_0_avalon_slave_0_grant_vector)
          xycoord_interface_0_avalon_slave_0_arb_addend <=
xycoord_interface_0_avalon_slave_0_end_xfer?
xycoord_interface_0_avalon_slave_0_chosen_master_rot_left :
xycoord_interface_0_avalon_slave_0_grant_vector;
    end


  //xycoord_interface_0_avalon_slave_0_reset_n assignment, which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_reset_n = reset_n;
```

```
  assign xycoord_interface_0_avalon_slave_0_chipselect =
cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0 |
cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0;
  //xycoord_interface_0_avalon_slave_0_firsttransfer first transaction, which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_firsttransfer =
xycoord_interface_0_avalon_slave_0_begins_xfer ?
xycoord_interface_0_avalon_slave_0_unreg_firsttransfer :
xycoord_interface_0_avalon_slave_0_reg_firsttransfer;

  //xycoord_interface_0_avalon_slave_0_unreg_firsttransfer first transaction, which is an
e_assign
  assign xycoord_interface_0_avalon_slave_0_unreg_firsttransfer =
~(xycoord_interface_0_avalon_slave_0_slavearbiterlockenable &
xycoord_interface_0_avalon_slave_0_any_continuerequest);

  //xycoord_interface_0_avalon_slave_0_reg_firsttransfer first transaction, which is an
e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          xycoord_interface_0_avalon_slave_0_reg_firsttransfer <= 1'b1;
      else if (xycoord_interface_0_avalon_slave_0_begins_xfer)
          xycoord_interface_0_avalon_slave_0_reg_firsttransfer <=
xycoord_interface_0_avalon_slave_0_unreg_firsttransfer;
    end


  //xycoord_interface_0_avalon_slave_0_beginbursttransfer_internal begin burst transfer,
which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_beginbursttransfer_internal =
xycoord_interface_0_avalon_slave_0_begins_xfer;

  //xycoord_interface_0_avalon_slave_0_arbitration_holdoff_internal arbitration_holdoff,
which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_arbitration_holdoff_internal =
xycoord_interface_0_avalon_slave_0_begins_xfer &
xycoord_interface_0_avalon_slave_0_firsttransfer;

  //xycoord_interface_0_avalon_slave_0_read assignment, which is an e_mux
  assign xycoord_interface_0_avalon_slave_0_read =
(cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0 & cpu_0_data_master_read)
|  (cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0 &
cpu_0_instruction_master_read);

  //xycoord_interface_0_avalon_slave_0_write assignment, which is an e_mux
  assign xycoord_interface_0_avalon_slave_0_write =
cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0 &
cpu_0_data_master_write;

  assign shifted_address_to_xycoord_interface_0_avalon_slave_0_from_cpu_0_data_master =
{cpu_0_data_master_address_to_slave >> 2,
    cpu_0_data_master_dbs_address[1],
    {1 {1'b0}}};

  //xycoord_interface_0_avalon_slave_0_address mux, which is an e_mux
  assign xycoord_interface_0_avalon_slave_0_address =
(cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0)?
(shifted_address_to_xycoord_interface_0_avalon_slave_0_from_cpu_0_data_master >> 1) :
```

```
(shifted_address_to_xycoord_interface_0_avalon_slave_0_from_cpu_0_instruction_master >>
1);

  assign
shifted_address_to_xycoord_interface_0_avalon_slave_0_from_cpu_0_instruction_master =
{cpu_0_instruction_master_address_to_slave >> 2,
    cpu_0_instruction_master_dbs_address[1],
    {1 {1'b0}}};

  //d1_xycoord_interface_0_avalon_slave_0_end_xfer register, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          d1_xycoord_interface_0_avalon_slave_0_end_xfer <= 1;
      else
        d1_xycoord_interface_0_avalon_slave_0_end_xfer <=
xycoord_interface_0_avalon_slave_0_end_xfer;
    end


  //xycoord_interface_0_avalon_slave_0_waits_for_read in a cycle, which is an e_mux
  assign xycoord_interface_0_avalon_slave_0_waits_for_read =
xycoord_interface_0_avalon_slave_0_in_a_read_cycle &
xycoord_interface_0_avalon_slave_0_begins_xfer;

  //xycoord_interface_0_avalon_slave_0_in_a_read_cycle assignment, which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_in_a_read_cycle =
(cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0 & cpu_0_data_master_read)
|       (cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0 &
cpu_0_instruction_master_read);

  //in_a_read_cycle assignment, which is an e_mux
  assign in_a_read_cycle = xycoord_interface_0_avalon_slave_0_in_a_read_cycle;

  //xycoord_interface_0_avalon_slave_0_waits_for_write in a cycle, which is an e_mux
  assign xycoord_interface_0_avalon_slave_0_waits_for_write =
xycoord_interface_0_avalon_slave_0_in_a_write_cycle & 0;

  //xycoord_interface_0_avalon_slave_0_in_a_write_cycle assignment, which is an e_assign
  assign xycoord_interface_0_avalon_slave_0_in_a_write_cycle =
cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0 &
cpu_0_data_master_write;

  //in_a_write_cycle assignment, which is an e_mux
  assign in_a_write_cycle = xycoord_interface_0_avalon_slave_0_in_a_write_cycle;

  assign wait_for_xycoord_interface_0_avalon_slave_0_counter = 0;
  assign {cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0_segment_1,
cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0_segment_0} =
cpu_0_data_master_byteenable;
  assign cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0 =
((cpu_0_data_master_dbs_address[1] == 0))?
cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0_segment_0 :
    cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0_segment_1;


//synthesis translate_off
```

```
//////////////// SIMULATION-ONLY CONTENTS
  //xycoord_interface_0/avalon_slave_0 enable non-zero assertions, which is an e_register
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          enable_nonzero_assertions <= 0;
      else
        enable_nonzero_assertions <= 1'b1;
    end


  //grant signals are active simultaneously, which is an e_process
  always @(posedge clk)
    begin
      if          (cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0          +
cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0 > 1)
        begin
          $write("%0d ns: > 1 of grant signals are active simultaneously", $time);
          $stop;
        end
    end


  //saved_grant signals are active simultaneously, which is an e_process
  always @(posedge clk)
    begin
      if        (cpu_0_data_master_saved_grant_xycoord_interface_0_avalon_slave_0        +
cpu_0_instruction_master_saved_grant_xycoord_interface_0_avalon_slave_0 > 1)
        begin
          $write("%0d ns: > 1 of saved_grant signals are active simultaneously", $time);
          $stop;
        end
    end



//////////////// END SIMULATION-ONLY CONTENTS

//synthesis translate_on

endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module nios_system_reset_clk_0_domain_synch_module (
                                                     // inputs:
                                                      clk,
                                                      data_in,
                                                      reset_n,

                                                     // outputs:
```

```
                                                                    data_out
                                                                )
;

   output               data_out;
   input                clk;
   input                data_in;
   input                reset_n;

   reg                  data_in_d1 /* synthesis ALTERA_ATTRIBUTE = "{-from \"*\"} CUT=ON ;
PRESERVE_REGISTER=ON ; SUPPRESS_DA_RULE_INTERNAL=R101"    */;
   reg                  data_out /* synthesis ALTERA_ATTRIBUTE = "PRESERVE_REGISTER=ON ;
SUPPRESS_DA_RULE_INTERNAL=R101"    */;
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               data_in_d1 <= 0;
         else
            data_in_d1 <= data_in;
      end


   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               data_out <= 0;
         else
            data_out <= data_in_d1;
      end



endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module nios_system (
                              // 1) global signals:
                                clk_0,
                                reset_n,

                              // the_command_0
                                oMOLECTRL_from_the_command_0,
                                oPANELCTRL_from_the_command_0,

                              // the_interrupt_0
                                irq_adc_to_the_interrupt_0,

                              // the_musiccontroller_0
                                AUD_ADCDAT_to_the_musiccontroller_0,
                                AUD_ADCLRCK_from_the_musiccontroller_0,
```

```
                                AUD_BCLK_to_and_from_the_musiccontroller_0,
                                AUD_DACDAT_from_the_musiccontroller_0,
                                AUD_DACLRCK_from_the_musiccontroller_0,
                                AUD_XCK_from_the_musiccontroller_0,
                                clk_18_to_the_musiccontroller_0,

                               // the_sdram_0
                                zs_addr_from_the_sdram_0,
                                zs_ba_from_the_sdram_0,
                                zs_cas_n_from_the_sdram_0,
                                zs_cke_from_the_sdram_0,
                                zs_cs_n_from_the_sdram_0,
                                zs_dq_to_and_from_the_sdram_0,
                                zs_dqm_from_the_sdram_0,
                                zs_ras_n_from_the_sdram_0,
                                zs_we_n_from_the_sdram_0,

                               // the_sram_mux_0
                                SRAM_ADDR_from_the_sram_mux_0,
                                SRAM_CE_N_from_the_sram_mux_0,
                                SRAM_DQ_to_and_from_the_sram_mux_0,
                                SRAM_LB_N_from_the_sram_mux_0,
                                SRAM_OE_N_from_the_sram_mux_0,
                                SRAM_UB_N_from_the_sram_mux_0,
                                SRAM_WE_N_from_the_sram_mux_0,
                                VGA_ADDR_to_the_sram_mux_0,
                                VGA_DQ_from_the_sram_mux_0,
                                VGA_OE_N_to_the_sram_mux_0,
                                VGA_WE_N_to_the_sram_mux_0,

                               // the_xycoord_interface_0
                                iX_COORD_to_the_xycoord_interface_0,
                                iY_COORD_to_the_xycoord_interface_0
                             )
;

  output              AUD_ADCLRCK_from_the_musiccontroller_0;
  inout               AUD_BCLK_to_and_from_the_musiccontroller_0;
  output              AUD_DACDAT_from_the_musiccontroller_0;
  output              AUD_DACLRCK_from_the_musiccontroller_0;
  output              AUD_XCK_from_the_musiccontroller_0;
  output  [ 17: 0] SRAM_ADDR_from_the_sram_mux_0;
  output              SRAM_CE_N_from_the_sram_mux_0;
  inout   [ 15: 0] SRAM_DQ_to_and_from_the_sram_mux_0;
  output              SRAM_LB_N_from_the_sram_mux_0;
  output              SRAM_OE_N_from_the_sram_mux_0;
  output              SRAM_UB_N_from_the_sram_mux_0;
  output              SRAM_WE_N_from_the_sram_mux_0;
  output  [ 15: 0] VGA_DQ_from_the_sram_mux_0;
  output  [ 31: 0] oMOLECTRL_from_the_command_0;
  output  [ 31: 0] oPANELCTRL_from_the_command_0;
  output  [ 11: 0] zs_addr_from_the_sdram_0;
  output  [  1: 0] zs_ba_from_the_sdram_0;
  output              zs_cas_n_from_the_sdram_0;
  output              zs_cke_from_the_sdram_0;
  output              zs_cs_n_from_the_sdram_0;
  inout   [ 15: 0] zs_dq_to_and_from_the_sdram_0;
  output  [  1: 0] zs_dqm_from_the_sdram_0;
```

```
output              zs_ras_n_from_the_sdram_0;
output              zs_we_n_from_the_sdram_0;
input               AUD_ADCDAT_to_the_musiccontroller_0;
input     [ 17: 0] VGA_ADDR_to_the_sram_mux_0;
input               VGA_OE_N_to_the_sram_mux_0;
input               VGA_WE_N_to_the_sram_mux_0;
input               clk_0;
input               clk_18_to_the_musiccontroller_0;
input     [ 11: 0] iX_COORD_to_the_xycoord_interface_0;
input     [ 11: 0] iY_COORD_to_the_xycoord_interface_0;
input               irq_adc_to_the_interrupt_0;
input               reset_n;

wire                AUD_ADCLRCK_from_the_musiccontroller_0;
wire                AUD_BCLK_to_and_from_the_musiccontroller_0;
wire                AUD_DACDAT_from_the_musiccontroller_0;
wire                AUD_DACLRCK_from_the_musiccontroller_0;
wire                AUD_XCK_from_the_musiccontroller_0;
wire      [ 17: 0] SRAM_ADDR_from_the_sram_mux_0;
wire                SRAM_CE_N_from_the_sram_mux_0;
wire      [ 15: 0] SRAM_DQ_to_and_from_the_sram_mux_0;
wire                SRAM_LB_N_from_the_sram_mux_0;
wire                SRAM_OE_N_from_the_sram_mux_0;
wire                SRAM_UB_N_from_the_sram_mux_0;
wire                SRAM_WE_N_from_the_sram_mux_0;
wire      [ 15: 0] VGA_DQ_from_the_sram_mux_0;
wire      [  4: 0] audio_controller_0_avalon_slave_0_address;
wire                audio_controller_0_avalon_slave_0_chipselect;
wire                audio_controller_0_avalon_slave_0_read;
wire      [ 15: 0] audio_controller_0_avalon_slave_0_readdata;
wire      [ 15: 0] audio_controller_0_avalon_slave_0_readdata_from_sa;
wire                audio_controller_0_avalon_slave_0_reset_n;
wire                audio_controller_0_avalon_slave_0_write;
wire      [ 15: 0] audio_controller_0_avalon_slave_0_writedata;
wire                clk_0_reset_n;
wire      [  4: 0] command_0_avalon_slave_0_address;
wire                command_0_avalon_slave_0_chipselect;
wire                command_0_avalon_slave_0_read;
wire      [ 31: 0] command_0_avalon_slave_0_readdata;
wire      [ 31: 0] command_0_avalon_slave_0_readdata_from_sa;
wire                command_0_avalon_slave_0_reset_n;
wire                command_0_avalon_slave_0_write;
wire      [ 31: 0] command_0_avalon_slave_0_writedata;
wire      [ 24: 0] cpu_0_data_master_address;
wire      [ 24: 0] cpu_0_data_master_address_to_slave;
wire      [  3: 0] cpu_0_data_master_byteenable;
wire      [  1: 0] cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0;
wire      [  1: 0] cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0;
wire      [  1: 0] cpu_0_data_master_byteenable_sdram_0_s1;
wire      [  1: 0] cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0;
wire      [  1: 0] cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0;
wire      [  1: 0] cpu_0_data_master_dbs_address;
wire      [ 15: 0] cpu_0_data_master_dbs_write_16;
wire                cpu_0_data_master_debugaccess;
wire                cpu_0_data_master_granted_audio_controller_0_avalon_slave_0;
wire                cpu_0_data_master_granted_command_0_avalon_slave_0;
wire                cpu_0_data_master_granted_cpu_0_jtag_debug_module;
wire                cpu_0_data_master_granted_interrupt_0_avalon_slave_0;
```

```
  wire                    cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave;
  wire                    cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0;
  wire                    cpu_0_data_master_granted_sdram_0_s1;
  wire                    cpu_0_data_master_granted_sram_mux_0_avalon_slave_0;
  wire                    cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0;
  wire      [ 31: 0] cpu_0_data_master_irq;
  wire                    cpu_0_data_master_no_byte_enables_and_last_term;
  wire
cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0;
  wire                    cpu_0_data_master_qualified_request_command_0_avalon_slave_0;
  wire                    cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module;
  wire                    cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0;
  wire                    cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave;
  wire
cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0;
  wire                    cpu_0_data_master_qualified_request_sdram_0_s1;
  wire                    cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0;
  wire
cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0;
  wire                    cpu_0_data_master_read;
  wire
cpu_0_data_master_read_data_valid_audio_controller_0_avalon_slave_0;
  wire                    cpu_0_data_master_read_data_valid_command_0_avalon_slave_0;
  wire                    cpu_0_data_master_read_data_valid_cpu_0_jtag_debug_module;
  wire                    cpu_0_data_master_read_data_valid_interrupt_0_avalon_slave_0;
  wire                    cpu_0_data_master_read_data_valid_jtag_uart_0_avalon_jtag_slave;
  wire                    cpu_0_data_master_read_data_valid_musiccontroller_0_avalon_slave_0;
  wire                    cpu_0_data_master_read_data_valid_sdram_0_s1;
  wire                    cpu_0_data_master_read_data_valid_sdram_0_s1_shift_register;
  wire                    cpu_0_data_master_read_data_valid_sram_mux_0_avalon_slave_0;
  wire
cpu_0_data_master_read_data_valid_xycoord_interface_0_avalon_slave_0;
  wire      [ 31: 0] cpu_0_data_master_readdata;
  wire                    cpu_0_data_master_requests_audio_controller_0_avalon_slave_0;
  wire                    cpu_0_data_master_requests_command_0_avalon_slave_0;
  wire                    cpu_0_data_master_requests_cpu_0_jtag_debug_module;
  wire                    cpu_0_data_master_requests_interrupt_0_avalon_slave_0;
  wire                    cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave;
  wire                    cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0;
  wire                    cpu_0_data_master_requests_sdram_0_s1;
  wire                    cpu_0_data_master_requests_sram_mux_0_avalon_slave_0;
  wire                    cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0;
  wire                    cpu_0_data_master_waitrequest;
  wire                    cpu_0_data_master_write;
  wire      [ 31: 0] cpu_0_data_master_writedata;
  wire      [ 24: 0] cpu_0_instruction_master_address;
  wire      [ 24: 0] cpu_0_instruction_master_address_to_slave;
  wire      [  1: 0] cpu_0_instruction_master_dbs_address;
  wire                    cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0;
  wire                    cpu_0_instruction_master_granted_command_0_avalon_slave_0;
  wire                    cpu_0_instruction_master_granted_cpu_0_jtag_debug_module;
  wire                    cpu_0_instruction_master_granted_sdram_0_s1;
  wire                    cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0;
  wire
cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0;
  wire
cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0;
  wire
```

```
cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0;
   wire
cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module;
   wire                    cpu_0_instruction_master_qualified_request_sdram_0_s1;
   wire
cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0;
   wire
cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0;
   wire                    cpu_0_instruction_master_read;
   wire
cpu_0_instruction_master_read_data_valid_audio_controller_0_avalon_slave_0;
   wire
cpu_0_instruction_master_read_data_valid_command_0_avalon_slave_0;
   wire                    cpu_0_instruction_master_read_data_valid_cpu_0_jtag_debug_module;
   wire                    cpu_0_instruction_master_read_data_valid_sdram_0_s1;
   wire                    cpu_0_instruction_master_read_data_valid_sdram_0_s1_shift_register;
   wire
cpu_0_instruction_master_read_data_valid_sram_mux_0_avalon_slave_0;
   wire
cpu_0_instruction_master_read_data_valid_xycoord_interface_0_avalon_slave_0;
   wire      [ 31: 0] cpu_0_instruction_master_readdata;
   wire                    cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0;
   wire                    cpu_0_instruction_master_requests_command_0_avalon_slave_0;
   wire                    cpu_0_instruction_master_requests_cpu_0_jtag_debug_module;
   wire                    cpu_0_instruction_master_requests_sdram_0_s1;
   wire                    cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0;
   wire
cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0;
   wire                    cpu_0_instruction_master_waitrequest;
   wire      [  8: 0] cpu_0_jtag_debug_module_address;
   wire                    cpu_0_jtag_debug_module_begintransfer;
   wire      [  3: 0] cpu_0_jtag_debug_module_byteenable;
   wire                    cpu_0_jtag_debug_module_chipselect;
   wire                    cpu_0_jtag_debug_module_debugaccess;
   wire      [ 31: 0] cpu_0_jtag_debug_module_readdata;
   wire      [ 31: 0] cpu_0_jtag_debug_module_readdata_from_sa;
   wire                    cpu_0_jtag_debug_module_reset_n;
   wire                    cpu_0_jtag_debug_module_resetrequest;
   wire                    cpu_0_jtag_debug_module_resetrequest_from_sa;
   wire                    cpu_0_jtag_debug_module_write;
   wire      [ 31: 0] cpu_0_jtag_debug_module_writedata;
   wire                    d1_audio_controller_0_avalon_slave_0_end_xfer;
   wire                    d1_command_0_avalon_slave_0_end_xfer;
   wire                    d1_cpu_0_jtag_debug_module_end_xfer;
   wire                    d1_interrupt_0_avalon_slave_0_end_xfer;
   wire                    d1_jtag_uart_0_avalon_jtag_slave_end_xfer;
   wire                    d1_musiccontroller_0_avalon_slave_0_end_xfer;
   wire                    d1_sdram_0_s1_end_xfer;
   wire                    d1_sram_mux_0_avalon_slave_0_end_xfer;
   wire                    d1_xycoord_interface_0_avalon_slave_0_end_xfer;
   wire      [  4: 0] interrupt_0_avalon_slave_0_address;
   wire                    interrupt_0_avalon_slave_0_chipselect;
   wire                    interrupt_0_avalon_slave_0_irq;
   wire                    interrupt_0_avalon_slave_0_irq_from_sa;
   wire                    interrupt_0_avalon_slave_0_read;
   wire      [ 31: 0] interrupt_0_avalon_slave_0_readdata;
   wire      [ 31: 0] interrupt_0_avalon_slave_0_readdata_from_sa;
   wire                    interrupt_0_avalon_slave_0_reset_n;
```

```
wire            interrupt_0_avalon_slave_0_write;
wire    [ 31: 0] interrupt_0_avalon_slave_0_writedata;
wire            jtag_uart_0_avalon_jtag_slave_address;
wire            jtag_uart_0_avalon_jtag_slave_chipselect;
wire            jtag_uart_0_avalon_jtag_slave_dataavailable;
wire            jtag_uart_0_avalon_jtag_slave_dataavailable_from_sa;
wire            jtag_uart_0_avalon_jtag_slave_irq;
wire            jtag_uart_0_avalon_jtag_slave_irq_from_sa;
wire            jtag_uart_0_avalon_jtag_slave_read_n;
wire    [ 31: 0] jtag_uart_0_avalon_jtag_slave_readdata;
wire    [ 31: 0] jtag_uart_0_avalon_jtag_slave_readdata_from_sa;
wire            jtag_uart_0_avalon_jtag_slave_readyfordata;
wire            jtag_uart_0_avalon_jtag_slave_readyfordata_from_sa;
wire            jtag_uart_0_avalon_jtag_slave_reset_n;
wire            jtag_uart_0_avalon_jtag_slave_waitrequest;
wire            jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa;
wire            jtag_uart_0_avalon_jtag_slave_write_n;
wire    [ 31: 0] jtag_uart_0_avalon_jtag_slave_writedata;
wire    [ 16: 0] musiccontroller_0_avalon_slave_0_address;
wire            musiccontroller_0_avalon_slave_0_chipselect;
wire            musiccontroller_0_avalon_slave_0_irq;
wire            musiccontroller_0_avalon_slave_0_irq_from_sa;
wire            musiccontroller_0_avalon_slave_0_read;
wire    [ 15: 0] musiccontroller_0_avalon_slave_0_readdata;
wire    [ 15: 0] musiccontroller_0_avalon_slave_0_readdata_from_sa;
wire            musiccontroller_0_avalon_slave_0_reset_n;
wire            musiccontroller_0_avalon_slave_0_write;
wire    [ 15: 0] musiccontroller_0_avalon_slave_0_writedata;
wire    [ 31: 0] oMOLECTRL_from_the_command_0;
wire    [ 31: 0] oPANELCTRL_from_the_command_0;
wire            reset_n_sources;
wire    [ 21: 0] sdram_0_s1_address;
wire    [  1: 0] sdram_0_s1_byteenable_n;
wire            sdram_0_s1_chipselect;
wire            sdram_0_s1_read_n;
wire    [ 15: 0] sdram_0_s1_readdata;
wire    [ 15: 0] sdram_0_s1_readdata_from_sa;
wire            sdram_0_s1_readdatavalid;
wire            sdram_0_s1_reset_n;
wire            sdram_0_s1_waitrequest;
wire            sdram_0_s1_waitrequest_from_sa;
wire            sdram_0_s1_write_n;
wire    [ 15: 0] sdram_0_s1_writedata;
wire    [ 17: 0] sram_mux_0_avalon_slave_0_address;
wire            sram_mux_0_avalon_slave_0_read;
wire    [ 15: 0] sram_mux_0_avalon_slave_0_readdata;
wire    [ 15: 0] sram_mux_0_avalon_slave_0_readdata_from_sa;
wire            sram_mux_0_avalon_slave_0_write;
wire    [ 15: 0] sram_mux_0_avalon_slave_0_writedata;
wire    [  4: 0] xycoord_interface_0_avalon_slave_0_address;
wire            xycoord_interface_0_avalon_slave_0_chipselect;
wire            xycoord_interface_0_avalon_slave_0_read;
wire    [ 15: 0] xycoord_interface_0_avalon_slave_0_readdata;
wire    [ 15: 0] xycoord_interface_0_avalon_slave_0_readdata_from_sa;
wire            xycoord_interface_0_avalon_slave_0_reset_n;
wire            xycoord_interface_0_avalon_slave_0_write;
wire    [ 15: 0] xycoord_interface_0_avalon_slave_0_writedata;
wire    [ 11: 0] zs_addr_from_the_sdram_0;
```

```
  wire       [  1: 0] zs_ba_from_the_sdram_0;
  wire                zs_cas_n_from_the_sdram_0;
  wire                zs_cke_from_the_sdram_0;
  wire                zs_cs_n_from_the_sdram_0;
  wire       [ 15: 0] zs_dq_to_and_from_the_sdram_0;
  wire       [  1: 0] zs_dqm_from_the_sdram_0;
  wire                zs_ras_n_from_the_sdram_0;
  wire                zs_we_n_from_the_sdram_0;
  audio_controller_0_avalon_slave_0_arbitrator the_audio_controller_0_avalon_slave_0
    (
      .audio_controller_0_avalon_slave_0_address
(audio_controller_0_avalon_slave_0_address),
      .audio_controller_0_avalon_slave_0_chipselect
(audio_controller_0_avalon_slave_0_chipselect),
      .audio_controller_0_avalon_slave_0_read
(audio_controller_0_avalon_slave_0_read),
      .audio_controller_0_avalon_slave_0_readdata
(audio_controller_0_avalon_slave_0_readdata),
      .audio_controller_0_avalon_slave_0_readdata_from_sa
(audio_controller_0_avalon_slave_0_readdata_from_sa),
      .audio_controller_0_avalon_slave_0_reset_n
(audio_controller_0_avalon_slave_0_reset_n),
      .audio_controller_0_avalon_slave_0_write
(audio_controller_0_avalon_slave_0_write),
      .audio_controller_0_avalon_slave_0_writedata
(audio_controller_0_avalon_slave_0_writedata),
      .clk
(clk_0),
      .cpu_0_data_master_address_to_slave
(cpu_0_data_master_address_to_slave),
      .cpu_0_data_master_byteenable
(cpu_0_data_master_byteenable),
      .cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0
(cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0),
      .cpu_0_data_master_dbs_address
(cpu_0_data_master_dbs_address),
      .cpu_0_data_master_dbs_write_16
(cpu_0_data_master_dbs_write_16),
      .cpu_0_data_master_granted_audio_controller_0_avalon_slave_0
(cpu_0_data_master_granted_audio_controller_0_avalon_slave_0),
      .cpu_0_data_master_no_byte_enables_and_last_term
(cpu_0_data_master_no_byte_enables_and_last_term),
      .cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0
(cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0),
      .cpu_0_data_master_read
(cpu_0_data_master_read),
      .cpu_0_data_master_read_data_valid_audio_controller_0_avalon_slave_0
(cpu_0_data_master_read_data_valid_audio_controller_0_avalon_slave_0),
      .cpu_0_data_master_requests_audio_controller_0_avalon_slave_0
(cpu_0_data_master_requests_audio_controller_0_avalon_slave_0),
      .cpu_0_data_master_waitrequest
(cpu_0_data_master_waitrequest),
      .cpu_0_data_master_write
(cpu_0_data_master_write),
      .cpu_0_instruction_master_address_to_slave
(cpu_0_instruction_master_address_to_slave),
      .cpu_0_instruction_master_dbs_address
(cpu_0_instruction_master_dbs_address),
```

```
        .cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0
(cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0),
        .cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0
(cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0),
        .cpu_0_instruction_master_read
(cpu_0_instruction_master_read),
        .cpu_0_instruction_master_read_data_valid_audio_controller_0_avalon_slave_0
(cpu_0_instruction_master_read_data_valid_audio_controller_0_avalon_slave_0),
        .cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0
(cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0),
        .d1_audio_controller_0_avalon_slave_0_end_xfer
(d1_audio_controller_0_avalon_slave_0_end_xfer),
        .reset_n
(clk_0_reset_n)
      );

   audio_controller_0 the_audio_controller_0
      (
        .address       (audio_controller_0_avalon_slave_0_address),
        .chipselect (audio_controller_0_avalon_slave_0_chipselect),
        .clk           (clk_0),
        .read          (audio_controller_0_avalon_slave_0_read),
        .readdata      (audio_controller_0_avalon_slave_0_readdata),
        .reset_n       (audio_controller_0_avalon_slave_0_reset_n),
        .write         (audio_controller_0_avalon_slave_0_write),
        .writedata     (audio_controller_0_avalon_slave_0_writedata)
      );

   command_0_avalon_slave_0_arbitrator the_command_0_avalon_slave_0
      (
        .clk
(clk_0),
        .command_0_avalon_slave_0_address
(command_0_avalon_slave_0_address),
        .command_0_avalon_slave_0_chipselect
(command_0_avalon_slave_0_chipselect),
        .command_0_avalon_slave_0_read
(command_0_avalon_slave_0_read),
        .command_0_avalon_slave_0_readdata
(command_0_avalon_slave_0_readdata),
        .command_0_avalon_slave_0_readdata_from_sa
(command_0_avalon_slave_0_readdata_from_sa),
        .command_0_avalon_slave_0_reset_n
(command_0_avalon_slave_0_reset_n),
        .command_0_avalon_slave_0_write
(command_0_avalon_slave_0_write),
        .command_0_avalon_slave_0_writedata
(command_0_avalon_slave_0_writedata),
        .cpu_0_data_master_address_to_slave
(cpu_0_data_master_address_to_slave),
        .cpu_0_data_master_granted_command_0_avalon_slave_0
(cpu_0_data_master_granted_command_0_avalon_slave_0),
        .cpu_0_data_master_qualified_request_command_0_avalon_slave_0
(cpu_0_data_master_qualified_request_command_0_avalon_slave_0),
        .cpu_0_data_master_read
(cpu_0_data_master_read),
        .cpu_0_data_master_read_data_valid_command_0_avalon_slave_0
(cpu_0_data_master_read_data_valid_command_0_avalon_slave_0),
```

```
        .cpu_0_data_master_requests_command_0_avalon_slave_0
(cpu_0_data_master_requests_command_0_avalon_slave_0),
        .cpu_0_data_master_waitrequest
(cpu_0_data_master_waitrequest),
        .cpu_0_data_master_write
(cpu_0_data_master_write),
        .cpu_0_data_master_writedata
(cpu_0_data_master_writedata),
        .cpu_0_instruction_master_address_to_slave
(cpu_0_instruction_master_address_to_slave),
        .cpu_0_instruction_master_granted_command_0_avalon_slave_0
(cpu_0_instruction_master_granted_command_0_avalon_slave_0),
        .cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0
(cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0),
        .cpu_0_instruction_master_read
(cpu_0_instruction_master_read),
        .cpu_0_instruction_master_read_data_valid_command_0_avalon_slave_0
(cpu_0_instruction_master_read_data_valid_command_0_avalon_slave_0),
        .cpu_0_instruction_master_requests_command_0_avalon_slave_0
(cpu_0_instruction_master_requests_command_0_avalon_slave_0),
        .d1_command_0_avalon_slave_0_end_xfer
(d1_command_0_avalon_slave_0_end_xfer),
        .reset_n
(clk_0_reset_n)
      );

   command_0 the_command_0
      (
        .address       (command_0_avalon_slave_0_address),
        .chipselect (command_0_avalon_slave_0_chipselect),
        .clk             (clk_0),
        .oMOLECTRL    (oMOLECTRL_from_the_command_0),
        .oPANELCTRL (oPANELCTRL_from_the_command_0),
        .read            (command_0_avalon_slave_0_read),
        .readdata     (command_0_avalon_slave_0_readdata),
        .reset_n       (command_0_avalon_slave_0_reset_n),
        .write          (command_0_avalon_slave_0_write),
        .writedata    (command_0_avalon_slave_0_writedata)
      );

   cpu_0_jtag_debug_module_arbitrator the_cpu_0_jtag_debug_module
      (
        .clk                                                                    (clk_0),
        .cpu_0_data_master_address_to_slave
(cpu_0_data_master_address_to_slave),
        .cpu_0_data_master_byteenable
(cpu_0_data_master_byteenable),
        .cpu_0_data_master_debugaccess
(cpu_0_data_master_debugaccess),
        .cpu_0_data_master_granted_cpu_0_jtag_debug_module
(cpu_0_data_master_granted_cpu_0_jtag_debug_module),
        .cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module
(cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module),
        .cpu_0_data_master_read
(cpu_0_data_master_read),
        .cpu_0_data_master_read_data_valid_cpu_0_jtag_debug_module
(cpu_0_data_master_read_data_valid_cpu_0_jtag_debug_module),
        .cpu_0_data_master_requests_cpu_0_jtag_debug_module
```

```
(cpu_0_data_master_requests_cpu_0_jtag_debug_module),
        .cpu_0_data_master_waitrequest
(cpu_0_data_master_waitrequest),
        .cpu_0_data_master_write
(cpu_0_data_master_write),
        .cpu_0_data_master_writedata
(cpu_0_data_master_writedata),
        .cpu_0_instruction_master_address_to_slave
(cpu_0_instruction_master_address_to_slave),
        .cpu_0_instruction_master_granted_cpu_0_jtag_debug_module
(cpu_0_instruction_master_granted_cpu_0_jtag_debug_module),
        .cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module
(cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module),
        .cpu_0_instruction_master_read
(cpu_0_instruction_master_read),
        .cpu_0_instruction_master_read_data_valid_cpu_0_jtag_debug_module
(cpu_0_instruction_master_read_data_valid_cpu_0_jtag_debug_module),
        .cpu_0_instruction_master_requests_cpu_0_jtag_debug_module
(cpu_0_instruction_master_requests_cpu_0_jtag_debug_module),
        .cpu_0_jtag_debug_module_address
(cpu_0_jtag_debug_module_address),
        .cpu_0_jtag_debug_module_begintransfer
(cpu_0_jtag_debug_module_begintransfer),
        .cpu_0_jtag_debug_module_byteenable
(cpu_0_jtag_debug_module_byteenable),
        .cpu_0_jtag_debug_module_chipselect
(cpu_0_jtag_debug_module_chipselect),
        .cpu_0_jtag_debug_module_debugaccess
(cpu_0_jtag_debug_module_debugaccess),
        .cpu_0_jtag_debug_module_readdata
(cpu_0_jtag_debug_module_readdata),
        .cpu_0_jtag_debug_module_readdata_from_sa
(cpu_0_jtag_debug_module_readdata_from_sa),
        .cpu_0_jtag_debug_module_reset_n
(cpu_0_jtag_debug_module_reset_n),
        .cpu_0_jtag_debug_module_resetrequest
(cpu_0_jtag_debug_module_resetrequest),
        .cpu_0_jtag_debug_module_resetrequest_from_sa
(cpu_0_jtag_debug_module_resetrequest_from_sa),
        .cpu_0_jtag_debug_module_write
(cpu_0_jtag_debug_module_write),
        .cpu_0_jtag_debug_module_writedata
(cpu_0_jtag_debug_module_writedata),
        .d1_cpu_0_jtag_debug_module_end_xfer
(d1_cpu_0_jtag_debug_module_end_xfer),
        .reset_n
(clk_0_reset_n)
      );

   cpu_0_data_master_arbitrator the_cpu_0_data_master
      (
        .audio_controller_0_avalon_slave_0_readdata_from_sa
(audio_controller_0_avalon_slave_0_readdata_from_sa),
        .clk
(clk_0),
        .command_0_avalon_slave_0_readdata_from_sa
(command_0_avalon_slave_0_readdata_from_sa),
        .cpu_0_data_master_address
```

```
(cpu_0_data_master_address),
        .cpu_0_data_master_address_to_slave
(cpu_0_data_master_address_to_slave),
        .cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0
(cpu_0_data_master_byteenable_audio_controller_0_avalon_slave_0),
        .cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0
(cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0),
        .cpu_0_data_master_byteenable_sdram_0_s1
(cpu_0_data_master_byteenable_sdram_0_s1),
        .cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0
(cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0),
        .cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0
(cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0),
        .cpu_0_data_master_dbs_address
(cpu_0_data_master_dbs_address),
        .cpu_0_data_master_dbs_write_16
(cpu_0_data_master_dbs_write_16),
        .cpu_0_data_master_granted_audio_controller_0_avalon_slave_0
(cpu_0_data_master_granted_audio_controller_0_avalon_slave_0),
        .cpu_0_data_master_granted_command_0_avalon_slave_0
(cpu_0_data_master_granted_command_0_avalon_slave_0),
        .cpu_0_data_master_granted_cpu_0_jtag_debug_module
(cpu_0_data_master_granted_cpu_0_jtag_debug_module),
        .cpu_0_data_master_granted_interrupt_0_avalon_slave_0
(cpu_0_data_master_granted_interrupt_0_avalon_slave_0),
        .cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave
(cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave),
        .cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0
(cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0),
        .cpu_0_data_master_granted_sdram_0_s1
(cpu_0_data_master_granted_sdram_0_s1),
        .cpu_0_data_master_granted_sram_mux_0_avalon_slave_0
(cpu_0_data_master_granted_sram_mux_0_avalon_slave_0),
        .cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0
(cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0),
        .cpu_0_data_master_irq
(cpu_0_data_master_irq),
        .cpu_0_data_master_no_byte_enables_and_last_term
(cpu_0_data_master_no_byte_enables_and_last_term),
        .cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0
(cpu_0_data_master_qualified_request_audio_controller_0_avalon_slave_0),
        .cpu_0_data_master_qualified_request_command_0_avalon_slave_0
(cpu_0_data_master_qualified_request_command_0_avalon_slave_0),
        .cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module
(cpu_0_data_master_qualified_request_cpu_0_jtag_debug_module),
        .cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0
(cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0),
        .cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave
(cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave),
        .cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0
(cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0),
        .cpu_0_data_master_qualified_request_sdram_0_s1
(cpu_0_data_master_qualified_request_sdram_0_s1),
        .cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0
(cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0),
        .cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0
(cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0),
        .cpu_0_data_master_read
```

```
(cpu_0_data_master_read),
        .cpu_0_data_master_read_data_valid_audio_controller_0_avalon_slave_0
(cpu_0_data_master_read_data_valid_audio_controller_0_avalon_slave_0),
        .cpu_0_data_master_read_data_valid_command_0_avalon_slave_0
(cpu_0_data_master_read_data_valid_command_0_avalon_slave_0),
        .cpu_0_data_master_read_data_valid_cpu_0_jtag_debug_module
(cpu_0_data_master_read_data_valid_cpu_0_jtag_debug_module),
        .cpu_0_data_master_read_data_valid_interrupt_0_avalon_slave_0
(cpu_0_data_master_read_data_valid_interrupt_0_avalon_slave_0),
        .cpu_0_data_master_read_data_valid_jtag_uart_0_avalon_jtag_slave
(cpu_0_data_master_read_data_valid_jtag_uart_0_avalon_jtag_slave),
        .cpu_0_data_master_read_data_valid_musiccontroller_0_avalon_slave_0
(cpu_0_data_master_read_data_valid_musiccontroller_0_avalon_slave_0),
        .cpu_0_data_master_read_data_valid_sdram_0_s1
(cpu_0_data_master_read_data_valid_sdram_0_s1),
        .cpu_0_data_master_read_data_valid_sdram_0_s1_shift_register
(cpu_0_data_master_read_data_valid_sdram_0_s1_shift_register),
        .cpu_0_data_master_read_data_valid_sram_mux_0_avalon_slave_0
(cpu_0_data_master_read_data_valid_sram_mux_0_avalon_slave_0),
        .cpu_0_data_master_read_data_valid_xycoord_interface_0_avalon_slave_0
(cpu_0_data_master_read_data_valid_xycoord_interface_0_avalon_slave_0),
        .cpu_0_data_master_readdata
(cpu_0_data_master_readdata),
        .cpu_0_data_master_requests_audio_controller_0_avalon_slave_0
(cpu_0_data_master_requests_audio_controller_0_avalon_slave_0),
        .cpu_0_data_master_requests_command_0_avalon_slave_0
(cpu_0_data_master_requests_command_0_avalon_slave_0),
        .cpu_0_data_master_requests_cpu_0_jtag_debug_module
(cpu_0_data_master_requests_cpu_0_jtag_debug_module),
        .cpu_0_data_master_requests_interrupt_0_avalon_slave_0
(cpu_0_data_master_requests_interrupt_0_avalon_slave_0),
        .cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave
(cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave),
        .cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0
(cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0),
        .cpu_0_data_master_requests_sdram_0_s1
(cpu_0_data_master_requests_sdram_0_s1),
        .cpu_0_data_master_requests_sram_mux_0_avalon_slave_0
(cpu_0_data_master_requests_sram_mux_0_avalon_slave_0),
        .cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0
(cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0),
        .cpu_0_data_master_waitrequest
(cpu_0_data_master_waitrequest),
        .cpu_0_data_master_write
(cpu_0_data_master_write),
        .cpu_0_data_master_writedata
(cpu_0_data_master_writedata),
        .cpu_0_jtag_debug_module_readdata_from_sa
(cpu_0_jtag_debug_module_readdata_from_sa),
        .d1_audio_controller_0_avalon_slave_0_end_xfer
(d1_audio_controller_0_avalon_slave_0_end_xfer),
        .d1_command_0_avalon_slave_0_end_xfer
(d1_command_0_avalon_slave_0_end_xfer),
        .d1_cpu_0_jtag_debug_module_end_xfer
(d1_cpu_0_jtag_debug_module_end_xfer),
        .d1_interrupt_0_avalon_slave_0_end_xfer
(d1_interrupt_0_avalon_slave_0_end_xfer),
        .d1_jtag_uart_0_avalon_jtag_slave_end_xfer
```

```
(d1_jtag_uart_0_avalon_jtag_slave_end_xfer),
        .d1_musiccontroller_0_avalon_slave_0_end_xfer
(d1_musiccontroller_0_avalon_slave_0_end_xfer),
        .d1_sdram_0_s1_end_xfer
(d1_sdram_0_s1_end_xfer),
        .d1_sram_mux_0_avalon_slave_0_end_xfer
(d1_sram_mux_0_avalon_slave_0_end_xfer),
        .d1_xycoord_interface_0_avalon_slave_0_end_xfer
(d1_xycoord_interface_0_avalon_slave_0_end_xfer),
        .interrupt_0_avalon_slave_0_irq_from_sa
(interrupt_0_avalon_slave_0_irq_from_sa),
        .interrupt_0_avalon_slave_0_readdata_from_sa
(interrupt_0_avalon_slave_0_readdata_from_sa),
        .jtag_uart_0_avalon_jtag_slave_irq_from_sa
(jtag_uart_0_avalon_jtag_slave_irq_from_sa),
        .jtag_uart_0_avalon_jtag_slave_readdata_from_sa
(jtag_uart_0_avalon_jtag_slave_readdata_from_sa),
        .jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa
(jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa),
        .musiccontroller_0_avalon_slave_0_irq_from_sa
(musiccontroller_0_avalon_slave_0_irq_from_sa),
        .musiccontroller_0_avalon_slave_0_readdata_from_sa
(musiccontroller_0_avalon_slave_0_readdata_from_sa),
        .reset_n
(clk_0_reset_n),
        .sdram_0_s1_readdata_from_sa
(sdram_0_s1_readdata_from_sa),
        .sdram_0_s1_waitrequest_from_sa
(sdram_0_s1_waitrequest_from_sa),
        .sram_mux_0_avalon_slave_0_readdata_from_sa
(sram_mux_0_avalon_slave_0_readdata_from_sa),
        .xycoord_interface_0_avalon_slave_0_readdata_from_sa
(xycoord_interface_0_avalon_slave_0_readdata_from_sa)
      );

   cpu_0_instruction_master_arbitrator the_cpu_0_instruction_master
      (
        .audio_controller_0_avalon_slave_0_readdata_from_sa
(audio_controller_0_avalon_slave_0_readdata_from_sa),
        .clk
(clk_0),
        .command_0_avalon_slave_0_readdata_from_sa
(command_0_avalon_slave_0_readdata_from_sa),
        .cpu_0_instruction_master_address
(cpu_0_instruction_master_address),
        .cpu_0_instruction_master_address_to_slave
(cpu_0_instruction_master_address_to_slave),
        .cpu_0_instruction_master_dbs_address
(cpu_0_instruction_master_dbs_address),
        .cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0
(cpu_0_instruction_master_granted_audio_controller_0_avalon_slave_0),
        .cpu_0_instruction_master_granted_command_0_avalon_slave_0
(cpu_0_instruction_master_granted_command_0_avalon_slave_0),
        .cpu_0_instruction_master_granted_cpu_0_jtag_debug_module
(cpu_0_instruction_master_granted_cpu_0_jtag_debug_module),
        .cpu_0_instruction_master_granted_sdram_0_s1
(cpu_0_instruction_master_granted_sdram_0_s1),
        .cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0
```

```
(cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0),
        .cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0
(cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0),
        .cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0
(cpu_0_instruction_master_qualified_request_audio_controller_0_avalon_slave_0),
        .cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0
(cpu_0_instruction_master_qualified_request_command_0_avalon_slave_0),
        .cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module
(cpu_0_instruction_master_qualified_request_cpu_0_jtag_debug_module),
        .cpu_0_instruction_master_qualified_request_sdram_0_s1
(cpu_0_instruction_master_qualified_request_sdram_0_s1),
        .cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0
(cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0),
        .cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0
(cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0),
        .cpu_0_instruction_master_read
(cpu_0_instruction_master_read),
        .cpu_0_instruction_master_read_data_valid_audio_controller_0_avalon_slave_0
(cpu_0_instruction_master_read_data_valid_audio_controller_0_avalon_slave_0),
        .cpu_0_instruction_master_read_data_valid_command_0_avalon_slave_0
(cpu_0_instruction_master_read_data_valid_command_0_avalon_slave_0),
        .cpu_0_instruction_master_read_data_valid_cpu_0_jtag_debug_module
(cpu_0_instruction_master_read_data_valid_cpu_0_jtag_debug_module),
        .cpu_0_instruction_master_read_data_valid_sdram_0_s1
(cpu_0_instruction_master_read_data_valid_sdram_0_s1),
        .cpu_0_instruction_master_read_data_valid_sdram_0_s1_shift_register
(cpu_0_instruction_master_read_data_valid_sdram_0_s1_shift_register),
        .cpu_0_instruction_master_read_data_valid_sram_mux_0_avalon_slave_0
(cpu_0_instruction_master_read_data_valid_sram_mux_0_avalon_slave_0),
        .cpu_0_instruction_master_read_data_valid_xycoord_interface_0_avalon_slave_0
(cpu_0_instruction_master_read_data_valid_xycoord_interface_0_avalon_slave_0),
        .cpu_0_instruction_master_readdata
(cpu_0_instruction_master_readdata),
        .cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0
(cpu_0_instruction_master_requests_audio_controller_0_avalon_slave_0),
        .cpu_0_instruction_master_requests_command_0_avalon_slave_0
(cpu_0_instruction_master_requests_command_0_avalon_slave_0),
        .cpu_0_instruction_master_requests_cpu_0_jtag_debug_module
(cpu_0_instruction_master_requests_cpu_0_jtag_debug_module),
        .cpu_0_instruction_master_requests_sdram_0_s1
(cpu_0_instruction_master_requests_sdram_0_s1),
        .cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0
(cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0),
        .cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0
(cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0),
        .cpu_0_instruction_master_waitrequest
(cpu_0_instruction_master_waitrequest),
        .cpu_0_jtag_debug_module_readdata_from_sa
(cpu_0_jtag_debug_module_readdata_from_sa),
        .d1_audio_controller_0_avalon_slave_0_end_xfer
(d1_audio_controller_0_avalon_slave_0_end_xfer),
        .d1_command_0_avalon_slave_0_end_xfer
(d1_command_0_avalon_slave_0_end_xfer),
        .d1_cpu_0_jtag_debug_module_end_xfer
(d1_cpu_0_jtag_debug_module_end_xfer),
        .d1_sdram_0_s1_end_xfer
(d1_sdram_0_s1_end_xfer),
        .d1_sram_mux_0_avalon_slave_0_end_xfer
```

```
(d1_sram_mux_0_avalon_slave_0_end_xfer),
        .d1_xycoord_interface_0_avalon_slave_0_end_xfer
(d1_xycoord_interface_0_avalon_slave_0_end_xfer),
        .reset_n
(clk_0_reset_n),
        .sdram_0_s1_readdata_from_sa
(sdram_0_s1_readdata_from_sa),
        .sdram_0_s1_waitrequest_from_sa
(sdram_0_s1_waitrequest_from_sa),
        .sram_mux_0_avalon_slave_0_readdata_from_sa
(sram_mux_0_avalon_slave_0_readdata_from_sa),
        .xycoord_interface_0_avalon_slave_0_readdata_from_sa
(xycoord_interface_0_avalon_slave_0_readdata_from_sa)
      );

   cpu_0 the_cpu_0
      (
        .clk                                   (clk_0),
        .d_address                             (cpu_0_data_master_address),
        .d_byteenable                          (cpu_0_data_master_byteenable),
        .d_irq                                 (cpu_0_data_master_irq),
        .d_read                                (cpu_0_data_master_read),
        .d_readdata                            (cpu_0_data_master_readdata),
        .d_waitrequest                         (cpu_0_data_master_waitrequest),
        .d_write                               (cpu_0_data_master_write),
        .d_writedata                           (cpu_0_data_master_writedata),
        .i_address                             (cpu_0_instruction_master_address),
        .i_read                                (cpu_0_instruction_master_read),
        .i_readdata                            (cpu_0_instruction_master_readdata),
        .i_waitrequest                         (cpu_0_instruction_master_waitrequest),
        .jtag_debug_module_address             (cpu_0_jtag_debug_module_address),
        .jtag_debug_module_begintransfer       (cpu_0_jtag_debug_module_begintransfer),
        .jtag_debug_module_byteenable          (cpu_0_jtag_debug_module_byteenable),
        .jtag_debug_module_debugaccess         (cpu_0_jtag_debug_module_debugaccess),
        .jtag_debug_module_debugaccess_to_roms (cpu_0_data_master_debugaccess),
        .jtag_debug_module_readdata            (cpu_0_jtag_debug_module_readdata),
        .jtag_debug_module_resetrequest        (cpu_0_jtag_debug_module_resetrequest),
        .jtag_debug_module_select              (cpu_0_jtag_debug_module_chipselect),
        .jtag_debug_module_write               (cpu_0_jtag_debug_module_write),
        .jtag_debug_module_writedata           (cpu_0_jtag_debug_module_writedata),
        .reset_n                               (cpu_0_jtag_debug_module_reset_n)
      );

   interrupt_0_avalon_slave_0_arbitrator the_interrupt_0_avalon_slave_0
      (
        .clk                                                                    (clk_0),
        .cpu_0_data_master_address_to_slave
(cpu_0_data_master_address_to_slave),
        .cpu_0_data_master_granted_interrupt_0_avalon_slave_0
(cpu_0_data_master_granted_interrupt_0_avalon_slave_0),
        .cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0
(cpu_0_data_master_qualified_request_interrupt_0_avalon_slave_0),
        .cpu_0_data_master_read
(cpu_0_data_master_read),
        .cpu_0_data_master_read_data_valid_interrupt_0_avalon_slave_0
(cpu_0_data_master_read_data_valid_interrupt_0_avalon_slave_0),
        .cpu_0_data_master_requests_interrupt_0_avalon_slave_0
(cpu_0_data_master_requests_interrupt_0_avalon_slave_0),
```

```
        .cpu_0_data_master_waitrequest
(cpu_0_data_master_waitrequest),
        .cpu_0_data_master_write
(cpu_0_data_master_write),
        .cpu_0_data_master_writedata
(cpu_0_data_master_writedata),
        .d1_interrupt_0_avalon_slave_0_end_xfer
(d1_interrupt_0_avalon_slave_0_end_xfer),
        .interrupt_0_avalon_slave_0_address
(interrupt_0_avalon_slave_0_address),
        .interrupt_0_avalon_slave_0_chipselect
(interrupt_0_avalon_slave_0_chipselect),
        .interrupt_0_avalon_slave_0_irq
(interrupt_0_avalon_slave_0_irq),
        .interrupt_0_avalon_slave_0_irq_from_sa
(interrupt_0_avalon_slave_0_irq_from_sa),
        .interrupt_0_avalon_slave_0_read
(interrupt_0_avalon_slave_0_read),
        .interrupt_0_avalon_slave_0_readdata
(interrupt_0_avalon_slave_0_readdata),
        .interrupt_0_avalon_slave_0_readdata_from_sa
(interrupt_0_avalon_slave_0_readdata_from_sa),
        .interrupt_0_avalon_slave_0_reset_n
(interrupt_0_avalon_slave_0_reset_n),
        .interrupt_0_avalon_slave_0_write
(interrupt_0_avalon_slave_0_write),
        .interrupt_0_avalon_slave_0_writedata
(interrupt_0_avalon_slave_0_writedata),
        .reset_n
(clk_0_reset_n)
      );

   interrupt_0 the_interrupt_0
      (
        .address       (interrupt_0_avalon_slave_0_address),
        .chipselect (interrupt_0_avalon_slave_0_chipselect),
        .clk              (clk_0),
        .irq              (interrupt_0_avalon_slave_0_irq),
        .irq_adc       (irq_adc_to_the_interrupt_0),
        .read             (interrupt_0_avalon_slave_0_read),
        .readdata      (interrupt_0_avalon_slave_0_readdata),
        .reset_n       (interrupt_0_avalon_slave_0_reset_n),
        .write            (interrupt_0_avalon_slave_0_write),
        .writedata    (interrupt_0_avalon_slave_0_writedata)
      );

   jtag_uart_0_avalon_jtag_slave_arbitrator the_jtag_uart_0_avalon_jtag_slave
      (
        .clk                                                                                    (clk_0),
        .cpu_0_data_master_address_to_slave
(cpu_0_data_master_address_to_slave),
        .cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave
(cpu_0_data_master_granted_jtag_uart_0_avalon_jtag_slave),
        .cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave
(cpu_0_data_master_qualified_request_jtag_uart_0_avalon_jtag_slave),
        .cpu_0_data_master_read
(cpu_0_data_master_read),
        .cpu_0_data_master_read_data_valid_jtag_uart_0_avalon_jtag_slave
```

```
(cpu_0_data_master_read_data_valid_jtag_uart_0_avalon_jtag_slave),
        .cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave
(cpu_0_data_master_requests_jtag_uart_0_avalon_jtag_slave),
        .cpu_0_data_master_waitrequest
(cpu_0_data_master_waitrequest),
        .cpu_0_data_master_write
(cpu_0_data_master_write),
        .cpu_0_data_master_writedata
(cpu_0_data_master_writedata),
        .d1_jtag_uart_0_avalon_jtag_slave_end_xfer
(d1_jtag_uart_0_avalon_jtag_slave_end_xfer),
        .jtag_uart_0_avalon_jtag_slave_address
(jtag_uart_0_avalon_jtag_slave_address),
        .jtag_uart_0_avalon_jtag_slave_chipselect
(jtag_uart_0_avalon_jtag_slave_chipselect),
        .jtag_uart_0_avalon_jtag_slave_dataavailable
(jtag_uart_0_avalon_jtag_slave_dataavailable),
        .jtag_uart_0_avalon_jtag_slave_dataavailable_from_sa
(jtag_uart_0_avalon_jtag_slave_dataavailable_from_sa),
        .jtag_uart_0_avalon_jtag_slave_irq
(jtag_uart_0_avalon_jtag_slave_irq),
        .jtag_uart_0_avalon_jtag_slave_irq_from_sa
(jtag_uart_0_avalon_jtag_slave_irq_from_sa),
        .jtag_uart_0_avalon_jtag_slave_read_n
(jtag_uart_0_avalon_jtag_slave_read_n),
        .jtag_uart_0_avalon_jtag_slave_readdata
(jtag_uart_0_avalon_jtag_slave_readdata),
        .jtag_uart_0_avalon_jtag_slave_readdata_from_sa
(jtag_uart_0_avalon_jtag_slave_readdata_from_sa),
        .jtag_uart_0_avalon_jtag_slave_readyfordata
(jtag_uart_0_avalon_jtag_slave_readyfordata),
        .jtag_uart_0_avalon_jtag_slave_readyfordata_from_sa
(jtag_uart_0_avalon_jtag_slave_readyfordata_from_sa),
        .jtag_uart_0_avalon_jtag_slave_reset_n
(jtag_uart_0_avalon_jtag_slave_reset_n),
        .jtag_uart_0_avalon_jtag_slave_waitrequest
(jtag_uart_0_avalon_jtag_slave_waitrequest),
        .jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa
(jtag_uart_0_avalon_jtag_slave_waitrequest_from_sa),
        .jtag_uart_0_avalon_jtag_slave_write_n
(jtag_uart_0_avalon_jtag_slave_write_n),
        .jtag_uart_0_avalon_jtag_slave_writedata
(jtag_uart_0_avalon_jtag_slave_writedata),
        .reset_n
(clk_0_reset_n)
      );

   jtag_uart_0 the_jtag_uart_0
     (
       .av_address         (jtag_uart_0_avalon_jtag_slave_address),
       .av_chipselect    (jtag_uart_0_avalon_jtag_slave_chipselect),
       .av_irq               (jtag_uart_0_avalon_jtag_slave_irq),
       .av_read_n          (jtag_uart_0_avalon_jtag_slave_read_n),
       .av_readdata       (jtag_uart_0_avalon_jtag_slave_readdata),
       .av_waitrequest (jtag_uart_0_avalon_jtag_slave_waitrequest),
       .av_write_n         (jtag_uart_0_avalon_jtag_slave_write_n),
       .av_writedata      (jtag_uart_0_avalon_jtag_slave_writedata),
       .clk                   (clk_0),
```

```
        .dataavailable    (jtag_uart_0_avalon_jtag_slave_dataavailable),
        .readyfordata     (jtag_uart_0_avalon_jtag_slave_readyfordata),
        .rst_n            (jtag_uart_0_avalon_jtag_slave_reset_n)
    );

  musiccontroller_0_avalon_slave_0_arbitrator the_musiccontroller_0_avalon_slave_0
    (
      .clk
(clk_0),
      .cpu_0_data_master_address_to_slave
(cpu_0_data_master_address_to_slave),
      .cpu_0_data_master_byteenable
(cpu_0_data_master_byteenable),
      .cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0
(cpu_0_data_master_byteenable_musiccontroller_0_avalon_slave_0),
      .cpu_0_data_master_dbs_address
(cpu_0_data_master_dbs_address),
      .cpu_0_data_master_dbs_write_16
(cpu_0_data_master_dbs_write_16),
      .cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0
(cpu_0_data_master_granted_musiccontroller_0_avalon_slave_0),
      .cpu_0_data_master_no_byte_enables_and_last_term
(cpu_0_data_master_no_byte_enables_and_last_term),
      .cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0
(cpu_0_data_master_qualified_request_musiccontroller_0_avalon_slave_0),
      .cpu_0_data_master_read
(cpu_0_data_master_read),
      .cpu_0_data_master_read_data_valid_musiccontroller_0_avalon_slave_0
(cpu_0_data_master_read_data_valid_musiccontroller_0_avalon_slave_0),
      .cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0
(cpu_0_data_master_requests_musiccontroller_0_avalon_slave_0),
      .cpu_0_data_master_waitrequest
(cpu_0_data_master_waitrequest),
      .cpu_0_data_master_write
(cpu_0_data_master_write),
      .d1_musiccontroller_0_avalon_slave_0_end_xfer
(d1_musiccontroller_0_avalon_slave_0_end_xfer),
      .musiccontroller_0_avalon_slave_0_address
(musiccontroller_0_avalon_slave_0_address),
      .musiccontroller_0_avalon_slave_0_chipselect
(musiccontroller_0_avalon_slave_0_chipselect),
      .musiccontroller_0_avalon_slave_0_irq
(musiccontroller_0_avalon_slave_0_irq),
      .musiccontroller_0_avalon_slave_0_irq_from_sa
(musiccontroller_0_avalon_slave_0_irq_from_sa),
      .musiccontroller_0_avalon_slave_0_read
(musiccontroller_0_avalon_slave_0_read),
      .musiccontroller_0_avalon_slave_0_readdata
(musiccontroller_0_avalon_slave_0_readdata),
      .musiccontroller_0_avalon_slave_0_readdata_from_sa
(musiccontroller_0_avalon_slave_0_readdata_from_sa),
      .musiccontroller_0_avalon_slave_0_reset_n
(musiccontroller_0_avalon_slave_0_reset_n),
      .musiccontroller_0_avalon_slave_0_write
(musiccontroller_0_avalon_slave_0_write),
      .musiccontroller_0_avalon_slave_0_writedata
(musiccontroller_0_avalon_slave_0_writedata),
      .reset_n
```

```
(clk_0_reset_n)
      );

   musiccontroller_0 the_musiccontroller_0
      (
        .AUD_ADCDAT    (AUD_ADCDAT_to_the_musiccontroller_0),
        .AUD_ADCLRCK (AUD_ADCLRCK_from_the_musiccontroller_0),
        .AUD_BCLK       (AUD_BCLK_to_and_from_the_musiccontroller_0),
        .AUD_DACDAT    (AUD_DACDAT_from_the_musiccontroller_0),
        .AUD_DACLRCK (AUD_DACLRCK_from_the_musiccontroller_0),
        .AUD_XCK         (AUD_XCK_from_the_musiccontroller_0),
        .address         (musiccontroller_0_avalon_slave_0_address),
        .chipselect    (musiccontroller_0_avalon_slave_0_chipselect),
        .clk               (clk_0),
        .clk_18          (clk_18_to_the_musiccontroller_0),
        .irq               (musiccontroller_0_avalon_slave_0_irq),
        .read              (musiccontroller_0_avalon_slave_0_read),
        .readdata       (musiccontroller_0_avalon_slave_0_readdata),
        .reset_n         (musiccontroller_0_avalon_slave_0_reset_n),
        .write             (musiccontroller_0_avalon_slave_0_write),
        .writedata      (musiccontroller_0_avalon_slave_0_writedata)
      );

   sdram_0_s1_arbitrator the_sdram_0_s1
      (
        .clk                                                                    (clk_0),
        .cpu_0_data_master_address_to_slave
(cpu_0_data_master_address_to_slave),
        .cpu_0_data_master_byteenable
(cpu_0_data_master_byteenable),
        .cpu_0_data_master_byteenable_sdram_0_s1
(cpu_0_data_master_byteenable_sdram_0_s1),
        .cpu_0_data_master_dbs_address
(cpu_0_data_master_dbs_address),
        .cpu_0_data_master_dbs_write_16
(cpu_0_data_master_dbs_write_16),
        .cpu_0_data_master_granted_sdram_0_s1
(cpu_0_data_master_granted_sdram_0_s1),
        .cpu_0_data_master_no_byte_enables_and_last_term
(cpu_0_data_master_no_byte_enables_and_last_term),
        .cpu_0_data_master_qualified_request_sdram_0_s1
(cpu_0_data_master_qualified_request_sdram_0_s1),
        .cpu_0_data_master_read
(cpu_0_data_master_read),
        .cpu_0_data_master_read_data_valid_sdram_0_s1
(cpu_0_data_master_read_data_valid_sdram_0_s1),
        .cpu_0_data_master_read_data_valid_sdram_0_s1_shift_register
(cpu_0_data_master_read_data_valid_sdram_0_s1_shift_register),
        .cpu_0_data_master_requests_sdram_0_s1
(cpu_0_data_master_requests_sdram_0_s1),
        .cpu_0_data_master_waitrequest
(cpu_0_data_master_waitrequest),
        .cpu_0_data_master_write
(cpu_0_data_master_write),
        .cpu_0_instruction_master_address_to_slave
(cpu_0_instruction_master_address_to_slave),
        .cpu_0_instruction_master_dbs_address
(cpu_0_instruction_master_dbs_address),
```

```
        .cpu_0_instruction_master_granted_sdram_0_s1
(cpu_0_instruction_master_granted_sdram_0_s1),
        .cpu_0_instruction_master_qualified_request_sdram_0_s1
(cpu_0_instruction_master_qualified_request_sdram_0_s1),
        .cpu_0_instruction_master_read
(cpu_0_instruction_master_read),
        .cpu_0_instruction_master_read_data_valid_sdram_0_s1
(cpu_0_instruction_master_read_data_valid_sdram_0_s1),
        .cpu_0_instruction_master_read_data_valid_sdram_0_s1_shift_register
(cpu_0_instruction_master_read_data_valid_sdram_0_s1_shift_register),
        .cpu_0_instruction_master_requests_sdram_0_s1
(cpu_0_instruction_master_requests_sdram_0_s1),
        .d1_sdram_0_s1_end_xfer
(d1_sdram_0_s1_end_xfer),
        .reset_n
(clk_0_reset_n),
        .sdram_0_s1_address
(sdram_0_s1_address),
        .sdram_0_s1_byteenable_n
(sdram_0_s1_byteenable_n),
        .sdram_0_s1_chipselect
(sdram_0_s1_chipselect),
        .sdram_0_s1_read_n
(sdram_0_s1_read_n),
        .sdram_0_s1_readdata
(sdram_0_s1_readdata),
        .sdram_0_s1_readdata_from_sa
(sdram_0_s1_readdata_from_sa),
        .sdram_0_s1_readdatavalid
(sdram_0_s1_readdatavalid),
        .sdram_0_s1_reset_n
(sdram_0_s1_reset_n),
        .sdram_0_s1_waitrequest
(sdram_0_s1_waitrequest),
        .sdram_0_s1_waitrequest_from_sa
(sdram_0_s1_waitrequest_from_sa),
        .sdram_0_s1_write_n
(sdram_0_s1_write_n),
        .sdram_0_s1_writedata
(sdram_0_s1_writedata)
      );

   sdram_0 the_sdram_0
     (
       .az_addr             (sdram_0_s1_address),
       .az_be_n             (sdram_0_s1_byteenable_n),
       .az_cs               (sdram_0_s1_chipselect),
       .az_data             (sdram_0_s1_writedata),
       .az_rd_n             (sdram_0_s1_read_n),
       .az_wr_n             (sdram_0_s1_write_n),
       .clk                 (clk_0),
       .reset_n             (sdram_0_s1_reset_n),
       .za_data             (sdram_0_s1_readdata),
       .za_valid            (sdram_0_s1_readdatavalid),
       .za_waitrequest (sdram_0_s1_waitrequest),
       .zs_addr             (zs_addr_from_the_sdram_0),
       .zs_ba               (zs_ba_from_the_sdram_0),
       .zs_cas_n            (zs_cas_n_from_the_sdram_0),
```

```
        .zs_cke               (zs_cke_from_the_sdram_0),
        .zs_cs_n              (zs_cs_n_from_the_sdram_0),
        .zs_dq                (zs_dq_to_and_from_the_sdram_0),
        .zs_dqm               (zs_dqm_from_the_sdram_0),
        .zs_ras_n             (zs_ras_n_from_the_sdram_0),
        .zs_we_n              (zs_we_n_from_the_sdram_0)
    );

  sram_mux_0_avalon_slave_0_arbitrator the_sram_mux_0_avalon_slave_0
    (
      .clk
(clk_0),
      .cpu_0_data_master_address_to_slave
(cpu_0_data_master_address_to_slave),
      .cpu_0_data_master_byteenable
(cpu_0_data_master_byteenable),
      .cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0
(cpu_0_data_master_byteenable_sram_mux_0_avalon_slave_0),
      .cpu_0_data_master_dbs_address
(cpu_0_data_master_dbs_address),
      .cpu_0_data_master_dbs_write_16
(cpu_0_data_master_dbs_write_16),
      .cpu_0_data_master_granted_sram_mux_0_avalon_slave_0
(cpu_0_data_master_granted_sram_mux_0_avalon_slave_0),
      .cpu_0_data_master_no_byte_enables_and_last_term
(cpu_0_data_master_no_byte_enables_and_last_term),
      .cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0
(cpu_0_data_master_qualified_request_sram_mux_0_avalon_slave_0),
      .cpu_0_data_master_read
(cpu_0_data_master_read),
      .cpu_0_data_master_read_data_valid_sram_mux_0_avalon_slave_0
(cpu_0_data_master_read_data_valid_sram_mux_0_avalon_slave_0),
      .cpu_0_data_master_requests_sram_mux_0_avalon_slave_0
(cpu_0_data_master_requests_sram_mux_0_avalon_slave_0),
      .cpu_0_data_master_waitrequest
(cpu_0_data_master_waitrequest),
      .cpu_0_data_master_write
(cpu_0_data_master_write),
      .cpu_0_instruction_master_address_to_slave
(cpu_0_instruction_master_address_to_slave),
      .cpu_0_instruction_master_dbs_address
(cpu_0_instruction_master_dbs_address),
      .cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0
(cpu_0_instruction_master_granted_sram_mux_0_avalon_slave_0),
      .cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0
(cpu_0_instruction_master_qualified_request_sram_mux_0_avalon_slave_0),
      .cpu_0_instruction_master_read
(cpu_0_instruction_master_read),
      .cpu_0_instruction_master_read_data_valid_sram_mux_0_avalon_slave_0
(cpu_0_instruction_master_read_data_valid_sram_mux_0_avalon_slave_0),
      .cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0
(cpu_0_instruction_master_requests_sram_mux_0_avalon_slave_0),
      .d1_sram_mux_0_avalon_slave_0_end_xfer
(d1_sram_mux_0_avalon_slave_0_end_xfer),
      .reset_n
(clk_0_reset_n),
      .sram_mux_0_avalon_slave_0_address
(sram_mux_0_avalon_slave_0_address),
```

```
        .sram_mux_0_avalon_slave_0_read
(sram_mux_0_avalon_slave_0_read),
        .sram_mux_0_avalon_slave_0_readdata
(sram_mux_0_avalon_slave_0_readdata),
        .sram_mux_0_avalon_slave_0_readdata_from_sa
(sram_mux_0_avalon_slave_0_readdata_from_sa),
        .sram_mux_0_avalon_slave_0_write
(sram_mux_0_avalon_slave_0_write),
        .sram_mux_0_avalon_slave_0_writedata
(sram_mux_0_avalon_slave_0_writedata)
      );

   sram_mux_0 the_sram_mux_0
      (
        .SRAM_ADDR (SRAM_ADDR_from_the_sram_mux_0),
        .SRAM_CE_N (SRAM_CE_N_from_the_sram_mux_0),
        .SRAM_DQ     (SRAM_DQ_to_and_from_the_sram_mux_0),
        .SRAM_LB_N (SRAM_LB_N_from_the_sram_mux_0),
        .SRAM_OE_N (SRAM_OE_N_from_the_sram_mux_0),
        .SRAM_UB_N (SRAM_UB_N_from_the_sram_mux_0),
        .SRAM_WE_N (SRAM_WE_N_from_the_sram_mux_0),
        .VGA_ADDR    (VGA_ADDR_to_the_sram_mux_0),
        .VGA_DQ      (VGA_DQ_from_the_sram_mux_0),
        .VGA_OE_N    (VGA_OE_N_to_the_sram_mux_0),
        .VGA_WE_N    (VGA_WE_N_to_the_sram_mux_0),
        .address     (sram_mux_0_avalon_slave_0_address),
        .read        (sram_mux_0_avalon_slave_0_read),
        .readdata    (sram_mux_0_avalon_slave_0_readdata),
        .write       (sram_mux_0_avalon_slave_0_write),
        .writedata (sram_mux_0_avalon_slave_0_writedata)
      );

   xycoord_interface_0_avalon_slave_0_arbitrator the_xycoord_interface_0_avalon_slave_0
      (
        .clk
(clk_0),
        .cpu_0_data_master_address_to_slave
(cpu_0_data_master_address_to_slave),
        .cpu_0_data_master_byteenable
(cpu_0_data_master_byteenable),
        .cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0
(cpu_0_data_master_byteenable_xycoord_interface_0_avalon_slave_0),
        .cpu_0_data_master_dbs_address
(cpu_0_data_master_dbs_address),
        .cpu_0_data_master_dbs_write_16
(cpu_0_data_master_dbs_write_16),
        .cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0
(cpu_0_data_master_granted_xycoord_interface_0_avalon_slave_0),
        .cpu_0_data_master_no_byte_enables_and_last_term
(cpu_0_data_master_no_byte_enables_and_last_term),
        .cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0
(cpu_0_data_master_qualified_request_xycoord_interface_0_avalon_slave_0),
        .cpu_0_data_master_read
(cpu_0_data_master_read),
        .cpu_0_data_master_read_data_valid_xycoord_interface_0_avalon_slave_0
(cpu_0_data_master_read_data_valid_xycoord_interface_0_avalon_slave_0),
        .cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0
(cpu_0_data_master_requests_xycoord_interface_0_avalon_slave_0),
```

```
        .cpu_0_data_master_waitrequest
(cpu_0_data_master_waitrequest),
        .cpu_0_data_master_write
(cpu_0_data_master_write),
        .cpu_0_instruction_master_address_to_slave
(cpu_0_instruction_master_address_to_slave),
        .cpu_0_instruction_master_dbs_address
(cpu_0_instruction_master_dbs_address),
        .cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0
(cpu_0_instruction_master_granted_xycoord_interface_0_avalon_slave_0),
        .cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0
(cpu_0_instruction_master_qualified_request_xycoord_interface_0_avalon_slave_0),
        .cpu_0_instruction_master_read
(cpu_0_instruction_master_read),
        .cpu_0_instruction_master_read_data_valid_xycoord_interface_0_avalon_slave_0
(cpu_0_instruction_master_read_data_valid_xycoord_interface_0_avalon_slave_0),
        .cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0
(cpu_0_instruction_master_requests_xycoord_interface_0_avalon_slave_0),
        .d1_xycoord_interface_0_avalon_slave_0_end_xfer
(d1_xycoord_interface_0_avalon_slave_0_end_xfer),
        .reset_n
(clk_0_reset_n),
        .xycoord_interface_0_avalon_slave_0_address
(xycoord_interface_0_avalon_slave_0_address),
        .xycoord_interface_0_avalon_slave_0_chipselect
(xycoord_interface_0_avalon_slave_0_chipselect),
        .xycoord_interface_0_avalon_slave_0_read
(xycoord_interface_0_avalon_slave_0_read),
        .xycoord_interface_0_avalon_slave_0_readdata
(xycoord_interface_0_avalon_slave_0_readdata),
        .xycoord_interface_0_avalon_slave_0_readdata_from_sa
(xycoord_interface_0_avalon_slave_0_readdata_from_sa),
        .xycoord_interface_0_avalon_slave_0_reset_n
(xycoord_interface_0_avalon_slave_0_reset_n),
        .xycoord_interface_0_avalon_slave_0_write
(xycoord_interface_0_avalon_slave_0_write),
        .xycoord_interface_0_avalon_slave_0_writedata
(xycoord_interface_0_avalon_slave_0_writedata)
      );

   xycoord_interface_0 the_xycoord_interface_0
      (
        .address       (xycoord_interface_0_avalon_slave_0_address),
        .chipselect (xycoord_interface_0_avalon_slave_0_chipselect),
        .clk              (clk_0),
        .iX_COORD      (iX_COORD_to_the_xycoord_interface_0),
        .iY_COORD      (iY_COORD_to_the_xycoord_interface_0),
        .read             (xycoord_interface_0_avalon_slave_0_read),
        .readdata      (xycoord_interface_0_avalon_slave_0_readdata),
        .reset_n       (xycoord_interface_0_avalon_slave_0_reset_n),
        .write           (xycoord_interface_0_avalon_slave_0_write),
        .writedata    (xycoord_interface_0_avalon_slave_0_writedata)
      );

   //reset is asserted asynchronously and deasserted synchronously
   nios_system_reset_clk_0_domain_synch_module nios_system_reset_clk_0_domain_synch
      (
        .clk          (clk_0),
```

```
          .data_in    (1'b1),
          .data_out (clk_0_reset_n),
          .reset_n    (reset_n_sources)
       );

   //reset sources mux, which is an e_mux
   assign reset_n_sources = ~(~reset_n |
      0 |
      cpu_0_jtag_debug_module_resetrequest_from_sa |
      cpu_0_jtag_debug_module_resetrequest_from_sa);


endmodule


//synthesis translate_off



// <ALTERA_NOTE> CODE INSERTED BETWEEN HERE

// AND HERE WILL BE PRESERVED </ALTERA_NOTE>


// If user logic components use Altsync_Ram with convert_hex2ver.dll,
// set USE_convert_hex2ver in the user comments section above

// `ifdef USE_convert_hex2ver
// `else
// `define NO_PLI 1
// `endif

`include "/opt/altera/altera12.1/quartus/eda/sim_lib/altera_mf.v"
`include "/opt/altera/altera12.1/quartus/eda/sim_lib/220model.v"
`include "/opt/altera/altera12.1/quartus/eda/sim_lib/sgate.v"
`include "interrupt.v"
`include "command.v"
`include "command_0.v"
`include "xycoord_interface.v"
`include "xycoord_interface_0.v"
`include "sram_mux.v"
`include "sram_mux_0.v"
// musiccontroller.vhd
// musiccontroller_0.vhd
`include "audio_controller.v"
`include "audio_controller_0.v"
`include "sdram_0.v"
`include "cpu_0_test_bench.v"
`include "cpu_0_oci_test_bench.v"
`include "cpu_0_jtag_debug_module_tck.v"
`include "cpu_0_jtag_debug_module_sysclk.v"
`include "cpu_0_jtag_debug_module_wrapper.v"
`include "cpu_0.v"
`include "jtag_uart_0.v"

`timescale 1ns / 1ps

module test_bench
```

```
;


   wire              AUD_ADCDAT_to_the_musiccontroller_0;
   wire              AUD_ADCLRCK_from_the_musiccontroller_0;
   wire              AUD_BCLK_to_and_from_the_musiccontroller_0;
   wire              AUD_DACDAT_from_the_musiccontroller_0;
   wire              AUD_DACLRCK_from_the_musiccontroller_0;
   wire              AUD_XCK_from_the_musiccontroller_0;
   wire      [ 17: 0] SRAM_ADDR_from_the_sram_mux_0;
   wire              SRAM_CE_N_from_the_sram_mux_0;
   wire      [ 15: 0] SRAM_DQ_to_and_from_the_sram_mux_0;
   wire              SRAM_LB_N_from_the_sram_mux_0;
   wire              SRAM_OE_N_from_the_sram_mux_0;
   wire              SRAM_UB_N_from_the_sram_mux_0;
   wire              SRAM_WE_N_from_the_sram_mux_0;
   wire      [ 17: 0] VGA_ADDR_to_the_sram_mux_0;
   wire      [ 15: 0] VGA_DQ_from_the_sram_mux_0;
   wire              VGA_OE_N_to_the_sram_mux_0;
   wire              VGA_WE_N_to_the_sram_mux_0;
   wire              clk;
   reg               clk_0;
   wire              clk_18_to_the_musiccontroller_0;
   wire      [ 11: 0] iX_COORD_to_the_xycoord_interface_0;
   wire      [ 11: 0] iY_COORD_to_the_xycoord_interface_0;
   wire              irq_adc_to_the_interrupt_0;
   wire              jtag_uart_0_avalon_jtag_slave_dataavailable_from_sa;
   wire              jtag_uart_0_avalon_jtag_slave_readyfordata_from_sa;
   wire      [ 31: 0] oMOLECTRL_from_the_command_0;
   wire      [ 31: 0] oPANELCTRL_from_the_command_0;
   reg               reset_n;
   wire      [ 11: 0] zs_addr_from_the_sdram_0;
   wire      [  1: 0] zs_ba_from_the_sdram_0;
   wire              zs_cas_n_from_the_sdram_0;
   wire              zs_cke_from_the_sdram_0;
   wire              zs_cs_n_from_the_sdram_0;
   wire      [ 15: 0] zs_dq_to_and_from_the_sdram_0;
   wire      [  1: 0] zs_dqm_from_the_sdram_0;
   wire              zs_ras_n_from_the_sdram_0;
   wire              zs_we_n_from_the_sdram_0;


// <ALTERA_NOTE> CODE INSERTED BETWEEN HERE
//    add your signals and additional architecture here
// AND HERE WILL BE PRESERVED </ALTERA_NOTE>

   //Set us up the Dut
   nios_system DUT
      (
        .AUD_ADCDAT_to_the_musiccontroller_0
(AUD_ADCDAT_to_the_musiccontroller_0),
        .AUD_ADCLRCK_from_the_musiccontroller_0
(AUD_ADCLRCK_from_the_musiccontroller_0),
        .AUD_BCLK_to_and_from_the_musiccontroller_0
(AUD_BCLK_to_and_from_the_musiccontroller_0),
        .AUD_DACDAT_from_the_musiccontroller_0
(AUD_DACDAT_from_the_musiccontroller_0),
        .AUD_DACLRCK_from_the_musiccontroller_0
```

```
(AUD_DACLRCK_from_the_musiccontroller_0),
        .AUD_XCK_from_the_musiccontroller_0
(AUD_XCK_from_the_musiccontroller_0),
        .SRAM_ADDR_from_the_sram_mux_0
(SRAM_ADDR_from_the_sram_mux_0),
        .SRAM_CE_N_from_the_sram_mux_0
(SRAM_CE_N_from_the_sram_mux_0),
        .SRAM_DQ_to_and_from_the_sram_mux_0
(SRAM_DQ_to_and_from_the_sram_mux_0),
        .SRAM_LB_N_from_the_sram_mux_0
(SRAM_LB_N_from_the_sram_mux_0),
        .SRAM_OE_N_from_the_sram_mux_0
(SRAM_OE_N_from_the_sram_mux_0),
        .SRAM_UB_N_from_the_sram_mux_0
(SRAM_UB_N_from_the_sram_mux_0),
        .SRAM_WE_N_from_the_sram_mux_0
(SRAM_WE_N_from_the_sram_mux_0),
        .VGA_ADDR_to_the_sram_mux_0
(VGA_ADDR_to_the_sram_mux_0),
        .VGA_DQ_from_the_sram_mux_0
(VGA_DQ_from_the_sram_mux_0),
        .VGA_OE_N_to_the_sram_mux_0
(VGA_OE_N_to_the_sram_mux_0),
        .VGA_WE_N_to_the_sram_mux_0
(VGA_WE_N_to_the_sram_mux_0),
        .clk_0                                  (clk_0),
        .clk_18_to_the_musiccontroller_0        (clk_18_to_the_musiccontroller_0),
        .iX_COORD_to_the_xycoord_interface_0
(iX_COORD_to_the_xycoord_interface_0),
        .iY_COORD_to_the_xycoord_interface_0
(iY_COORD_to_the_xycoord_interface_0),
        .irq_adc_to_the_interrupt_0             (irq_adc_to_the_interrupt_0),
        .oMOLECTRL_from_the_command_0
(oMOLECTRL_from_the_command_0),
        .oPANELCTRL_from_the_command_0
(oPANELCTRL_from_the_command_0),
        .reset_n                                (reset_n),
        .zs_addr_from_the_sdram_0               (zs_addr_from_the_sdram_0),
        .zs_ba_from_the_sdram_0                 (zs_ba_from_the_sdram_0),
        .zs_cas_n_from_the_sdram_0              (zs_cas_n_from_the_sdram_0),
        .zs_cke_from_the_sdram_0                (zs_cke_from_the_sdram_0),
        .zs_cs_n_from_the_sdram_0               (zs_cs_n_from_the_sdram_0),
        .zs_dq_to_and_from_the_sdram_0          (zs_dq_to_and_from_the_sdram_0),
        .zs_dqm_from_the_sdram_0                (zs_dqm_from_the_sdram_0),
        .zs_ras_n_from_the_sdram_0              (zs_ras_n_from_the_sdram_0),
        .zs_we_n_from_the_sdram_0               (zs_we_n_from_the_sdram_0)
    );

  initial
    clk_0 = 1'b0;
  always
    #10 clk_0 <= ~clk_0;

  initial
    begin
      reset_n <= 0;
      #200 reset_n <= 1;
    end
```

```
endmodule

//synthesis translate_on
```

Adc_spi_controller.v

```
module adc_spi_controller    (
                        iCLK,

                        iRST_n,
                        oADC_DIN,
                        oADC_DCLK,
                        oADC_CS,
                        iADC_DOUT,
                        iADC_BUSY,
                        iADC_PENIRQ_n,
                        oTOUCH_IRQ,
                        oX_COORD,
                        oY_COORD,
                        oNEW_COORD,
                        ////////////////////
                        );


//=============================================================================
// PARAMETER declarations
//=============================================================================

parameter SYSCLK_FRQ  = 50000000;
parameter ADC_DCLK_FRQ    = 1000;
```

```
parameter ADC_DCLK_CNT    = SYSCLK_FRQ/(ADC_DCLK_FRQ*2);


//=============================================================================
// PORT declarations
//=============================================================================
input                iCLK;
input                iRST_n;
input                iADC_DOUT;
input                iADC_PENIRQ_n;
input                iADC_BUSY;
output               oADC_DIN;
output               oADC_DCLK;
output               oADC_CS;
output               oTOUCH_IRQ;
output    [11:0]     oX_COORD;
output    [11:0]     oY_COORD;
output               oNEW_COORD;
//=============================================================================
// REG/WIRE declarations
//=============================================================================
reg                  d1_PENIRQ_n;
reg                  d2_PENIRQ_n;
wire            touch_irq;
reg       [15:0]     dclk_cnt;
wire            dclk;
reg                  transmit_en;
reg       [6:0] spi_ctrl_cnt;
wire            oADC_CS;
reg                  mcs;
```

```
reg                     mdclk;
wire [7:0] x_config_reg;
wire [7:0] y_config_reg;
wire [7:0] ctrl_reg;
reg      [7:0] mdata_in;
reg                     y_coordinate_config;
wire            eof_transmition;
reg      [5:0] bit_cnt;
reg                     madc_out;
reg      [11:0]     mx_coordinate;
reg      [11:0]     my_coordinate;
reg      [11:0]     oX_COORD;
reg      [11:0]     oY_COORD;
wire            rd_coord_strob;
reg                     oNEW_COORD;
reg      [5:0] irq_cnt;
reg      [15:0]     clk_cnt;
//=============================================================================
// Structural coding
//=============================================================================
assign     x_config_reg = 8'h92;
assign     y_config_reg = 8'hd2;

always@(posedge iCLK or negedge iRST_n)
    begin
        if (!iRST_n)
            madc_out <= 0;
        else
            madc_out <= iADC_DOUT;
```

```
    end

///////////////     pen irq detect    ////////
always@(posedge iCLK or negedge iRST_n)
    begin
        if (!iRST_n)
            begin
                d1_PENIRQ_n <= 0;
                d2_PENIRQ_n <= 0;
            end
        else
            begin
                d1_PENIRQ_n <= iADC_PENIRQ_n;
                d2_PENIRQ_n <= d1_PENIRQ_n;
            end
    end

// if iADC_PENIRQ_n form high to low , touch_irq goes high
assign          touch_irq = d2_PENIRQ_n & ~d1_PENIRQ_n;
assign          oTOUCH_IRQ = touch_irq;
// if touch_irq goes high , starting transmit procedure ,transmit_en goes high
// if end of transmition and no penirq , transmit procedure stop.

always@(posedge iCLK or negedge iRST_n)
    begin
        if (!iRST_n)
            transmit_en <= 0;
        else if (eof_transmition&&iADC_PENIRQ_n)
            transmit_en <= 0;
```

```
        else if (touch_irq)
            transmit_en <= 1;
    end

always@(posedge iCLK or negedge iRST_n)
    begin
        if (!iRST_n)
            dclk_cnt <= 0;
        else if (transmit_en)
            begin
                if (dclk_cnt == ADC_DCLK_CNT)
                    dclk_cnt <= 0;
                else
                    dclk_cnt <= dclk_cnt + 1;
            end
        else
            dclk_cnt <= 0;
    end

assign  dclk =  (dclk_cnt == ADC_DCLK_CNT)? 1 : 0;

always@(posedge iCLK or negedge iRST_n)
    begin
        if (!iRST_n)
            spi_ctrl_cnt <= 0;
        else if (dclk)
            begin
                if (spi_ctrl_cnt == 65)
                    spi_ctrl_cnt <= 0;
```

```
                else
                    spi_ctrl_cnt <= spi_ctrl_cnt + 1;
            end
    end

always@(posedge iCLK or negedge iRST_n)
    begin
        if (!iRST_n)
            begin
                mcs         <= 1;
                mdclk       <= 0;
                mdata_in <= 0;
                y_coordinate_config <= 0;
                mx_coordinate <= 0;
                my_coordinate <= 0;
            end
        else if (transmit_en)
            begin
                if (dclk)
                    begin
                        if (spi_ctrl_cnt == 0)
                            begin
                                mcs         <= 0;
                                mdata_in <= ctrl_reg;
                            end
                        else if (spi_ctrl_cnt == 49)
                            begin
                                mdclk       <= 0;
                                y_coordinate_config <= ~y_coordinate_config;
```

```
                        if (y_coordinate_config)
                            mcs     <= 1;
                        else
                            mcs     <= 0;
                    end
                else if (spi_ctrl_cnt != 0)
                    mdclk   <= ~mdclk;
                if (mdclk)
                    mdata_in <= {mdata_in[6:0],1'b0};
                if (!mdclk)
                    begin
                        if(rd_coord_strob)
                            begin
                                if(y_coordinate_config)
                                    my_coordinate                   <=
{my_coordinate[10:0],madc_out};
                                else
                                    mx_coordinate                   <=
{mx_coordinate[10:0],madc_out};
                            end
                    end
            end
        end
    end

assign  oADC_CS    = mcs;
assign  oADC_DIN =    mdata_in[7];
assign  oADC_DCLK = mdclk;
assign  ctrl_reg = y_coordinate_config ? y_config_reg : x_config_reg;
```

```
assign      eof_transmition = (y_coordinate_config & (spi_ctrl_cnt == 49) & dclk);

assign      rd_coord_strob = ((spi_ctrl_cnt>=19)&&(spi_ctrl_cnt<=41)) ? 1 : 0;

always@(posedge iCLK or negedge iRST_n)
      begin
            if (!iRST_n)
                  begin
                        oX_COORD <= 0;
                        oY_COORD <= 0;
                  end
            else if (eof_transmition&&(my_coordinate!=0))
                  begin
                        oX_COORD <= mx_coordinate;
                        oY_COORD <= my_coordinate;
                  end
      end

always@(posedge iCLK or negedge iRST_n)
      begin
            if (!iRST_n)
                  oNEW_COORD <= 0;
            else if (eof_transmition&&(my_coordinate!=0))
                  oNEW_COORD <= 1;
            else
                  oNEW_COORD <= 0;
      end
```

```
endmodule
```

Audio_controller.v

```
module audio_controller         (
                                clk,                    // LCD display clock
                                reset_n,                // systen reset
                                read,
                                write,
                                chipselect,
                                address,
                                readdata,
                                writedata
                                );


input           clk;
input           reset_n;
input           read;
input           write;
input           chipselect;
input [4:0]address;
output [15:0]readdata;
input [15:0]writedata;

endmodule
```

Command.v

```
module command(
                clk,
                reset_n,
                chipselect,
                read,
                write,
                address,
                readdata,
                writedata,
                oMOLECTRL,
                oPANELCTRL
                );

//================================
//IO PORT
//================================
input clk;
input reset_n;
input chipselect;
input read;
input write;
input [4:0] address;
output [31:0] readdata;
input [31:0] writedata;
```

```
output [31:0]oMOLECTRL;
output [31:0]oPANELCTRL;

//====================================
//REG and WIRE
//====================================
reg [31:0] mole;
reg [31:0] panel;



//====================================
//STRUCTURE LOGIC
//====================================
always@(posedge clk or negedge reset_n)
begin
	if(!reset_n)
		begin
			mole <= 0;
			panel <= 0;
		end
	else if (chipselect)
		begin
			if(write)
			begin
				if(address == 5'b00000)
					panel <= writedata;
				else if(address == 5'b00001)
					mole <= writedata;
			end
		end
end

assign oMOLECTRL = mole;
assign oPANELCTRL = panel;

endmodule
```

Control_panel.v

```
module control_panel(
xcount,
ycount,

)

endmodule
```

Cpu_0.v

```
//Legal Notice: (C)2013 Altera Corporation. All rights reserved.  Your
//use of Altera Corporation's design tools, logic functions and other
//software and tools, and its AMPP partner logic functions, and any
//output files any of the foregoing (including device programming or
//simulation files), and any associated documentation or information are
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```
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//License Subscription Agreement or other applicable license agreement,
//including, without limitation, that your use is for the sole purpose
//of programming logic devices manufactured by Altera and sold by Altera
//or its authorized distributors.  Please refer to the applicable
//agreement for further details.

// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_register_bank_a_module (
                                      // inputs:
                                       clock,
                                       data,
                                       rdaddress,
                                       wraddress,
                                       wren,

                                      // outputs:
                                       q
                                    )
;

  parameter lpm_file = "UNUSED";


  output  [ 31: 0] q;
  input            clock;
  input   [ 31: 0] data;
  input   [  4: 0] rdaddress;
  input   [  4: 0] wraddress;
  input            wren;

  wire    [ 31: 0] q;
  wire    [ 31: 0] ram_q;
  assign q = ram_q;
  altsyncram the_altsyncram
    (
      .address_a (wraddress),
      .address_b (rdaddress),
      .clock0 (clock),
      .data_a (data),
      .q_b (ram_q),
      .wren_a (wren)
    );

  defparam the_altsyncram.address_reg_b = "CLOCK0",
           the_altsyncram.init_file = lpm_file,
           the_altsyncram.maximum_depth = 0,
           the_altsyncram.numwords_a = 32,
           the_altsyncram.numwords_b = 32,
           the_altsyncram.operation_mode = "DUAL_PORT",
           the_altsyncram.outdata_reg_b = "UNREGISTERED",
```

```
                the_altsyncram.ram_block_type = "AUTO",
                the_altsyncram.rdcontrol_reg_b = "CLOCK0",
                the_altsyncram.read_during_write_mode_mixed_ports = "DONT_CARE",
                the_altsyncram.width_a = 32,
                the_altsyncram.width_b = 32,
                the_altsyncram.widthad_a = 5,
                the_altsyncram.widthad_b = 5;


endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_register_bank_b_module (
                                                    // inputs:
                                                      clock,
                                                      data,
                                                      rdaddress,
                                                      wraddress,
                                                      wren,

                                                    // outputs:
                                                      q
                                                   )
;

   parameter lpm_file = "UNUSED";


   output    [ 31: 0] q;
   input              clock;
   input     [ 31: 0] data;
   input     [  4: 0] rdaddress;
   input     [  4: 0] wraddress;
   input              wren;

   wire      [ 31: 0] q;
   wire      [ 31: 0] ram_q;
   assign q = ram_q;
   altsyncram the_altsyncram
     (
       .address_a (wraddress),
       .address_b (rdaddress),
       .clock0 (clock),
       .data_a (data),
       .q_b (ram_q),
       .wren_a (wren)
     );

   defparam the_altsyncram.address_reg_b = "CLOCK0",
                the_altsyncram.init_file = lpm_file,
```

```
                the_altsyncram.maximum_depth = 0,
                the_altsyncram.numwords_a = 32,
                the_altsyncram.numwords_b = 32,
                the_altsyncram.operation_mode = "DUAL_PORT",
                the_altsyncram.outdata_reg_b = "UNREGISTERED",
                the_altsyncram.ram_block_type = "AUTO",
                the_altsyncram.rdcontrol_reg_b = "CLOCK0",
                the_altsyncram.read_during_write_mode_mixed_ports = "DONT_CARE",
                the_altsyncram.width_a = 32,
                the_altsyncram.width_b = 32,
                the_altsyncram.widthad_a = 5,
                the_altsyncram.widthad_b = 5;


endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci_debug (
                                        // inputs:
                                          clk,
                                          dbrk_break,
                                          debugreq,
                                          hbreak_enabled,
                                          jdo,
                                          jrst_n,
                                          ocireg_ers,
                                          ocireg_mrs,
                                          reset,
                                          st_ready_test_idle,
                                          take_action_ocimem_a,
                                          take_action_ocireg,
                                          xbrk_break,

                                        // outputs:
                                          debugack,
                                          monitor_error,
                                          monitor_go,
                                          monitor_ready,
                                          oci_hbreak_req,
                                          resetlatch,
                                          resetrequest
                                       )
;

  output           debugack;
  output           monitor_error;
  output           monitor_go;
  output           monitor_ready;
  output           oci_hbreak_req;
  output           resetlatch;
```

```
  output              resetrequest;
  input               clk;
  input               dbrk_break;
  input               debugreq;
  input               hbreak_enabled;
  input    [ 37: 0] jdo;
  input               jrst_n;
  input               ocireg_ers;
  input               ocireg_mrs;
  input               reset;
  input               st_ready_test_idle;
  input               take_action_ocimem_a;
  input               take_action_ocireg;
  input               xbrk_break;

  wire                debugack;
  reg                                 jtag_break   /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,R101\"" */;
  reg                               monitor_error  /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=D101" */;
  reg                                 monitor_go   /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=D101" */;
  reg                               monitor_ready  /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=D101" */;
  wire                oci_hbreak_req;
  reg                                 probepresent /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,R101\"" */;
  reg                                   resetlatch /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,R101\"" */;
  reg                                 resetrequest /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,R101\"" */;
  always @(posedge clk or negedge jrst_n)
    begin
      if (jrst_n == 0)
        begin
          probepresent <= 1'b0;
          resetrequest <= 1'b0;
          jtag_break <= 1'b0;
        end
      else if (take_action_ocimem_a)
        begin
          resetrequest <= jdo[22];
          jtag_break <= jdo[21]       ? 1
                      : jdo[20]    ? 0
                      : jtag_break;

          probepresent <= jdo[19]       ? 1
                      : jdo[18]    ? 0
                      :    probepresent;

          resetlatch <= jdo[24] ? 0 : resetlatch;
        end
      else if (reset)
        begin
          jtag_break <= probepresent;
          resetlatch <= 1;
        end
      else if (~debugack & debugreq & probepresent)
```

```
                jtag_break <= 1'b1;
        end


    always @(posedge clk or negedge jrst_n)
        begin
            if (jrst_n == 0)
                begin
                    monitor_ready <= 1'b0;
                    monitor_error <= 1'b0;
                    monitor_go <= 1'b0;
                end
            else
                begin
                    if (take_action_ocimem_a && jdo[25])
                            monitor_ready <= 1'b0;
                    else if (take_action_ocireg && ocireg_mrs)
                            monitor_ready <= 1'b1;
                    if (take_action_ocimem_a && jdo[25])
                            monitor_error <= 1'b0;
                    else if (take_action_ocireg && ocireg_ers)
                            monitor_error <= 1'b1;
                    if (take_action_ocimem_a && jdo[23])
                            monitor_go <= 1'b1;
                    else if (st_ready_test_idle)
                            monitor_go <= 1'b0;
                end
        end


    assign oci_hbreak_req = jtag_break | dbrk_break | xbrk_break | debugreq;
    assign debugack = ~hbreak_enabled;

endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_ociram_lpm_dram_bdp_component_module (
                                                                        // inputs:
                                                                          address_a,
                                                                          address_b,
                                                                          byteena_a,
                                                                          clock0,
                                                                          clock1,
                                                                          clocken0,
                                                                          clocken1,
                                                                          data_a,
                                                                          data_b,
                                                                          wren_a,
                                                                          wren_b,
```

```
                                                                    // outputs:
                                                                      q_a,
                                                                      q_b
                                                                   )
;

   parameter lpm_file = "UNUSED";


   output    [ 31: 0] q_a;
   output    [ 31: 0] q_b;
   input     [    7: 0] address_a;
   input     [    7: 0] address_b;
   input     [    3: 0] byteena_a;
   input                clock0;
   input                clock1;
   input                clocken0;
   input                clocken1;
   input     [ 31: 0] data_a;
   input     [ 31: 0] data_b;
   input                wren_a;
   input                wren_b;

   wire      [ 31: 0] q_a;
   wire      [ 31: 0] q_b;
   altsyncram the_altsyncram
     (
       .address_a (address_a),
       .address_b (address_b),
       .byteena_a (byteena_a),
       .clock0 (clock0),
       .clock1 (clock1),
       .clocken0 (clocken0),
       .clocken1 (clocken1),
       .data_a (data_a),
       .data_b (data_b),
       .q_a (q_a),
       .q_b (q_b),
       .wren_a (wren_a),
       .wren_b (wren_b)
     );

   defparam the_altsyncram.address_aclr_a = "NONE",
            the_altsyncram.address_aclr_b = "NONE",
            the_altsyncram.address_reg_b = "CLOCK1",
            the_altsyncram.indata_aclr_a = "NONE",
            the_altsyncram.indata_aclr_b = "NONE",
            the_altsyncram.init_file = lpm_file,
            the_altsyncram.intended_device_family = "CYCLONEII",
            the_altsyncram.lpm_type = "altsyncram",
            the_altsyncram.numwords_a = 256,
            the_altsyncram.numwords_b = 256,
            the_altsyncram.operation_mode = "BIDIR_DUAL_PORT",
            the_altsyncram.outdata_aclr_a = "NONE",
            the_altsyncram.outdata_aclr_b = "NONE",
            the_altsyncram.outdata_reg_a = "UNREGISTERED",
            the_altsyncram.outdata_reg_b = "UNREGISTERED",
            the_altsyncram.ram_block_type = "AUTO",
```

```
                the_altsyncram.read_during_write_mode_mixed_ports = "OLD_DATA",
                the_altsyncram.width_a = 32,
                the_altsyncram.width_b = 32,
                the_altsyncram.width_byteena_a = 4,
                the_altsyncram.widthad_a = 8,
                the_altsyncram.widthad_b = 8,
                the_altsyncram.wrcontrol_aclr_a = "NONE",
                the_altsyncram.wrcontrol_aclr_b = "NONE";


endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_ocimem (
                                    // inputs:
                                      address,
                                      begintransfer,
                                      byteenable,
                                      chipselect,
                                      clk,
                                      debugaccess,
                                      jdo,
                                      jrst_n,
                                      resetrequest,
                                      take_action_ocimem_a,
                                      take_action_ocimem_b,
                                      take_no_action_ocimem_a,
                                      write,
                                      writedata,

                                    // outputs:
                                      MonDReg,
                                      oci_ram_readdata
                                   )
;

  output  [ 31: 0] MonDReg;
  output  [ 31: 0] oci_ram_readdata;
  input   [  8: 0] address;
  input            begintransfer;
  input   [  3: 0] byteenable;
  input            chipselect;
  input            clk;
  input            debugaccess;
  input   [ 37: 0] jdo;
  input            jrst_n;
  input            resetrequest;
  input            take_action_ocimem_a;
  input            take_action_ocimem_b;
  input            take_no_action_ocimem_a;
```

```
  input                  write;
  input     [ 31: 0] writedata;

  reg                  [  10:  0] MonAReg /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,D103,R101\"" */;
  reg                  [  31:  0] MonDReg /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,D103,R101\"" */;
  reg                                     MonRd /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,D103,R101\"" */;
  reg                                    MonRd1 /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,D103,R101\"" */;
  reg                                     MonWr /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,D103,R101\"" */;
  wire                   avalon;
  wire      [ 31: 0] cfgdout;
  wire      [ 31: 0] oci_ram_readdata;
  wire      [ 31: 0] sramdout;
  assign avalon = begintransfer & ~resetrequest;
  always @(posedge clk or negedge jrst_n)
    begin
      if (jrst_n == 0)
        begin
          MonWr <= 1'b0;
          MonRd <= 1'b0;
          MonRd1 <= 1'b0;
          MonAReg <= 0;
          MonDReg <= 0;
        end
      else
        begin
          if (take_no_action_ocimem_a)
            begin
              MonAReg[10 : 2] <= MonAReg[10 : 2]+1;
              MonRd <= 1'b1;
            end
          else if (take_action_ocimem_a)
            begin
              MonAReg[10 : 2] <= { jdo[17],
                                   jdo[33 : 26] };

              MonRd <= 1'b1;
            end
          else if (take_action_ocimem_b)
            begin
              MonAReg[10 : 2] <= MonAReg[10 : 2]+1;
              MonDReg <= jdo[34 : 3];
              MonWr <= 1'b1;
            end
          else
            begin
              if (~avalon)
                begin
                  MonWr <= 0;
                  MonRd <= 0;
                end
              if (MonRd1)
                  MonDReg <= MonAReg[10] ? cfgdout : sramdout;
            end
```

```
            MonRd1 <= MonRd;
          end
      end


//cpu_0_ociram_lpm_dram_bdp_component, which is an nios_tdp_ram
cpu_0_ociram_lpm_dram_bdp_component_module cpu_0_ociram_lpm_dram_bdp_component
   (
      .address_a (address[7 : 0]),
      .address_b (MonAReg[9 : 2]),
      .byteena_a (byteenable),
      .clock0    (clk),
      .clock1    (clk),
      .clocken0  (1'b1),
      .clocken1  (1'b1),
      .data_a    (writedata),
      .data_b    (MonDReg[31 : 0]),
      .q_a       (oci_ram_readdata),
      .q_b       (sramdout),
      .wren_a    (chipselect & write & debugaccess &
                              ~address[8]
                              ),
      .wren_b    (MonWr)
   );

//synthesis translate_off
`ifdef NO_PLI
defparam                cpu_0_ociram_lpm_dram_bdp_component.lpm_file                =
"cpu_0_ociram_default_contents.dat";
`else
defparam                cpu_0_ociram_lpm_dram_bdp_component.lpm_file                =
"cpu_0_ociram_default_contents.hex";
`endif
//synthesis translate_on
//synthesis read_comments_as_HDL on
//defparam                cpu_0_ociram_lpm_dram_bdp_component.lpm_file                =
"cpu_0_ociram_default_contents.mif";
//synthesis read_comments_as_HDL off
   assign cfgdout = (MonAReg[4 : 2] == 3'd0)? 32'h00800020 :
      (MonAReg[4 : 2] == 3'd1)? 32'h00001919 :
      (MonAReg[4 : 2] == 3'd2)? 32'h00040000 :
      (MonAReg[4 : 2] == 3'd3)? 32'h00000000 :
      (MonAReg[4 : 2] == 3'd4)? 32'h20000000 :
      (MonAReg[4 : 2] == 3'd5)? 32'h00800000 :
      (MonAReg[4 : 2] == 3'd6)? 32'h00000000 :
      32'h00000000;


endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030
```

```
module cpu_0_nios2_avalon_reg (
                                        // inputs:
                                          address,
                                          chipselect,
                                          clk,
                                          debugaccess,
                                          monitor_error,
                                          monitor_go,
                                          monitor_ready,
                                          reset_n,
                                          write,
                                          writedata,

                                        // outputs:
                                          oci_ienable,
                                          oci_reg_readdata,
                                          oci_single_step_mode,
                                          ocireg_ers,
                                          ocireg_mrs,
                                          take_action_ocireg
                                       )
;

  output  [ 31: 0] oci_ienable;
  output  [ 31: 0] oci_reg_readdata;
  output           oci_single_step_mode;
  output           ocireg_ers;
  output           ocireg_mrs;
  output           take_action_ocireg;
  input   [  8: 0] address;
  input            chipselect;
  input            clk;
  input            debugaccess;
  input            monitor_error;
  input            monitor_go;
  input            monitor_ready;
  input            reset_n;
  input            write;
  input   [ 31: 0] writedata;

  reg     [ 31: 0] oci_ienable;
  wire             oci_reg_00_addressed;
  wire             oci_reg_01_addressed;
  wire    [ 31: 0] oci_reg_readdata;
  reg              oci_single_step_mode;
  wire             ocireg_ers;
  wire             ocireg_mrs;
  wire             ocireg_sstep;
  wire             take_action_oci_intr_mask_reg;
  wire             take_action_ocireg;
  wire             write_strobe;
  assign oci_reg_00_addressed = address == 9'h100;
  assign oci_reg_01_addressed = address == 9'h101;
  assign write_strobe = chipselect & write & debugaccess;
  assign take_action_ocireg = write_strobe & oci_reg_00_addressed;
  assign take_action_oci_intr_mask_reg = write_strobe & oci_reg_01_addressed;
  assign ocireg_ers = writedata[1];
```

```
  assign ocireg_mrs = writedata[0];
  assign ocireg_sstep = writedata[3];
  assign oci_reg_readdata = oci_reg_00_addressed ? {28'b0, oci_single_step_mode, monitor_go,
      monitor_ready, monitor_error} :
      oci_reg_01_addressed ?  oci_ienable :
      32'b0;

  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          oci_single_step_mode <= 1'b0;
      else if (take_action_ocireg)
          oci_single_step_mode <= ocireg_sstep;
    end


  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          oci_ienable <= 32'b00000000000000000000000000000111;
      else if (take_action_oci_intr_mask_reg)
          oci_ienable <= writedata | ~(32'b00000000000000000000000000000111);
    end



endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci_break (
                               // inputs:
                                 clk,
                                 dbrk_break,
                                 dbrk_goto0,
                                 dbrk_goto1,
                                 jdo,
                                 jrst_n,
                                 reset_n,
                                 take_action_break_a,
                                 take_action_break_b,
                                 take_action_break_c,
                                 take_no_action_break_a,
                                 take_no_action_break_b,
                                 take_no_action_break_c,
                                 xbrk_goto0,
                                 xbrk_goto1,

                               // outputs:
                                 break_readreg,
```

```
                                        dbrk_hit0_latch,
                                        dbrk_hit1_latch,
                                        dbrk_hit2_latch,
                                        dbrk_hit3_latch,
                                        trigbrktype,
                                        trigger_state_0,
                                        trigger_state_1,
                                        xbrk_ctrl0,
                                        xbrk_ctrl1,
                                        xbrk_ctrl2,
                                        xbrk_ctrl3
                                    )
;

   output    [ 31: 0] break_readreg;
   output             dbrk_hit0_latch;
   output             dbrk_hit1_latch;
   output             dbrk_hit2_latch;
   output             dbrk_hit3_latch;
   output             trigbrktype;
   output             trigger_state_0;
   output             trigger_state_1;
   output    [  7: 0] xbrk_ctrl0;
   output    [  7: 0] xbrk_ctrl1;
   output    [  7: 0] xbrk_ctrl2;
   output    [  7: 0] xbrk_ctrl3;
   input              clk;
   input              dbrk_break;
   input              dbrk_goto0;
   input              dbrk_goto1;
   input     [ 37: 0] jdo;
   input              jrst_n;
   input              reset_n;
   input              take_action_break_a;
   input              take_action_break_b;
   input              take_action_break_c;
   input              take_no_action_break_a;
   input              take_no_action_break_b;
   input              take_no_action_break_c;
   input              xbrk_goto0;
   input              xbrk_goto1;

   wire      [  3: 0] break_a_wpr;
   wire      [  1: 0] break_a_wpr_high_bits;
   wire      [  1: 0] break_a_wpr_low_bits;
   wire      [  1: 0] break_b_rr;
   wire      [  1: 0] break_c_rr;
   reg       [ 31: 0] break_readreg /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,R101\"" */;
   wire               dbrk0_high_value;
   wire               dbrk0_low_value;
   wire               dbrk1_high_value;
   wire               dbrk1_low_value;
   wire               dbrk2_high_value;
   wire               dbrk2_low_value;
   wire               dbrk3_high_value;
   wire               dbrk3_low_value;
   wire               dbrk_hit0_latch;
```

```
  wire              dbrk_hit1_latch;
  wire              dbrk_hit2_latch;
  wire              dbrk_hit3_latch;
  wire              take_action_any_break;
  reg                                   trigbrktype /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,R101\"" */;
  reg               trigger_state;
  wire              trigger_state_0;
  wire              trigger_state_1;
  wire    [ 31: 0] xbrk0_value;
  wire    [ 31: 0] xbrk1_value;
  wire    [ 31: 0] xbrk2_value;
  wire    [ 31: 0] xbrk3_value;
  reg               [    7:    0]   xbrk_ctrl0   /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,R101\"" */;
  reg               [    7:    0]   xbrk_ctrl1   /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,R101\"" */;
  reg               [    7:    0]   xbrk_ctrl2   /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,R101\"" */;
  reg               [    7:    0]   xbrk_ctrl3   /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,R101\"" */;
  assign break_a_wpr = jdo[35 : 32];
  assign break_a_wpr_high_bits = break_a_wpr[3 : 2];
  assign break_a_wpr_low_bits = break_a_wpr[1 : 0];
  assign break_b_rr = jdo[33 : 32];
  assign break_c_rr = jdo[33 : 32];
  assign take_action_any_break = take_action_break_a | take_action_break_b |
take_action_break_c;
  always @(posedge clk or negedge jrst_n)
    begin
      if (jrst_n == 0)
        begin
          xbrk_ctrl0 <= 0;
          xbrk_ctrl1 <= 0;
          xbrk_ctrl2 <= 0;
          xbrk_ctrl3 <= 0;
          trigbrktype <= 0;
        end
      else
        begin
          if (take_action_any_break)
              trigbrktype <= 0;
          else if (dbrk_break)
              trigbrktype <= 1;
          if (take_action_break_b)
            begin
              if ((break_b_rr == 2'b00) && (0 >= 1))
                begin
                  xbrk_ctrl0[0] <= jdo[27];
                  xbrk_ctrl0[1] <= jdo[28];
                  xbrk_ctrl0[2] <= jdo[29];
                  xbrk_ctrl0[3] <= jdo[30];
                  xbrk_ctrl0[4] <= jdo[21];
                  xbrk_ctrl0[5] <= jdo[20];
                  xbrk_ctrl0[6] <= jdo[19];
                  xbrk_ctrl0[7] <= jdo[18];
                end
              if ((break_b_rr == 2'b01) && (0 >= 2))
```

```
                    begin
                        xbrk_ctrl1[0] <= jdo[27];
                        xbrk_ctrl1[1] <= jdo[28];
                        xbrk_ctrl1[2] <= jdo[29];
                        xbrk_ctrl1[3] <= jdo[30];
                        xbrk_ctrl1[4] <= jdo[21];
                        xbrk_ctrl1[5] <= jdo[20];
                        xbrk_ctrl1[6] <= jdo[19];
                        xbrk_ctrl1[7] <= jdo[18];
                    end
                if ((break_b_rr == 2'b10) && (0 >= 3))
                    begin
                        xbrk_ctrl2[0] <= jdo[27];
                        xbrk_ctrl2[1] <= jdo[28];
                        xbrk_ctrl2[2] <= jdo[29];
                        xbrk_ctrl2[3] <= jdo[30];
                        xbrk_ctrl2[4] <= jdo[21];
                        xbrk_ctrl2[5] <= jdo[20];
                        xbrk_ctrl2[6] <= jdo[19];
                        xbrk_ctrl2[7] <= jdo[18];
                    end
                if ((break_b_rr == 2'b11) && (0 >= 4))
                    begin
                        xbrk_ctrl3[0] <= jdo[27];
                        xbrk_ctrl3[1] <= jdo[28];
                        xbrk_ctrl3[2] <= jdo[29];
                        xbrk_ctrl3[3] <= jdo[30];
                        xbrk_ctrl3[4] <= jdo[21];
                        xbrk_ctrl3[5] <= jdo[20];
                        xbrk_ctrl3[6] <= jdo[19];
                        xbrk_ctrl3[7] <= jdo[18];
                    end
            end
        end
    end


assign dbrk_hit0_latch = 1'b0;
assign dbrk0_low_value = 0;
assign dbrk0_high_value = 0;
assign dbrk_hit1_latch = 1'b0;
assign dbrk1_low_value = 0;
assign dbrk1_high_value = 0;
assign dbrk_hit2_latch = 1'b0;
assign dbrk2_low_value = 0;
assign dbrk2_high_value = 0;
assign dbrk_hit3_latch = 1'b0;
assign dbrk3_low_value = 0;
assign dbrk3_high_value = 0;
assign xbrk0_value = 32'b0;
assign xbrk1_value = 32'b0;
assign xbrk2_value = 32'b0;
assign xbrk3_value = 32'b0;
always @(posedge clk or negedge jrst_n)
    begin
        if (jrst_n == 0)
            break_readreg <= 32'b0;
        else if (take_action_any_break)
```

```
        break_readreg <= jdo[31 : 0];
    else if (take_no_action_break_a)
        case (break_a_wpr_high_bits)

            2'd0: begin
                case (break_a_wpr_low_bits) // synthesis full_case

                    2'd0: begin
                        break_readreg <= xbrk0_value;
                    end // 2'd0

                    2'd1: begin
                        break_readreg <= xbrk1_value;
                    end // 2'd1

                    2'd2: begin
                        break_readreg <= xbrk2_value;
                    end // 2'd2

                    2'd3: begin
                        break_readreg <= xbrk3_value;
                    end // 2'd3

                endcase // break_a_wpr_low_bits
            end // 2'd0

            2'd1: begin
                break_readreg <= 32'b0;
            end // 2'd1

            2'd2: begin
                case (break_a_wpr_low_bits) // synthesis full_case

                    2'd0: begin
                        break_readreg <= dbrk0_low_value;
                    end // 2'd0

                    2'd1: begin
                        break_readreg <= dbrk1_low_value;
                    end // 2'd1

                    2'd2: begin
                        break_readreg <= dbrk2_low_value;
                    end // 2'd2

                    2'd3: begin
                        break_readreg <= dbrk3_low_value;
                    end // 2'd3

                endcase // break_a_wpr_low_bits
            end // 2'd2

            2'd3: begin
                case (break_a_wpr_low_bits) // synthesis full_case

                    2'd0: begin
                        break_readreg <= dbrk0_high_value;
                    end // 2'd0
```

```
                                2'd1: begin
                                      break_readreg <= dbrk1_high_value;
                                end // 2'd1

                                2'd2: begin
                                      break_readreg <= dbrk2_high_value;
                                end // 2'd2

                                2'd3: begin
                                      break_readreg <= dbrk3_high_value;
                                end // 2'd3

                          endcase // break_a_wpr_low_bits
                    end // 2'd3

              endcase // break_a_wpr_high_bits
        else if (take_no_action_break_b)
              break_readreg <= jdo[31 : 0];
        else if (take_no_action_break_c)
              break_readreg <= jdo[31 : 0];
      end


   always @(posedge clk or negedge reset_n)
      begin
        if (reset_n == 0)
              trigger_state <= 0;
        else if (trigger_state_1 & (xbrk_goto0 | dbrk_goto0))
              trigger_state <= 0;
        else if (trigger_state_0 & (xbrk_goto1 | dbrk_goto1))
              trigger_state <= -1;
      end


   assign trigger_state_0 = ~trigger_state;
   assign trigger_state_1 = trigger_state;

endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci_xbrk (
                                          // inputs:
                                            D_valid,
                                            E_valid,
                                            F_pc,
                                            clk,
                                            reset_n,
                                            trigger_state_0,
                                            trigger_state_1,
```

```
                                    xbrk_ctrl0,
                                    xbrk_ctrl1,
                                    xbrk_ctrl2,
                                    xbrk_ctrl3,

                                   // outputs:
                                    xbrk_break,
                                    xbrk_goto0,
                                    xbrk_goto1,
                                    xbrk_traceoff,
                                    xbrk_traceon,
                                    xbrk_trigout
                                  )
;

  output            xbrk_break;
  output            xbrk_goto0;
  output            xbrk_goto1;
  output            xbrk_traceoff;
  output            xbrk_traceon;
  output            xbrk_trigout;
  input             D_valid;
  input             E_valid;
  input     [ 22: 0] F_pc;
  input             clk;
  input             reset_n;
  input             trigger_state_0;
  input             trigger_state_1;
  input     [  7: 0] xbrk_ctrl0;
  input     [  7: 0] xbrk_ctrl1;
  input     [  7: 0] xbrk_ctrl2;
  input     [  7: 0] xbrk_ctrl3;

  wire              D_cpu_addr_en;
  wire              E_cpu_addr_en;
  reg               E_xbrk_goto0;
  reg               E_xbrk_goto1;
  reg               E_xbrk_traceoff;
  reg               E_xbrk_traceon;
  reg               E_xbrk_trigout;
  wire      [ 24: 0] cpu_i_address;
  wire              xbrk0_armed;
  wire              xbrk0_break_hit;
  wire              xbrk0_goto0_hit;
  wire              xbrk0_goto1_hit;
  wire              xbrk0_toff_hit;
  wire              xbrk0_ton_hit;
  wire              xbrk0_tout_hit;
  wire              xbrk1_armed;
  wire              xbrk1_break_hit;
  wire              xbrk1_goto0_hit;
  wire              xbrk1_goto1_hit;
  wire              xbrk1_toff_hit;
  wire              xbrk1_ton_hit;
  wire              xbrk1_tout_hit;
  wire              xbrk2_armed;
  wire              xbrk2_break_hit;
  wire              xbrk2_goto0_hit;
```

```
  wire            xbrk2_goto1_hit;
  wire            xbrk2_toff_hit;
  wire            xbrk2_ton_hit;
  wire            xbrk2_tout_hit;
  wire            xbrk3_armed;
  wire            xbrk3_break_hit;
  wire            xbrk3_goto0_hit;
  wire            xbrk3_goto1_hit;
  wire            xbrk3_toff_hit;
  wire            xbrk3_ton_hit;
  wire            xbrk3_tout_hit;
  reg             xbrk_break;
  wire            xbrk_break_hit;
  wire            xbrk_goto0;
  wire            xbrk_goto0_hit;
  wire            xbrk_goto1;
  wire            xbrk_goto1_hit;
  wire            xbrk_toff_hit;
  wire            xbrk_ton_hit;
  wire            xbrk_tout_hit;
  wire            xbrk_traceoff;
  wire            xbrk_traceon;
  wire            xbrk_trigout;
  assign cpu_i_address = {F_pc, 2'b00};
  assign D_cpu_addr_en = D_valid;
  assign E_cpu_addr_en = E_valid;
  assign xbrk0_break_hit = 0;
  assign xbrk0_ton_hit = 0;
  assign xbrk0_toff_hit = 0;
  assign xbrk0_tout_hit = 0;
  assign xbrk0_goto0_hit = 0;
  assign xbrk0_goto1_hit = 0;
  assign xbrk1_break_hit = 0;
  assign xbrk1_ton_hit = 0;
  assign xbrk1_toff_hit = 0;
  assign xbrk1_tout_hit = 0;
  assign xbrk1_goto0_hit = 0;
  assign xbrk1_goto1_hit = 0;
  assign xbrk2_break_hit = 0;
  assign xbrk2_ton_hit = 0;
  assign xbrk2_toff_hit = 0;
  assign xbrk2_tout_hit = 0;
  assign xbrk2_goto0_hit = 0;
  assign xbrk2_goto1_hit = 0;
  assign xbrk3_break_hit = 0;
  assign xbrk3_ton_hit = 0;
  assign xbrk3_toff_hit = 0;
  assign xbrk3_tout_hit = 0;
  assign xbrk3_goto0_hit = 0;
  assign xbrk3_goto1_hit = 0;
  assign xbrk_break_hit = (xbrk0_break_hit) | (xbrk1_break_hit) | (xbrk2_break_hit) |
(xbrk3_break_hit);
  assign xbrk_ton_hit = (xbrk0_ton_hit) | (xbrk1_ton_hit) | (xbrk2_ton_hit) | (xbrk3_ton_hit);
  assign xbrk_toff_hit = (xbrk0_toff_hit) | (xbrk1_toff_hit) | (xbrk2_toff_hit) | (xbrk3_toff_hit);
  assign xbrk_tout_hit = (xbrk0_tout_hit) | (xbrk1_tout_hit) | (xbrk2_tout_hit) |
(xbrk3_tout_hit);
  assign xbrk_goto0_hit = (xbrk0_goto0_hit) | (xbrk1_goto0_hit) | (xbrk2_goto0_hit) |
(xbrk3_goto0_hit);
```

```
  assign xbrk_goto1_hit = (xbrk0_goto1_hit) | (xbrk1_goto1_hit) | (xbrk2_goto1_hit) |
(xbrk3_goto1_hit);
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            xbrk_break <= 0;
      else if (E_cpu_addr_en)
            xbrk_break <= xbrk_break_hit;
    end


  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            E_xbrk_traceon <= 0;
      else if (E_cpu_addr_en)
            E_xbrk_traceon <= xbrk_ton_hit;
    end


  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            E_xbrk_traceoff <= 0;
      else if (E_cpu_addr_en)
            E_xbrk_traceoff <= xbrk_toff_hit;
    end


  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            E_xbrk_trigout <= 0;
      else if (E_cpu_addr_en)
            E_xbrk_trigout <= xbrk_tout_hit;
    end


  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            E_xbrk_goto0 <= 0;
      else if (E_cpu_addr_en)
            E_xbrk_goto0 <= xbrk_goto0_hit;
    end


  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            E_xbrk_goto1 <= 0;
      else if (E_cpu_addr_en)
            E_xbrk_goto1 <= xbrk_goto1_hit;
    end


  assign xbrk_traceon = 1'b0;
  assign xbrk_traceoff = 1'b0;
```

```
  assign xbrk_trigout = 1'b0;
  assign xbrk_goto0 = 1'b0;
  assign xbrk_goto1 = 1'b0;
  assign xbrk0_armed = (xbrk_ctrl0[4] & trigger_state_0) ||
    (xbrk_ctrl0[5] & trigger_state_1);

  assign xbrk1_armed = (xbrk_ctrl1[4] & trigger_state_0) ||
    (xbrk_ctrl1[5] & trigger_state_1);

  assign xbrk2_armed = (xbrk_ctrl2[4] & trigger_state_0) ||
    (xbrk_ctrl2[5] & trigger_state_1);

  assign xbrk3_armed = (xbrk_ctrl3[4] & trigger_state_0) ||
    (xbrk_ctrl3[5] & trigger_state_1);


endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci_dbrk (
                              // inputs:
                                E_st_data,
                                av_ld_data_aligned_filtered,
                                clk,
                                d_address,
                                d_read,
                                d_waitrequest,
                                d_write,
                                debugack,
                                reset_n,

                              // outputs:
                                cpu_d_address,
                                cpu_d_read,
                                cpu_d_readdata,
                                cpu_d_wait,
                                cpu_d_write,
                                cpu_d_writedata,
                                dbrk_break,
                                dbrk_goto0,
                                dbrk_goto1,
                                dbrk_traceme,
                                dbrk_traceoff,
                                dbrk_traceon,
                                dbrk_trigout
                             )
;

  output  [ 24: 0] cpu_d_address;
  output           cpu_d_read;
```

```
output   [ 31: 0] cpu_d_readdata;
output            cpu_d_wait;
output            cpu_d_write;
output   [ 31: 0] cpu_d_writedata;
output            dbrk_break;
output            dbrk_goto0;
output            dbrk_goto1;
output            dbrk_traceme;
output            dbrk_traceoff;
output            dbrk_traceon;
output            dbrk_trigout;
input    [ 31: 0] E_st_data;
input    [ 31: 0] av_ld_data_aligned_filtered;
input             clk;
input    [ 24: 0] d_address;
input             d_read;
input             d_waitrequest;
input             d_write;
input             debugack;
input             reset_n;

wire     [ 24: 0] cpu_d_address;
wire              cpu_d_read;
wire     [ 31: 0] cpu_d_readdata;
wire              cpu_d_wait;
wire              cpu_d_write;
wire     [ 31: 0] cpu_d_writedata;
wire              dbrk0_armed;
wire              dbrk0_break_pulse;
wire              dbrk0_goto0;
wire              dbrk0_goto1;
wire              dbrk0_traceme;
wire              dbrk0_traceoff;
wire              dbrk0_traceon;
wire              dbrk0_trigout;
wire              dbrk1_armed;
wire              dbrk1_break_pulse;
wire              dbrk1_goto0;
wire              dbrk1_goto1;
wire              dbrk1_traceme;
wire              dbrk1_traceoff;
wire              dbrk1_traceon;
wire              dbrk1_trigout;
wire              dbrk2_armed;
wire              dbrk2_break_pulse;
wire              dbrk2_goto0;
wire              dbrk2_goto1;
wire              dbrk2_traceme;
wire              dbrk2_traceoff;
wire              dbrk2_traceon;
wire              dbrk2_trigout;
wire              dbrk3_armed;
wire              dbrk3_break_pulse;
wire              dbrk3_goto0;
wire              dbrk3_goto1;
wire              dbrk3_traceme;
wire              dbrk3_traceoff;
wire              dbrk3_traceon;
```

```
wire                    dbrk3_trigout;
reg                     dbrk_break;
reg                     dbrk_break_pulse;
wire       [ 31: 0] dbrk_data;
reg                     dbrk_goto0;
reg                     dbrk_goto1;
reg                     dbrk_traceme;
reg                     dbrk_traceoff;
reg                     dbrk_traceon;
reg                     dbrk_trigout;
assign cpu_d_address = d_address;
assign cpu_d_readdata = av_ld_data_aligned_filtered;
assign cpu_d_read = d_read;
assign cpu_d_writedata = E_st_data;
assign cpu_d_write = d_write;
assign cpu_d_wait = d_waitrequest;
assign dbrk_data = cpu_d_write ? cpu_d_writedata : cpu_d_readdata;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
           dbrk_break <= 0;
      else
         dbrk_break <= dbrk_break      ? ~debugack
                     : dbrk_break_pulse;

   end


assign dbrk0_armed = 1'b0;
assign dbrk0_trigout = 1'b0;
assign dbrk0_break_pulse = 1'b0;
assign dbrk0_traceoff = 1'b0;
assign dbrk0_traceon = 1'b0;
assign dbrk0_traceme = 1'b0;
assign dbrk0_goto0 = 1'b0;
assign dbrk0_goto1 = 1'b0;
assign dbrk1_armed = 1'b0;
assign dbrk1_trigout = 1'b0;
assign dbrk1_break_pulse = 1'b0;
assign dbrk1_traceoff = 1'b0;
assign dbrk1_traceon = 1'b0;
assign dbrk1_traceme = 1'b0;
assign dbrk1_goto0 = 1'b0;
assign dbrk1_goto1 = 1'b0;
assign dbrk2_armed = 1'b0;
assign dbrk2_trigout = 1'b0;
assign dbrk2_break_pulse = 1'b0;
assign dbrk2_traceoff = 1'b0;
assign dbrk2_traceon = 1'b0;
assign dbrk2_traceme = 1'b0;
assign dbrk2_goto0 = 1'b0;
assign dbrk2_goto1 = 1'b0;
assign dbrk3_armed = 1'b0;
assign dbrk3_trigout = 1'b0;
assign dbrk3_break_pulse = 1'b0;
assign dbrk3_traceoff = 1'b0;
assign dbrk3_traceon = 1'b0;
assign dbrk3_traceme = 1'b0;
```

```
  assign dbrk3_goto0 = 1'b0;
  assign dbrk3_goto1 = 1'b0;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
        begin
          dbrk_trigout <= 0;
          dbrk_break_pulse <= 0;
          dbrk_traceoff <= 0;
          dbrk_traceon <= 0;
          dbrk_traceme <= 0;
          dbrk_goto0 <= 0;
          dbrk_goto1 <= 0;
        end
      else
        begin
          dbrk_trigout <= dbrk0_trigout | dbrk1_trigout | dbrk2_trigout | dbrk3_trigout;
          dbrk_break_pulse <= dbrk0_break_pulse | dbrk1_break_pulse | dbrk2_break_pulse
| dbrk3_break_pulse;
          dbrk_traceoff <= dbrk0_traceoff | dbrk1_traceoff | dbrk2_traceoff | dbrk3_traceoff;
          dbrk_traceon <= dbrk0_traceon | dbrk1_traceon | dbrk2_traceon | dbrk3_traceon;
          dbrk_traceme <= dbrk0_traceme | dbrk1_traceme | dbrk2_traceme |
dbrk3_traceme;
          dbrk_goto0 <= dbrk0_goto0 | dbrk1_goto0 | dbrk2_goto0 | dbrk3_goto0;
          dbrk_goto1 <= dbrk0_goto1 | dbrk1_goto1 | dbrk2_goto1 | dbrk3_goto1;
        end
    end



endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci_itrace (
                                        // inputs:
                                          clk,
                                          dbrk_traceoff,
                                          dbrk_traceon,
                                          jdo,
                                          jrst_n,
                                          take_action_tracectrl,
                                          trc_enb,
                                          xbrk_traceoff,
                                          xbrk_traceon,
                                          xbrk_wrap_traceoff,

                                        // outputs:
                                          dct_buffer,
                                          dct_count,
                                          itm,
```

```
                                        trc_ctrl,
                                        trc_on
                                    )
;

   output   [ 29: 0] dct_buffer;
   output   [  3: 0] dct_count;
   output   [ 35: 0] itm;
   output   [ 15: 0] trc_ctrl;
   output            trc_on;
   input             clk;
   input             dbrk_traceoff;
   input             dbrk_traceon;
   input    [ 15: 0] jdo;
   input             jrst_n;
   input             take_action_tracectrl;
   input             trc_enb;
   input             xbrk_traceoff;
   input             xbrk_traceon;
   input             xbrk_wrap_traceoff;

   wire              curr_pid;
   reg               [ 29: 0] dct_buffer /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   wire     [  1: 0] dct_code;
   reg               [  3: 0] dct_count /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   wire              dct_is_taken;
   wire     [ 31: 0] excaddr;
   wire              instr_retired;
   wire              is_advanced_exception;
   wire              is_cond_dct;
   wire              is_dct;
   wire              is_exception_no_break;
   wire              is_fast_tlb_miss_exception;
   wire              is_idct;
   reg               [ 35: 0] itm /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   wire              not_in_debug_mode;
   reg               pending_curr_pid /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   reg               [ 31: 0] pending_excaddr /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   reg               pending_exctype /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   reg               [  3: 0] pending_frametype /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   reg               pending_prev_pid /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   reg               prev_pid /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   reg               prev_pid_valid /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   wire              record_dct_outcome_in_sync;
   wire              record_itrace;
   wire     [ 31: 0] retired_pcb;
   reg               snapped_curr_pid /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
```

```
  reg                                   snapped_pid  /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101"  */;
  reg                                snapped_prev_pid  /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101"  */;
  wire      [  1: 0] sync_code;
  wire      [  6: 0] sync_interval;
  wire               sync_pending;
  reg               [      6:   0]  sync_timer  /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101"  */;
  wire      [  6: 0] sync_timer_next;
  reg                                  trc_clear  /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=D101"  */;
  wire      [ 15: 0] trc_ctrl;
  reg               [   10:   0]  trc_ctrl_reg  /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,D103,R101\""  */;
  wire               trc_on;
  assign is_cond_dct = 1'b0;
  assign is_dct = 1'b0;
  assign dct_is_taken = 1'b0;
  assign is_idct = 1'b0;
  assign retired_pcb = 32'b0;
  assign not_in_debug_mode = 1'b0;
  assign instr_retired = 1'b0;
  assign is_advanced_exception = 1'b0;
  assign is_exception_no_break = 1'b0;
  assign is_fast_tlb_miss_exception = 1'b0;
  assign curr_pid = 1'b0;
  assign excaddr = 32'b0;
  assign sync_code = trc_ctrl[3 : 2];
  assign sync_interval = { sync_code[1] & sync_code[0], 1'b0, sync_code[1] & ~sync_code[0],
1'b0, ~sync_code[1] & sync_code[0], 2'b00 };
  assign sync_pending = sync_timer == 0;
  assign record_dct_outcome_in_sync = dct_is_taken & sync_pending;
  assign sync_timer_next = sync_pending ? sync_timer : (sync_timer - 1);
  assign record_itrace = trc_on & trc_ctrl[4];
  assign dct_code = {is_cond_dct, dct_is_taken};
  always @(posedge clk or negedge jrst_n)
    begin
      if (jrst_n == 0)
          trc_clear <= 0;
      else
        trc_clear <= ~trc_enb &
                  take_action_tracectrl & jdo[4];

    end


  always @(posedge clk or negedge jrst_n)
    begin
      if (jrst_n == 0)
        begin
          itm <= 0;
          dct_buffer <= 0;
          dct_count <= 0;
          sync_timer <= 0;
          pending_frametype <= 4'b0000;
          pending_exctype <= 1'b0;
          pending_excaddr <= 0;
```

```
        prev_pid <= 0;
        prev_pid_valid <= 0;
        snapped_pid <= 0;
        snapped_curr_pid <= 0;
        snapped_prev_pid <= 0;
        pending_curr_pid <= 0;
        pending_prev_pid <= 0;
    end
else if (trc_clear || (!0 && !0))
    begin
        itm <= 0;
        dct_buffer <= 0;
        dct_count <= 0;
        sync_timer <= 0;
        pending_frametype <= 4'b0000;
        pending_exctype <= 1'b0;
        pending_excaddr <= 0;
        prev_pid <= 0;
        prev_pid_valid <= 0;
        snapped_pid <= 0;
        snapped_curr_pid <= 0;
        snapped_prev_pid <= 0;
        pending_curr_pid <= 0;
        pending_prev_pid <= 0;
    end
else
    begin
        if (!prev_pid_valid)
            begin
                prev_pid <= curr_pid;
                prev_pid_valid <= 1;
            end
        if ((curr_pid != prev_pid) & prev_pid_valid & !snapped_pid)
            begin
                snapped_pid <= 1;
                snapped_curr_pid <= curr_pid;
                snapped_prev_pid <= prev_pid;
                prev_pid <= curr_pid;
                prev_pid_valid <= 1;
            end
        if (instr_retired | is_advanced_exception)
            begin
                if (~record_itrace)
                        pending_frametype <= 4'b1010;
                else if (is_exception_no_break)
                    begin
                        pending_frametype <= 4'b0010;
                        pending_excaddr <= excaddr;
                        if (is_fast_tlb_miss_exception)
                                pending_exctype <= 1'b1;
                        else
                            pending_exctype <= 1'b0;
                    end
                else if (is_idct)
                        pending_frametype <= 4'b1001;
                else if (record_dct_outcome_in_sync)
                        pending_frametype <= 4'b1000;
                else if (!is_dct & snapped_pid)
```

```
                    begin
                        pending_frametype <= 4'b0011;
                        pending_curr_pid <= snapped_curr_pid;
                        pending_prev_pid <= snapped_prev_pid;
                        snapped_pid <= 0;
                    end
                else
                    pending_frametype <= 4'b0000;
                if ((dct_count != 0) &
            (~record_itrace |
             is_exception_no_break |
             is_idct |
             record_dct_outcome_in_sync |
             (!is_dct & snapped_pid)))
                    begin
                        itm <= {4'b0001, dct_buffer, 2'b00};
                        dct_buffer <= 0;
                        dct_count <= 0;
                        sync_timer <= sync_timer_next;
                    end
                else
                    begin
                        if (record_itrace & (is_dct & (dct_count != 4'd15)) &
~record_dct_outcome_in_sync & ~is_advanced_exception)
                            begin
                                dct_buffer <= {dct_code, dct_buffer[29 : 2]};
                                dct_count <= dct_count + 1;
                            end
                        if (record_itrace & (pending_frametype == 4'b0010))
                                itm <= {4'b0010, pending_excaddr[31 : 1], pending_exctype};
                        else if (record_itrace & (
                    (pending_frametype == 4'b1000) |
                    (pending_frametype == 4'b1010) |
                    (pending_frametype == 4'b1001)))
                            begin
                                itm <= {pending_frametype, retired_pcb};
                                sync_timer <= sync_interval;
                                if (0 &
                            ((pending_frametype == 4'b1000) | (pending_frametype == 4'b1010)) &
                            !snapped_pid & prev_pid_valid)
                                    begin
                                        snapped_pid <= 1;
                                        snapped_curr_pid <= curr_pid;
                                        snapped_prev_pid <= prev_pid;
                                    end
                            end
                        else if (record_itrace &
                    0 & (pending_frametype == 4'b0011))
                                itm <= {4'b0011, 2'b00, pending_prev_pid, 2'b00, pending_curr_pid};
                        else if (record_itrace & is_dct)
                            begin
                                if (dct_count == 4'd15)
                                    begin
                                        itm <= {4'b0001, dct_code, dct_buffer};
                                        dct_buffer <= 0;
                                        dct_count <= 0;
                                        sync_timer <= sync_timer_next;
                                    end
```

```
                        else
                            itm <= 4'b0000;
                        end
                    else
                        itm <= {4'b0000, 32'b0};
                end
            end
        else
            itm <= {4'b0000, 32'b0};
        end
    end


  always @(posedge clk or negedge jrst_n)
    begin
      if (jrst_n == 0)
        begin
          trc_ctrl_reg[0] <= 1'b0;
          trc_ctrl_reg[1] <= 1'b0;
          trc_ctrl_reg[3 : 2] <= 2'b00;
          trc_ctrl_reg[4] <= 1'b0;
          trc_ctrl_reg[7 : 5] <= 3'b000;
          trc_ctrl_reg[8] <= 0;
          trc_ctrl_reg[9] <= 1'b0;
          trc_ctrl_reg[10] <= 1'b0;
        end
      else if (take_action_tracectrl)
        begin
          trc_ctrl_reg[0] <= jdo[5];
          trc_ctrl_reg[1] <= jdo[6];
          trc_ctrl_reg[3 : 2] <= jdo[8 : 7];
          trc_ctrl_reg[4] <= jdo[9];
          trc_ctrl_reg[9] <= jdo[14];
          trc_ctrl_reg[10] <= jdo[2];
          if (0)
              trc_ctrl_reg[7 : 5] <= jdo[12 : 10];
          if (0 & 0)
              trc_ctrl_reg[8] <= jdo[13];
        end
      else if (xbrk_wrap_traceoff)
        begin
          trc_ctrl_reg[1] <= 0;
          trc_ctrl_reg[0] <= 0;
        end
      else if (dbrk_traceoff | xbrk_traceoff)
          trc_ctrl_reg[1] <= 0;
      else if (trc_ctrl_reg[0] &
                                          (dbrk_traceon | xbrk_traceon))
          trc_ctrl_reg[1] <= 1;
    end


  assign trc_ctrl = (0 || 0) ? {6'b000000, trc_ctrl_reg} : 0;
  assign trc_on = trc_ctrl[1] & (trc_ctrl[9] | not_in_debug_mode);

endmodule
```

```
// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci_td_mode (
                                                // inputs:
                                                  ctrl,

                                                // outputs:
                                                  td_mode
                                               )
;

   output    [    3: 0] td_mode;
   input     [    8: 0] ctrl;

   wire      [    2: 0] ctrl_bits_for_mux;
   reg       [    3: 0] td_mode;
   assign ctrl_bits_for_mux = ctrl[7 : 5];
   always @(ctrl_bits_for_mux)
      begin
         case (ctrl_bits_for_mux)

               3'b000: begin
                     td_mode = 4'b0000;
               end // 3'b000

               3'b001: begin
                     td_mode = 4'b1000;
               end // 3'b001

               3'b010: begin
                     td_mode = 4'b0100;
               end // 3'b010

               3'b011: begin
                     td_mode = 4'b1100;
               end // 3'b011

               3'b100: begin
                     td_mode = 4'b0010;
               end // 3'b100

               3'b101: begin
                     td_mode = 4'b1010;
               end // 3'b101

               3'b110: begin
                     td_mode = 4'b0101;
               end // 3'b110

               3'b111: begin
                     td_mode = 4'b1111;
               end // 3'b111
```

```
          endcase // ctrl_bits_for_mux
        end



endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci_dtrace (
                                                // inputs:
                                                  clk,
                                                  cpu_d_address,
                                                  cpu_d_read,
                                                  cpu_d_readdata,
                                                  cpu_d_wait,
                                                  cpu_d_write,
                                                  cpu_d_writedata,
                                                  jrst_n,
                                                  trc_ctrl,

                                                // outputs:
                                                  atm,
                                                  dtm
                                               )
;

   output    [ 35: 0] atm;
   output    [ 35: 0] dtm;
   input              clk;
   input     [ 24: 0] cpu_d_address;
   input              cpu_d_read;
   input     [ 31: 0] cpu_d_readdata;
   input              cpu_d_wait;
   input              cpu_d_write;
   input     [ 31: 0] cpu_d_writedata;
   input              jrst_n;
   input     [ 15: 0] trc_ctrl;

   reg                [ 35: 0] atm /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   wire      [ 31: 0] cpu_d_address_0_padded;
   wire      [ 31: 0] cpu_d_readdata_0_padded;
   wire      [ 31: 0] cpu_d_writedata_0_padded;
   reg                [ 35: 0] dtm /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   wire               record_load_addr;
   wire               record_load_data;
   wire               record_store_addr;
   wire               record_store_data;
```

```
  wire       [  3: 0] td_mode_trc_ctrl;
  assign cpu_d_writedata_0_padded = cpu_d_writedata | 32'b0;
  assign cpu_d_readdata_0_padded = cpu_d_readdata | 32'b0;
  assign cpu_d_address_0_padded = cpu_d_address | 32'b0;
  //cpu_0_nios2_oci_trc_ctrl_td_mode, which is an e_instance
  cpu_0_nios2_oci_td_mode cpu_0_nios2_oci_trc_ctrl_td_mode
    (
      .ctrl       (trc_ctrl[8 : 0]),
      .td_mode (td_mode_trc_ctrl)
    );

  assign {record_load_addr, record_store_addr,
            record_load_data, record_store_data} = td_mode_trc_ctrl;
  always @(posedge clk or negedge jrst_n)
    begin
      if (jrst_n == 0)
        begin
          atm <= 0;
          dtm <= 0;
        end
      else if (0)
        begin
          if (cpu_d_write & ~cpu_d_wait & record_store_addr)
                atm <= {4'b0101, cpu_d_address_0_padded};
          else if (cpu_d_read & ~cpu_d_wait & record_load_addr)
                atm <= {4'b0100, cpu_d_address_0_padded};
          else
             atm <= {4'b0000, cpu_d_address_0_padded};
          if (cpu_d_write & ~cpu_d_wait & record_store_data)
                dtm <= {4'b0111, cpu_d_writedata_0_padded};
          else if (cpu_d_read & ~cpu_d_wait & record_load_data)
                dtm <= {4'b0110, cpu_d_readdata_0_padded};
          else
             dtm <= {4'b0000, cpu_d_readdata_0_padded};
        end
      else
        begin
          atm <= 0;
          dtm <= 0;
        end
    end



endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci_compute_tm_count (
                                                        // inputs:
                                                          atm_valid,
```

```
                                                    dtm_valid,
                                                    itm_valid,

                                                  // outputs:
                                                    compute_tm_count
                                                )
;

   output    [    1: 0] compute_tm_count;
   input                atm_valid;
   input                dtm_valid;
   input                itm_valid;

   reg       [    1: 0] compute_tm_count;
   wire      [    2: 0] switch_for_mux;
   assign switch_for_mux = {itm_valid, atm_valid, dtm_valid};
   always @(switch_for_mux)
     begin
       case (switch_for_mux)

            3'b000: begin
                compute_tm_count = 0;
            end // 3'b000

            3'b001: begin
                compute_tm_count = 1;
            end // 3'b001

            3'b010: begin
                compute_tm_count = 1;
            end // 3'b010

            3'b011: begin
                compute_tm_count = 2;
            end // 3'b011

            3'b100: begin
                compute_tm_count = 1;
            end // 3'b100

            3'b101: begin
                compute_tm_count = 2;
            end // 3'b101

            3'b110: begin
                compute_tm_count = 2;
            end // 3'b110

            3'b111: begin
                compute_tm_count = 3;
            end // 3'b111

       endcase // switch_for_mux
     end


endmodule
```

```
// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci_fifowp_inc (
                                    // inputs:
                                      free2,
                                      free3,
                                      tm_count,

                                    // outputs:
                                      fifowp_inc
                                   )
;

   output    [  3: 0] fifowp_inc;
   input              free2;
   input              free3;
   input     [  1: 0] tm_count;

   reg       [  3: 0] fifowp_inc;
   always @(free2 or free3 or tm_count)
      begin
         if (free3 & (tm_count == 3))
               fifowp_inc = 3;
         else if (free2 & (tm_count >= 2))
               fifowp_inc = 2;
         else if (tm_count >= 1)
               fifowp_inc = 1;
         else
            fifowp_inc = 0;
      end



endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci_fifocount_inc (
                                       // inputs:
                                         empty,
                                         free2,
                                         free3,
                                         tm_count,
```

```
                                                    // outputs:
                                                      fifocount_inc
                                                   )
;

   output    [    4: 0] fifocount_inc;
   input                empty;
   input                free2;
   input                free3;
   input     [    1: 0] tm_count;

   reg       [    4: 0] fifocount_inc;
   always @(empty or free2 or free3 or tm_count)
      begin
         if (empty)
               fifocount_inc = tm_count[1 : 0];
         else if (free3 & (tm_count == 3))
               fifocount_inc = 2;
         else if (free2 & (tm_count >= 2))
               fifocount_inc = 1;
         else if (tm_count >= 1)
               fifocount_inc = 0;
         else
            fifocount_inc = {5{1'b1}};
      end



endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci_fifo (
                                                  // inputs:
                                                    atm,
                                                    clk,
                                                    dbrk_traceme,
                                                    dbrk_traceoff,
                                                    dbrk_traceon,
                                                    dct_buffer,
                                                    dct_count,
                                                    dtm,
                                                    itm,
                                                    jrst_n,
                                                    reset_n,
                                                    test_ending,
                                                    test_has_ended,
                                                    trc_on,

                                                  // outputs:
```

```
                                        tw
                                    )
;

   output   [ 35: 0] tw;
   input    [ 35: 0] atm;
   input             clk;
   input             dbrk_traceme;
   input             dbrk_traceoff;
   input             dbrk_traceon;
   input    [ 29: 0] dct_buffer;
   input    [    3: 0] dct_count;
   input    [ 35: 0] dtm;
   input    [ 35: 0] itm;
   input             jrst_n;
   input             reset_n;
   input             test_ending;
   input             test_has_ended;
   input             trc_on;

   wire              atm_valid;
   wire     [    1: 0] compute_tm_count_tm_count;
   wire              dtm_valid;
   wire              empty;
   reg      [ 35: 0] fifo_0;
   wire              fifo_0_enable;
   wire     [ 35: 0] fifo_0_mux;
   reg      [ 35: 0] fifo_1;
   reg      [ 35: 0] fifo_10;
   wire              fifo_10_enable;
   wire     [ 35: 0] fifo_10_mux;
   reg      [ 35: 0] fifo_11;
   wire              fifo_11_enable;
   wire     [ 35: 0] fifo_11_mux;
   reg      [ 35: 0] fifo_12;
   wire              fifo_12_enable;
   wire     [ 35: 0] fifo_12_mux;
   reg      [ 35: 0] fifo_13;
   wire              fifo_13_enable;
   wire     [ 35: 0] fifo_13_mux;
   reg      [ 35: 0] fifo_14;
   wire              fifo_14_enable;
   wire     [ 35: 0] fifo_14_mux;
   reg      [ 35: 0] fifo_15;
   wire              fifo_15_enable;
   wire     [ 35: 0] fifo_15_mux;
   wire              fifo_1_enable;
   wire     [ 35: 0] fifo_1_mux;
   reg      [ 35: 0] fifo_2;
   wire              fifo_2_enable;
   wire     [ 35: 0] fifo_2_mux;
   reg      [ 35: 0] fifo_3;
   wire              fifo_3_enable;
   wire     [ 35: 0] fifo_3_mux;
   reg      [ 35: 0] fifo_4;
   wire              fifo_4_enable;
   wire     [ 35: 0] fifo_4_mux;
   reg      [ 35: 0] fifo_5;
```

```
  wire              fifo_5_enable;
  wire    [ 35: 0] fifo_5_mux;
  reg     [ 35: 0] fifo_6;
  wire              fifo_6_enable;
  wire    [ 35: 0] fifo_6_mux;
  reg     [ 35: 0] fifo_7;
  wire              fifo_7_enable;
  wire    [ 35: 0] fifo_7_mux;
  reg     [ 35: 0] fifo_8;
  wire              fifo_8_enable;
  wire    [ 35: 0] fifo_8_mux;
  reg     [ 35: 0] fifo_9;
  wire              fifo_9_enable;
  wire    [ 35: 0] fifo_9_mux;
  wire    [ 35: 0] fifo_read_mux;
  reg               [    4:    0]    fifocount    /*    synthesis    ALTERA_ATTRIBUTE    =
"SUPPRESS_DA_RULE_INTERNAL=R101"  */;
  wire    [  4: 0] fifocount_inc_fifocount;
  wire    [ 35: 0] fifohead;
  reg               [    3:    0]    fiforp    /*    synthesis    ALTERA_ATTRIBUTE    =
"SUPPRESS_DA_RULE_INTERNAL=R101"  */;
  reg               [    3:    0]    fifowp    /*    synthesis    ALTERA_ATTRIBUTE    =
"SUPPRESS_DA_RULE_INTERNAL=R101"  */;
  wire    [  3: 0] fifowp1;
  wire    [  3: 0] fifowp2;
  wire    [  3: 0] fifowp_inc_fifowp;
  wire              free2;
  wire              free3;
  wire              itm_valid;
  reg                                 ovf_pending    /*    synthesis    ALTERA_ATTRIBUTE    =
"SUPPRESS_DA_RULE_INTERNAL=R101"  */;
  wire    [ 35: 0] ovr_pending_atm;
  wire    [ 35: 0] ovr_pending_dtm;
  wire    [  1: 0] tm_count;
  wire              tm_count_ge1;
  wire              tm_count_ge2;
  wire              tm_count_ge3;
  wire              trc_this;
  wire    [ 35: 0] tw;
  assign trc_this = trc_on | (dbrk_traceon & ~dbrk_traceoff) | dbrk_traceme;
  assign itm_valid = |itm[35 : 32];
  assign atm_valid = |atm[35 : 32] & trc_this;
  assign dtm_valid = |dtm[35 : 32] & trc_this;
  assign free2 = ~fifocount[4];
  assign free3 = ~fifocount[4] & ~&fifocount[3 : 0];
  assign empty = ~|fifocount;
  assign fifowp1 = fifowp + 1;
  assign fifowp2 = fifowp + 2;
  //cpu_0_nios2_oci_compute_tm_count_tm_count, which is an e_instance
  cpu_0_nios2_oci_compute_tm_count cpu_0_nios2_oci_compute_tm_count_tm_count
    (
      .atm_valid              (atm_valid),
      .compute_tm_count (compute_tm_count_tm_count),
      .dtm_valid              (dtm_valid),
      .itm_valid             (itm_valid)
    );

  assign tm_count = compute_tm_count_tm_count;
```

```
  //cpu_0_nios2_oci_fifowp_inc_fifowp, which is an e_instance
  cpu_0_nios2_oci_fifowp_inc cpu_0_nios2_oci_fifowp_inc_fifowp
    (
      .fifowp_inc (fifowp_inc_fifowp),
      .free2      (free2),
      .free3      (free3),
      .tm_count    (tm_count)
    );

  //cpu_0_nios2_oci_fifocount_inc_fifocount, which is an e_instance
  cpu_0_nios2_oci_fifocount_inc cpu_0_nios2_oci_fifocount_inc_fifocount
    (
      .empty              (empty),
      .fifocount_inc (fifocount_inc_fifocount),
      .free2              (free2),
      .free3              (free3),
      .tm_count          (tm_count)
    );

  //the_cpu_0_oci_test_bench, which is an e_instance
  cpu_0_oci_test_bench the_cpu_0_oci_test_bench
    (
      .dct_buffer         (dct_buffer),
      .dct_count          (dct_count),
      .test_ending        (test_ending),
      .test_has_ended (test_has_ended)
    );

  always @(posedge clk or negedge jrst_n)
    begin
      if (jrst_n == 0)
        begin
          fiforp <= 0;
          fifowp <= 0;
          fifocount <= 0;
          ovf_pending <= 1;
        end
      else
        begin
          fifowp <= fifowp + fifowp_inc_fifowp;
          fifocount <= fifocount + fifocount_inc_fifocount;
          if (~empty)
              fiforp <= fiforp + 1;
          if (~trc_this || (~free2 & tm_count[1])      || (~free3 & (&tm_count)))
              ovf_pending <= 1;
          else if (atm_valid | dtm_valid)
              ovf_pending <= 0;
        end
    end


  assign fifohead = fifo_read_mux;
  assign tw = 0 ?   { (empty ?          4'h0          : fifohead[35 : 32]),     fifohead[31 : 0]}   :
itm;
  assign fifo_0_enable = ((fifowp == 4'd0) && tm_count_ge1)   || (free2 && (fifowp1== 4'd0)
&& tm_count_ge2)   ||(free3 && (fifowp2== 4'd0) && tm_count_ge3);
  always @(posedge clk or negedge reset_n)
    begin
```

```
      if (reset_n == 0)
            fifo_0 <= 0;
      else if (fifo_0_enable)
            fifo_0 <= fifo_0_mux;
   end


assign fifo_0_mux = (((fifowp == 4'd0) && itm_valid))? itm :
   (((fifowp == 4'd0) && atm_valid))? ovr_pending_atm :
   (((fifowp == 4'd0) && dtm_valid))? ovr_pending_dtm :
   (((fifowp1 == 4'd0) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
   (((fifowp1 == 4'd0) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
   (((fifowp1 == 4'd0) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
   ovr_pending_dtm;

assign fifo_1_enable = ((fifowp == 4'd1) && tm_count_ge1)   || (free2 && (fifowp1== 4'd1)
&& tm_count_ge2)   ||(free3 && (fifowp2== 4'd1) && tm_count_ge3);
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            fifo_1 <= 0;
      else if (fifo_1_enable)
            fifo_1 <= fifo_1_mux;
   end


assign fifo_1_mux = (((fifowp == 4'd1) && itm_valid))? itm :
   (((fifowp == 4'd1) && atm_valid))? ovr_pending_atm :
   (((fifowp == 4'd1) && dtm_valid))? ovr_pending_dtm :
   (((fifowp1 == 4'd1) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
   (((fifowp1 == 4'd1) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
   (((fifowp1 == 4'd1) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
   ovr_pending_dtm;

assign fifo_2_enable = ((fifowp == 4'd2) && tm_count_ge1)   || (free2 && (fifowp1== 4'd2)
&& tm_count_ge2)   ||(free3 && (fifowp2== 4'd2) && tm_count_ge3);
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            fifo_2 <= 0;
      else if (fifo_2_enable)
            fifo_2 <= fifo_2_mux;
   end


assign fifo_2_mux = (((fifowp == 4'd2) && itm_valid))? itm :
   (((fifowp == 4'd2) && atm_valid))? ovr_pending_atm :
   (((fifowp == 4'd2) && dtm_valid))? ovr_pending_dtm :
   (((fifowp1 == 4'd2) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
   (((fifowp1 == 4'd2) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
   (((fifowp1 == 4'd2) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
   ovr_pending_dtm;

assign fifo_3_enable = ((fifowp == 4'd3) && tm_count_ge1)   || (free2 && (fifowp1== 4'd3)
&& tm_count_ge2)   ||(free3 && (fifowp2== 4'd3) && tm_count_ge3);
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
```

```
            fifo_3 <= 0;
        else if (fifo_3_enable)
            fifo_3 <= fifo_3_mux;
    end


  assign fifo_3_mux = (((fifowp == 4'd3) && itm_valid))? itm :
    (((fifowp == 4'd3) && atm_valid))? ovr_pending_atm :
    (((fifowp == 4'd3) && dtm_valid))? ovr_pending_dtm :
    (((fifowp1 == 4'd3) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
    (((fifowp1 == 4'd3) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
    (((fifowp1 == 4'd3) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
    ovr_pending_dtm;

  assign fifo_4_enable = ((fifowp == 4'd4) && tm_count_ge1)   || (free2 && (fifowp1== 4'd4)
&& tm_count_ge2)   ||(free3 && (fifowp2== 4'd4) && tm_count_ge3);
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            fifo_4 <= 0;
      else if (fifo_4_enable)
            fifo_4 <= fifo_4_mux;
    end


  assign fifo_4_mux = (((fifowp == 4'd4) && itm_valid))? itm :
    (((fifowp == 4'd4) && atm_valid))? ovr_pending_atm :
    (((fifowp == 4'd4) && dtm_valid))? ovr_pending_dtm :
    (((fifowp1 == 4'd4) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
    (((fifowp1 == 4'd4) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
    (((fifowp1 == 4'd4) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
    ovr_pending_dtm;

  assign fifo_5_enable = ((fifowp == 4'd5) && tm_count_ge1)   || (free2 && (fifowp1== 4'd5)
&& tm_count_ge2)   ||(free3 && (fifowp2== 4'd5) && tm_count_ge3);
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            fifo_5 <= 0;
      else if (fifo_5_enable)
            fifo_5 <= fifo_5_mux;
    end


  assign fifo_5_mux = (((fifowp == 4'd5) && itm_valid))? itm :
    (((fifowp == 4'd5) && atm_valid))? ovr_pending_atm :
    (((fifowp == 4'd5) && dtm_valid))? ovr_pending_dtm :
    (((fifowp1 == 4'd5) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
    (((fifowp1 == 4'd5) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
    (((fifowp1 == 4'd5) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
    ovr_pending_dtm;

  assign fifo_6_enable = ((fifowp == 4'd6) && tm_count_ge1)   || (free2 && (fifowp1== 4'd6)
&& tm_count_ge2)   ||(free3 && (fifowp2== 4'd6) && tm_count_ge3);
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            fifo_6 <= 0;
```

```
        else if (fifo_6_enable)
              fifo_6 <= fifo_6_mux;
     end


  assign fifo_6_mux = (((fifowp == 4'd6) && itm_valid))? itm :
     (((fifowp == 4'd6) && atm_valid))? ovr_pending_atm :
     (((fifowp == 4'd6) && dtm_valid))? ovr_pending_dtm :
     (((fifowp1 == 4'd6) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
     (((fifowp1 == 4'd6) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
     (((fifowp1 == 4'd6) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
     ovr_pending_dtm;

  assign fifo_7_enable = ((fifowp == 4'd7) && tm_count_ge1)   || (free2 && (fifowp1== 4'd7)
&& tm_count_ge2)   ||(free3 && (fifowp2== 4'd7) && tm_count_ge3);
  always @(posedge clk or negedge reset_n)
     begin
        if (reset_n == 0)
              fifo_7 <= 0;
        else if (fifo_7_enable)
              fifo_7 <= fifo_7_mux;
     end


  assign fifo_7_mux = (((fifowp == 4'd7) && itm_valid))? itm :
     (((fifowp == 4'd7) && atm_valid))? ovr_pending_atm :
     (((fifowp == 4'd7) && dtm_valid))? ovr_pending_dtm :
     (((fifowp1 == 4'd7) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
     (((fifowp1 == 4'd7) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
     (((fifowp1 == 4'd7) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
     ovr_pending_dtm;

  assign fifo_8_enable = ((fifowp == 4'd8) && tm_count_ge1)   || (free2 && (fifowp1== 4'd8)
&& tm_count_ge2)   ||(free3 && (fifowp2== 4'd8) && tm_count_ge3);
  always @(posedge clk or negedge reset_n)
     begin
        if (reset_n == 0)
              fifo_8 <= 0;
        else if (fifo_8_enable)
              fifo_8 <= fifo_8_mux;
     end


  assign fifo_8_mux = (((fifowp == 4'd8) && itm_valid))? itm :
     (((fifowp == 4'd8) && atm_valid))? ovr_pending_atm :
     (((fifowp == 4'd8) && dtm_valid))? ovr_pending_dtm :
     (((fifowp1 == 4'd8) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
     (((fifowp1 == 4'd8) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
     (((fifowp1 == 4'd8) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
     ovr_pending_dtm;

  assign fifo_9_enable = ((fifowp == 4'd9) && tm_count_ge1)   || (free2 && (fifowp1== 4'd9)
&& tm_count_ge2)   ||(free3 && (fifowp2== 4'd9) && tm_count_ge3);
  always @(posedge clk or negedge reset_n)
     begin
        if (reset_n == 0)
              fifo_9 <= 0;
        else if (fifo_9_enable)
```

```
            fifo_9 <= fifo_9_mux;
      end


   assign fifo_9_mux = (((fifowp == 4'd9) && itm_valid))? itm :
      (((fifowp == 4'd9) && atm_valid))? ovr_pending_atm :
      (((fifowp == 4'd9) && dtm_valid))? ovr_pending_dtm :
      (((fifowp1 == 4'd9) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
      (((fifowp1 == 4'd9) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
      (((fifowp1 == 4'd9) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
      ovr_pending_dtm;

   assign fifo_10_enable = ((fifowp == 4'd10) && tm_count_ge1)    || (free2 && (fifowp1== 4'd10)
&& tm_count_ge2)    ||(free3 && (fifowp2== 4'd10) && tm_count_ge3);
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
            fifo_10 <= 0;
         else if (fifo_10_enable)
            fifo_10 <= fifo_10_mux;
      end


   assign fifo_10_mux = (((fifowp == 4'd10) && itm_valid))? itm :
      (((fifowp == 4'd10) && atm_valid))? ovr_pending_atm :
      (((fifowp == 4'd10) && dtm_valid))? ovr_pending_dtm :
      (((fifowp1 == 4'd10) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
      (((fifowp1 == 4'd10) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
      (((fifowp1 == 4'd10) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
      ovr_pending_dtm;

   assign fifo_11_enable = ((fifowp == 4'd11) && tm_count_ge1)    || (free2 && (fifowp1== 4'd11)
&& tm_count_ge2)    ||(free3 && (fifowp2== 4'd11) && tm_count_ge3);
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
            fifo_11 <= 0;
         else if (fifo_11_enable)
            fifo_11 <= fifo_11_mux;
      end


   assign fifo_11_mux = (((fifowp == 4'd11) && itm_valid))? itm :
      (((fifowp == 4'd11) && atm_valid))? ovr_pending_atm :
      (((fifowp == 4'd11) && dtm_valid))? ovr_pending_dtm :
      (((fifowp1 == 4'd11) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
      (((fifowp1 == 4'd11) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
      (((fifowp1 == 4'd11) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
      ovr_pending_dtm;

   assign fifo_12_enable = ((fifowp == 4'd12) && tm_count_ge1)    || (free2 && (fifowp1== 4'd12)
&& tm_count_ge2)    ||(free3 && (fifowp2== 4'd12) && tm_count_ge3);
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
            fifo_12 <= 0;
         else if (fifo_12_enable)
            fifo_12 <= fifo_12_mux;
```

```
    end


  assign fifo_12_mux = (((fifowp == 4'd12) && itm_valid))? itm :
    (((fifowp == 4'd12) && atm_valid))? ovr_pending_atm :
    (((fifowp == 4'd12) && dtm_valid))? ovr_pending_dtm :
    (((fifowp1 == 4'd12) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
    (((fifowp1 == 4'd12) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
    (((fifowp1 == 4'd12) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
    ovr_pending_dtm;

  assign fifo_13_enable = ((fifowp == 4'd13) && tm_count_ge1)    || (free2 && (fifowp1== 4'd13)
&& tm_count_ge2)    ||(free3 && (fifowp2== 4'd13) && tm_count_ge3);
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          fifo_13 <= 0;
      else if (fifo_13_enable)
          fifo_13 <= fifo_13_mux;
    end


  assign fifo_13_mux = (((fifowp == 4'd13) && itm_valid))? itm :
    (((fifowp == 4'd13) && atm_valid))? ovr_pending_atm :
    (((fifowp == 4'd13) && dtm_valid))? ovr_pending_dtm :
    (((fifowp1 == 4'd13) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
    (((fifowp1 == 4'd13) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
    (((fifowp1 == 4'd13) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
    ovr_pending_dtm;

  assign fifo_14_enable = ((fifowp == 4'd14) && tm_count_ge1)    || (free2 && (fifowp1== 4'd14)
&& tm_count_ge2)    ||(free3 && (fifowp2== 4'd14) && tm_count_ge3);
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          fifo_14 <= 0;
      else if (fifo_14_enable)
          fifo_14 <= fifo_14_mux;
    end


  assign fifo_14_mux = (((fifowp == 4'd14) && itm_valid))? itm :
    (((fifowp == 4'd14) && atm_valid))? ovr_pending_atm :
    (((fifowp == 4'd14) && dtm_valid))? ovr_pending_dtm :
    (((fifowp1 == 4'd14) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
    (((fifowp1 == 4'd14) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
    (((fifowp1 == 4'd14) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
    ovr_pending_dtm;

  assign fifo_15_enable = ((fifowp == 4'd15) && tm_count_ge1)    || (free2 && (fifowp1== 4'd15)
&& tm_count_ge2)    ||(free3 && (fifowp2== 4'd15) && tm_count_ge3);
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          fifo_15 <= 0;
      else if (fifo_15_enable)
          fifo_15 <= fifo_15_mux;
    end
```

```
    assign fifo_15_mux = (((fifowp == 4'd15) && itm_valid))? itm :
      (((fifowp == 4'd15) && atm_valid))? ovr_pending_atm :
      (((fifowp == 4'd15) && dtm_valid))? ovr_pending_dtm :
      (((fifowp1 == 4'd15) && (free2 & itm_valid & atm_valid)))? ovr_pending_atm :
      (((fifowp1 == 4'd15) && (free2 & itm_valid & dtm_valid)))? ovr_pending_dtm :
      (((fifowp1 == 4'd15) && (free2 & atm_valid & dtm_valid)))? ovr_pending_dtm :
      ovr_pending_dtm;

    assign tm_count_ge1 = |tm_count;
    assign tm_count_ge2 = tm_count[1];
    assign tm_count_ge3 = &tm_count;
    assign ovr_pending_atm = {ovf_pending, atm[34 : 0]};
    assign ovr_pending_dtm = {ovf_pending, dtm[34 : 0]};
    assign fifo_read_mux = (fiforp == 4'd0)? fifo_0 :
      (fiforp == 4'd1)? fifo_1 :
      (fiforp == 4'd2)? fifo_2 :
      (fiforp == 4'd3)? fifo_3 :
      (fiforp == 4'd4)? fifo_4 :
      (fiforp == 4'd5)? fifo_5 :
      (fiforp == 4'd6)? fifo_6 :
      (fiforp == 4'd7)? fifo_7 :
      (fiforp == 4'd8)? fifo_8 :
      (fiforp == 4'd9)? fifo_9 :
      (fiforp == 4'd10)? fifo_10 :
      (fiforp == 4'd11)? fifo_11 :
      (fiforp == 4'd12)? fifo_12 :
      (fiforp == 4'd13)? fifo_13 :
      (fiforp == 4'd14)? fifo_14 :
      fifo_15;


endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci_pib (
                             // inputs:
                               clk,
                               clkx2,
                               jrst_n,
                               tw,

                             // outputs:
                               tr_clk,
                               tr_data
                           )
;

    output              tr_clk;
```

```
   output    [ 17: 0] tr_data;
   input               clk;
   input               clkx2;
   input               jrst_n;
   input     [ 35: 0] tw;

   wire                phase;
   wire                tr_clk;
   reg                 tr_clk_reg /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   wire      [ 17: 0] tr_data;
   reg       [ 17: 0] tr_data_reg /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   reg                 x1 /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   reg                 x2 /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=R101" */;
   assign phase = x1^x2;
   always @(posedge clk or negedge jrst_n)
      begin
         if (jrst_n == 0)
               x1 <= 0;
         else
            x1 <= ~x1;
      end


   always @(posedge clkx2 or negedge jrst_n)
      begin
         if (jrst_n == 0)
            begin
               x2 <= 0;
               tr_clk_reg <= 0;
               tr_data_reg <= 0;
            end
         else
            begin
               x2 <= x1;
               tr_clk_reg <= ~phase;
               tr_data_reg <= phase ?     tw[17 : 0] :     tw[35 : 18];
            end
      end


   assign tr_clk = 0 ? tr_clk_reg : 0;
   assign tr_data = 0 ? tr_data_reg : 0;

endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030
```

```
module cpu_0_traceram_lpm_dram_bdp_component_module (
                                                      // inputs:
                                                        address_a,
                                                        address_b,
                                                        clock0,
                                                        clock1,
                                                        clocken0,
                                                        clocken1,
                                                        data_a,
                                                        data_b,
                                                        wren_a,
                                                        wren_b,

                                                      // outputs:
                                                        q_a,
                                                        q_b
                                                     )
;

  parameter lpm_file = "UNUSED";


  output    [ 35: 0] q_a;
  output    [ 35: 0] q_b;
  input     [    6: 0] address_a;
  input     [    6: 0] address_b;
  input               clock0;
  input               clock1;
  input               clocken0;
  input               clocken1;
  input     [ 35: 0] data_a;
  input     [ 35: 0] data_b;
  input               wren_a;
  input               wren_b;

  wire      [ 35: 0] q_a;
  wire      [ 35: 0] q_b;
  altsyncram the_altsyncram
    (
      .address_a (address_a),
      .address_b (address_b),
      .clock0 (clock0),
      .clock1 (clock1),
      .clocken0 (clocken0),
      .clocken1 (clocken1),
      .data_a (data_a),
      .data_b (data_b),
      .q_a (q_a),
      .q_b (q_b),
      .wren_a (wren_a),
      .wren_b (wren_b)
    );

  defparam the_altsyncram.address_aclr_a = "NONE",
           the_altsyncram.address_aclr_b = "NONE",
           the_altsyncram.address_reg_b = "CLOCK1",
           the_altsyncram.indata_aclr_a = "NONE",
           the_altsyncram.indata_aclr_b = "NONE",
```

```
                the_altsyncram.init_file = lpm_file,
                the_altsyncram.intended_device_family = "CYCLONEII",
                the_altsyncram.lpm_type = "altsyncram",
                the_altsyncram.numwords_a = 128,
                the_altsyncram.numwords_b = 128,
                the_altsyncram.operation_mode = "BIDIR_DUAL_PORT",
                the_altsyncram.outdata_aclr_a = "NONE",
                the_altsyncram.outdata_aclr_b = "NONE",
                the_altsyncram.outdata_reg_a = "UNREGISTERED",
                the_altsyncram.outdata_reg_b = "UNREGISTERED",
                the_altsyncram.ram_block_type = "AUTO",
                the_altsyncram.read_during_write_mode_mixed_ports = "OLD_DATA",
                the_altsyncram.width_a = 36,
                the_altsyncram.width_b = 36,
                the_altsyncram.widthad_a = 7,
                the_altsyncram.widthad_b = 7,
                the_altsyncram.wrcontrol_aclr_a = "NONE",
                the_altsyncram.wrcontrol_aclr_b = "NONE";


endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci_im (
                                        // inputs:
                                          clk,
                                          jdo,
                                          jrst_n,
                                          reset_n,
                                          take_action_tracectrl,
                                          take_action_tracemem_a,
                                          take_action_tracemem_b,
                                          take_no_action_tracemem_a,
                                          trc_ctrl,
                                          tw,

                                        // outputs:
                                          tracemem_on,
                                          tracemem_trcdata,
                                          tracemem_tw,
                                          trc_enb,
                                          trc_im_addr,
                                          trc_wrap,
                                          xbrk_wrap_traceoff
                                       )
;

  output           tracemem_on;
  output    [ 35: 0] tracemem_trcdata;
  output           tracemem_tw;
```

```
  output              trc_enb;
  output   [  6: 0] trc_im_addr;
  output              trc_wrap;
  output              xbrk_wrap_traceoff;
  input               clk;
  input    [ 37: 0] jdo;
  input               jrst_n;
  input               reset_n;
  input               take_action_tracectrl;
  input               take_action_tracemem_a;
  input               take_action_tracemem_b;
  input               take_no_action_tracemem_a;
  input    [ 15: 0] trc_ctrl;
  input    [ 35: 0] tw;

  wire                tracemem_on;
  wire     [ 35: 0] tracemem_trcdata;
  wire                tracemem_tw;
  wire                trc_enb;
  reg                 [  6:  0] trc_im_addr /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,D103,R101\"" */;
  wire     [ 35: 0] trc_im_data;
  reg                 [ 16:  0] trc_jtag_addr /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=D101" */;
  wire     [ 35: 0] trc_jtag_data;
  wire                trc_on_chip;
  reg                                   trc_wrap /* synthesis ALTERA_ATTRIBUTE =
"SUPPRESS_DA_RULE_INTERNAL=\"D101,D103,R101\"" */;
  wire                tw_valid;
  wire     [ 35: 0] unused_bdpram_port_q_a;
  wire                xbrk_wrap_traceoff;
  assign trc_im_data = tw;
  always @(posedge clk or negedge jrst_n)
    begin
      if (jrst_n == 0)
        begin
          trc_im_addr <= 0;
          trc_wrap <= 0;
        end
      else if (!0)
        begin
          trc_im_addr <= 0;
          trc_wrap <= 0;
        end
      else if (take_action_tracectrl &&
                          (jdo[4] | jdo[3]))
        begin
          if (jdo[4])
              trc_im_addr <= 0;
          if (jdo[3])
              trc_wrap <= 0;
        end
      else if (trc_enb & trc_on_chip & tw_valid)
        begin
          trc_im_addr <= trc_im_addr+1;
          if (&trc_im_addr)
              trc_wrap <= 1;
        end
```

```
      end


   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               trc_jtag_addr <= 0;
         else if (take_action_tracemem_a ||
                        take_no_action_tracemem_a ||
                        take_action_tracemem_b)
               trc_jtag_addr <= take_action_tracemem_a ?
                              jdo[35 : 19] :
                              trc_jtag_addr + 1;

      end


   assign trc_enb = trc_ctrl[0];
   assign trc_on_chip = ~trc_ctrl[8];
   assign tw_valid = |trc_im_data[35 : 32];
   assign xbrk_wrap_traceoff = trc_ctrl[10] & trc_wrap;
   assign tracemem_trcdata = (0) ?
      trc_jtag_data : 0;

   assign tracemem_tw = trc_wrap;
   assign tracemem_on = trc_enb;
//cpu_0_traceram_lpm_dram_bdp_component, which is an nios_tdp_ram
cpu_0_traceram_lpm_dram_bdp_component_module
cpu_0_traceram_lpm_dram_bdp_component
   (
      .address_a (trc_im_addr),
      .address_b (trc_jtag_addr),
      .clock0       (clk),
      .clock1       (clk),
      .clocken0    (1'b1),
      .clocken1    (1'b1),
      .data_a       (trc_im_data),
      .data_b       (jdo[36 : 1]),
      .q_a          (unused_bdpram_port_q_a),
      .q_b          (trc_jtag_data),
      .wren_a       (tw_valid & trc_enb),
      .wren_b       (take_action_tracemem_b)
   );


endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_performance_monitors
;
```

```
endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0_nios2_oci (
                                    // inputs:
                                      D_valid,
                                      E_st_data,
                                      E_valid,
                                      F_pc,
                                      address,
                                      av_ld_data_aligned_filtered,
                                      begintransfer,
                                      byteenable,
                                      chipselect,
                                      clk,
                                      d_address,
                                      d_read,
                                      d_waitrequest,
                                      d_write,
                                      debugaccess,
                                      hbreak_enabled,
                                      reset,
                                      reset_n,
                                      test_ending,
                                      test_has_ended,
                                      write,
                                      writedata,

                                    // outputs:
                                      jtag_debug_module_debugaccess_to_roms,
                                      oci_hbreak_req,
                                      oci_ienable,
                                      oci_single_step_mode,
                                      readdata,
                                      resetrequest
                                   )
;

  output           jtag_debug_module_debugaccess_to_roms;
  output           oci_hbreak_req;
  output   [ 31: 0] oci_ienable;
  output           oci_single_step_mode;
  output   [ 31: 0] readdata;
  output           resetrequest;
  input            D_valid;
  input    [ 31: 0] E_st_data;
  input            E_valid;
```

```
input     [ 22: 0] F_pc;
input     [  8: 0] address;
input     [ 31: 0] av_ld_data_aligned_filtered;
input              begintransfer;
input     [  3: 0] byteenable;
input              chipselect;
input              clk;
input     [ 24: 0] d_address;
input              d_read;
input              d_waitrequest;
input              d_write;
input              debugaccess;
input              hbreak_enabled;
input              reset;
input              reset_n;
input              test_ending;
input              test_has_ended;
input              write;
input     [ 31: 0] writedata;

wire      [ 31: 0] MonDReg;
wire      [ 35: 0] atm;
wire      [ 31: 0] break_readreg;
wire               clkx2;
wire      [ 24: 0] cpu_d_address;
wire               cpu_d_read;
wire      [ 31: 0] cpu_d_readdata;
wire               cpu_d_wait;
wire               cpu_d_write;
wire      [ 31: 0] cpu_d_writedata;
wire               dbrk_break;
wire               dbrk_goto0;
wire               dbrk_goto1;
wire               dbrk_hit0_latch;
wire               dbrk_hit1_latch;
wire               dbrk_hit2_latch;
wire               dbrk_hit3_latch;
wire               dbrk_traceme;
wire               dbrk_traceoff;
wire               dbrk_traceon;
wire               dbrk_trigout;
wire      [ 29: 0] dct_buffer;
wire      [  3: 0] dct_count;
wire               debugack;
wire               debugreq;
wire      [ 35: 0] dtm;
wire               dummy_sink;
wire      [ 35: 0] itm;
wire      [ 37: 0] jdo;
wire               jrst_n;
wire               jtag_debug_module_debugaccess_to_roms;
wire               monitor_error;
wire               monitor_go;
wire               monitor_ready;
wire               oci_hbreak_req;
wire      [ 31: 0] oci_ienable;
wire      [ 31: 0] oci_ram_readdata;
wire      [ 31: 0] oci_reg_readdata;
```

```
wire                    oci_single_step_mode;
wire                    ocireg_ers;
wire                    ocireg_mrs;
wire      [ 31: 0] readdata;
wire                    resetlatch;
wire                    resetrequest;
wire                    st_ready_test_idle;
wire                    take_action_break_a;
wire                    take_action_break_b;
wire                    take_action_break_c;
wire                    take_action_ocimem_a;
wire                    take_action_ocimem_b;
wire                    take_action_ocireg;
wire                    take_action_tracectrl;
wire                    take_action_tracemem_a;
wire                    take_action_tracemem_b;
wire                    take_no_action_break_a;
wire                    take_no_action_break_b;
wire                    take_no_action_break_c;
wire                    take_no_action_ocimem_a;
wire                    take_no_action_tracemem_a;
wire                    tr_clk;
wire      [ 17: 0] tr_data;
wire                    tracemem_on;
wire      [ 35: 0] tracemem_trcdata;
wire                    tracemem_tw;
wire      [ 15: 0] trc_ctrl;
wire                    trc_enb;
wire      [  6: 0] trc_im_addr;
wire                    trc_on;
wire                    trc_wrap;
wire                    trigbrktype;
wire                    trigger_state_0;
wire                    trigger_state_1;
wire                    trigout;
wire      [ 35: 0] tw;
wire                    xbrk_break;
wire      [  7: 0] xbrk_ctrl0;
wire      [  7: 0] xbrk_ctrl1;
wire      [  7: 0] xbrk_ctrl2;
wire      [  7: 0] xbrk_ctrl3;
wire                    xbrk_goto0;
wire                    xbrk_goto1;
wire                    xbrk_traceoff;
wire                    xbrk_traceon;
wire                    xbrk_trigout;
wire                    xbrk_wrap_traceoff;
cpu_0_nios2_oci_debug the_cpu_0_nios2_oci_debug
  (
    .clk                    (clk),
    .dbrk_break             (dbrk_break),
    .debugack               (debugack),
    .debugreq               (debugreq),
    .hbreak_enabled         (hbreak_enabled),
    .jdo                    (jdo),
    .jrst_n                 (jrst_n),
    .monitor_error          (monitor_error),
    .monitor_go             (monitor_go),
```

```
      .monitor_ready              (monitor_ready),
      .oci_hbreak_req             (oci_hbreak_req),
      .ocireg_ers                 (ocireg_ers),
      .ocireg_mrs                 (ocireg_mrs),
      .reset                      (reset),
      .resetlatch                 (resetlatch),
      .resetrequest               (resetrequest),
      .st_ready_test_idle     (st_ready_test_idle),
      .take_action_ocimem_a (take_action_ocimem_a),
      .take_action_ocireg     (take_action_ocireg),
      .xbrk_break                 (xbrk_break)
   );

cpu_0_nios2_ocimem the_cpu_0_nios2_ocimem
   (
      .MonDReg                        (MonDReg),
      .address                        (address),
      .begintransfer                  (begintransfer),
      .byteenable                     (byteenable),
      .chipselect                     (chipselect),
      .clk                            (clk),
      .debugaccess                    (debugaccess),
      .jdo                            (jdo),
      .jrst_n                         (jrst_n),
      .oci_ram_readdata               (oci_ram_readdata),
      .resetrequest                   (resetrequest),
      .take_action_ocimem_a       (take_action_ocimem_a),
      .take_action_ocimem_b       (take_action_ocimem_b),
      .take_no_action_ocimem_a (take_no_action_ocimem_a),
      .write                          (write),
      .writedata                      (writedata)
   );

cpu_0_nios2_avalon_reg the_cpu_0_nios2_avalon_reg
   (
      .address                    (address),
      .chipselect                 (chipselect),
      .clk                        (clk),
      .debugaccess                (debugaccess),
      .monitor_error              (monitor_error),
      .monitor_go                 (monitor_go),
      .monitor_ready              (monitor_ready),
      .oci_ienable                (oci_ienable),
      .oci_reg_readdata           (oci_reg_readdata),
      .oci_single_step_mode (oci_single_step_mode),
      .ocireg_ers                 (ocireg_ers),
      .ocireg_mrs                 (ocireg_mrs),
      .reset_n                    (reset_n),
      .take_action_ocireg     (take_action_ocireg),
      .write                      (write),
      .writedata                  (writedata)
   );

cpu_0_nios2_oci_break the_cpu_0_nios2_oci_break
   (
      .break_readreg              (break_readreg),
      .clk                        (clk),
      .dbrk_break                 (dbrk_break),
```

```
      .dbrk_goto0                    (dbrk_goto0),
      .dbrk_goto1                    (dbrk_goto1),
      .dbrk_hit0_latch               (dbrk_hit0_latch),
      .dbrk_hit1_latch               (dbrk_hit1_latch),
      .dbrk_hit2_latch               (dbrk_hit2_latch),
      .dbrk_hit3_latch               (dbrk_hit3_latch),
      .jdo                           (jdo),
      .jrst_n                        (jrst_n),
      .reset_n                       (reset_n),
      .take_action_break_a           (take_action_break_a),
      .take_action_break_b           (take_action_break_b),
      .take_action_break_c           (take_action_break_c),
      .take_no_action_break_a (take_no_action_break_a),
      .take_no_action_break_b (take_no_action_break_b),
      .take_no_action_break_c (take_no_action_break_c),
      .trigbrktype                   (trigbrktype),
      .trigger_state_0               (trigger_state_0),
      .trigger_state_1               (trigger_state_1),
      .xbrk_ctrl0                    (xbrk_ctrl0),
      .xbrk_ctrl1                    (xbrk_ctrl1),
      .xbrk_ctrl2                    (xbrk_ctrl2),
      .xbrk_ctrl3                    (xbrk_ctrl3),
      .xbrk_goto0                    (xbrk_goto0),
      .xbrk_goto1                    (xbrk_goto1)
    );

cpu_0_nios2_oci_xbrk the_cpu_0_nios2_oci_xbrk
    (
      .D_valid               (D_valid),
      .E_valid               (E_valid),
      .F_pc                  (F_pc),
      .clk                   (clk),
      .reset_n               (reset_n),
      .trigger_state_0 (trigger_state_0),
      .trigger_state_1 (trigger_state_1),
      .xbrk_break            (xbrk_break),
      .xbrk_ctrl0            (xbrk_ctrl0),
      .xbrk_ctrl1            (xbrk_ctrl1),
      .xbrk_ctrl2            (xbrk_ctrl2),
      .xbrk_ctrl3            (xbrk_ctrl3),
      .xbrk_goto0            (xbrk_goto0),
      .xbrk_goto1            (xbrk_goto1),
      .xbrk_traceoff         (xbrk_traceoff),
      .xbrk_traceon          (xbrk_traceon),
      .xbrk_trigout          (xbrk_trigout)
    );

cpu_0_nios2_oci_dbrk the_cpu_0_nios2_oci_dbrk
    (
      .E_st_data                          (E_st_data),
      .av_ld_data_aligned_filtered (av_ld_data_aligned_filtered),
      .clk                                (clk),
      .cpu_d_address                      (cpu_d_address),
      .cpu_d_read                         (cpu_d_read),
      .cpu_d_readdata                     (cpu_d_readdata),
      .cpu_d_wait                         (cpu_d_wait),
      .cpu_d_write                        (cpu_d_write),
      .cpu_d_writedata                    (cpu_d_writedata),
```

```
      .d_address                    (d_address),
      .d_read                       (d_read),
      .d_waitrequest                (d_waitrequest),
      .d_write                      (d_write),
      .dbrk_break                   (dbrk_break),
      .dbrk_goto0                   (dbrk_goto0),
      .dbrk_goto1                   (dbrk_goto1),
      .dbrk_traceme                 (dbrk_traceme),
      .dbrk_traceoff                (dbrk_traceoff),
      .dbrk_traceon                 (dbrk_traceon),
      .dbrk_trigout                 (dbrk_trigout),
      .debugack                     (debugack),
      .reset_n                      (reset_n)
   );

cpu_0_nios2_oci_itrace the_cpu_0_nios2_oci_itrace
   (
      .clk                          (clk),
      .dbrk_traceoff                (dbrk_traceoff),
      .dbrk_traceon                 (dbrk_traceon),
      .dct_buffer                   (dct_buffer),
      .dct_count                    (dct_count),
      .itm                          (itm),
      .jdo                          (jdo),
      .jrst_n                       (jrst_n),
      .take_action_tracectrl (take_action_tracectrl),
      .trc_ctrl                     (trc_ctrl),
      .trc_enb                      (trc_enb),
      .trc_on                       (trc_on),
      .xbrk_traceoff                (xbrk_traceoff),
      .xbrk_traceon                 (xbrk_traceon),
      .xbrk_wrap_traceoff       (xbrk_wrap_traceoff)
   );

cpu_0_nios2_oci_dtrace the_cpu_0_nios2_oci_dtrace
   (
      .atm                      (atm),
      .clk                      (clk),
      .cpu_d_address      (cpu_d_address),
      .cpu_d_read          (cpu_d_read),
      .cpu_d_readdata    (cpu_d_readdata),
      .cpu_d_wait          (cpu_d_wait),
      .cpu_d_write         (cpu_d_write),
      .cpu_d_writedata (cpu_d_writedata),
      .dtm                      (dtm),
      .jrst_n                (jrst_n),
      .trc_ctrl             (trc_ctrl)
   );

cpu_0_nios2_oci_fifo the_cpu_0_nios2_oci_fifo
   (
      .atm                    (atm),
      .clk                    (clk),
      .dbrk_traceme      (dbrk_traceme),
      .dbrk_traceoff    (dbrk_traceoff),
      .dbrk_traceon      (dbrk_traceon),
      .dct_buffer         (dct_buffer),
      .dct_count          (dct_count),
```

```
      .dtm                  (dtm),
      .itm                  (itm),
      .jrst_n               (jrst_n),
      .reset_n              (reset_n),
      .test_ending          (test_ending),
      .test_has_ended (test_has_ended),
      .trc_on               (trc_on),
      .tw                   (tw)
   );

cpu_0_nios2_oci_pib the_cpu_0_nios2_oci_pib
   (
      .clk         (clk),
      .clkx2       (clkx2),
      .jrst_n      (jrst_n),
      .tr_clk      (tr_clk),
      .tr_data (tr_data),
      .tw          (tw)
   );

cpu_0_nios2_oci_im the_cpu_0_nios2_oci_im
   (
      .clk                                (clk),
      .jdo                                (jdo),
      .jrst_n                             (jrst_n),
      .reset_n                            (reset_n),
      .take_action_tracectrl         (take_action_tracectrl),
      .take_action_tracemem_a        (take_action_tracemem_a),
      .take_action_tracemem_b        (take_action_tracemem_b),
      .take_no_action_tracemem_a (take_no_action_tracemem_a),
      .tracemem_on                      (tracemem_on),
      .tracemem_trcdata                 (tracemem_trcdata),
      .tracemem_tw                      (tracemem_tw),
      .trc_ctrl                        (trc_ctrl),
      .trc_enb                          (trc_enb),
      .trc_im_addr                      (trc_im_addr),
      .trc_wrap                         (trc_wrap),
      .tw                               (tw),
      .xbrk_wrap_traceoff              (xbrk_wrap_traceoff)
   );

assign trigout = dbrk_trigout | xbrk_trigout;
assign readdata = address[8] ? oci_reg_readdata : oci_ram_readdata;
assign jtag_debug_module_debugaccess_to_roms = debugack;
cpu_0_jtag_debug_module_wrapper the_cpu_0_jtag_debug_module_wrapper
   (
      .MonDReg                          (MonDReg),
      .break_readreg                   (break_readreg),
      .clk                              (clk),
      .dbrk_hit0_latch                 (dbrk_hit0_latch),
      .dbrk_hit1_latch                 (dbrk_hit1_latch),
      .dbrk_hit2_latch                 (dbrk_hit2_latch),
      .dbrk_hit3_latch                 (dbrk_hit3_latch),
      .debugack                         (debugack),
      .jdo                              (jdo),
      .jrst_n                          (jrst_n),
      .monitor_error                    (monitor_error),
      .monitor_ready                    (monitor_ready),
```

```
        .reset_n                        (reset_n),
        .resetlatch                     (resetlatch),
        .st_ready_test_idle             (st_ready_test_idle),
        .take_action_break_a            (take_action_break_a),
        .take_action_break_b            (take_action_break_b),
        .take_action_break_c            (take_action_break_c),
        .take_action_ocimem_a           (take_action_ocimem_a),
        .take_action_ocimem_b           (take_action_ocimem_b),
        .take_action_tracectrl          (take_action_tracectrl),
        .take_action_tracemem_a         (take_action_tracemem_a),
        .take_action_tracemem_b         (take_action_tracemem_b),
        .take_no_action_break_a         (take_no_action_break_a),
        .take_no_action_break_b         (take_no_action_break_b),
        .take_no_action_break_c         (take_no_action_break_c),
        .take_no_action_ocimem_a        (take_no_action_ocimem_a),
        .take_no_action_tracemem_a      (take_no_action_tracemem_a),
        .tracemem_on                    (tracemem_on),
        .tracemem_trcdata               (tracemem_trcdata),
        .tracemem_tw                    (tracemem_tw),
        .trc_im_addr                    (trc_im_addr),
        .trc_on                         (trc_on),
        .trc_wrap                       (trc_wrap),
        .trigbrktype                    (trigbrktype),
        .trigger_state_1                (trigger_state_1)
      );

    //dummy sink, which is an e_mux
    assign dummy_sink = tr_clk |
      tr_data |
      trigout |
      debugack;

    assign debugreq = 0;
    assign clkx2 = 0;

endmodule


// synthesis translate_off
`timescale 1ns / 1ps
// synthesis translate_on

// turn off superfluous verilog processor warnings
// altera message_level Level1
// altera message_off 10034 10035 10036 10037 10230 10240 10030

module cpu_0 (
                      // inputs:
                        clk,
                        d_irq,
                        d_readdata,
                        d_waitrequest,
                        i_readdata,
                        i_waitrequest,
                        jtag_debug_module_address,
                        jtag_debug_module_begintransfer,
                        jtag_debug_module_byteenable,
                        jtag_debug_module_debugaccess,
```

```
                    jtag_debug_module_select,
                    jtag_debug_module_write,
                    jtag_debug_module_writedata,
                    reset_n,

                  // outputs:
                    d_address,
                    d_byteenable,
                    d_read,
                    d_write,
                    d_writedata,
                    i_address,
                    i_read,
                    jtag_debug_module_debugaccess_to_roms,
                    jtag_debug_module_readdata,
                    jtag_debug_module_resetrequest
                )
;

  output  [ 24: 0] d_address;
  output  [  3: 0] d_byteenable;
  output           d_read;
  output           d_write;
  output  [ 31: 0] d_writedata;
  output  [ 24: 0] i_address;
  output           i_read;
  output           jtag_debug_module_debugaccess_to_roms;
  output  [ 31: 0] jtag_debug_module_readdata;
  output           jtag_debug_module_resetrequest;
  input            clk;
  input   [ 31: 0] d_irq;
  input   [ 31: 0] d_readdata;
  input            d_waitrequest;
  input   [ 31: 0] i_readdata;
  input            i_waitrequest;
  input   [  8: 0] jtag_debug_module_address;
  input            jtag_debug_module_begintransfer;
  input   [  3: 0] jtag_debug_module_byteenable;
  input            jtag_debug_module_debugaccess;
  input            jtag_debug_module_select;
  input            jtag_debug_module_write;
  input   [ 31: 0] jtag_debug_module_writedata;
  input            reset_n;

  wire    [  1: 0] D_compare_op;
  wire             D_ctrl_alu_force_xor;
  wire             D_ctrl_alu_signed_comparison;
  wire             D_ctrl_alu_subtract;
  wire             D_ctrl_b_is_dst;
  wire             D_ctrl_br;
  wire             D_ctrl_br_cmp;
  wire             D_ctrl_br_uncond;
  wire             D_ctrl_break;
  wire             D_ctrl_crst;
  wire             D_ctrl_custom;
  wire             D_ctrl_custom_multi;
  wire             D_ctrl_exception;
  wire             D_ctrl_force_src2_zero;
```

```
wire            D_ctrl_hi_imm16;
wire            D_ctrl_ignore_dst;
wire            D_ctrl_implicit_dst_eretaddr;
wire            D_ctrl_implicit_dst_retaddr;
wire            D_ctrl_jmp_direct;
wire            D_ctrl_jmp_indirect;
wire            D_ctrl_ld;
wire            D_ctrl_ld_io;
wire            D_ctrl_ld_non_io;
wire            D_ctrl_ld_signed;
wire            D_ctrl_logic;
wire            D_ctrl_rdctl_inst;
wire            D_ctrl_retaddr;
wire            D_ctrl_rot_right;
wire            D_ctrl_shift_logical;
wire            D_ctrl_shift_right_arith;
wire            D_ctrl_shift_rot;
wire            D_ctrl_shift_rot_right;
wire            D_ctrl_src2_choose_imm;
wire            D_ctrl_st;
wire            D_ctrl_uncond_cti_non_br;
wire            D_ctrl_unsigned_lo_imm16;
wire            D_ctrl_wrctl_inst;
wire    [  4: 0] D_dst_regnum;
wire    [ 55: 0] D_inst;
reg     [ 31: 0] D_iw /* synthesis ALTERA_IP_DEBUG_VISIBLE = 1 */;
wire    [  4: 0] D_iw_a;
wire    [  4: 0] D_iw_b;
wire    [  4: 0] D_iw_c;
wire    [  2: 0] D_iw_control_regnum;
wire    [  7: 0] D_iw_custom_n;
wire            D_iw_custom_readra;
wire            D_iw_custom_readrb;
wire            D_iw_custom_writerc;
wire    [ 15: 0] D_iw_imm16;
wire    [ 25: 0] D_iw_imm26;
wire    [  4: 0] D_iw_imm5;
wire    [  1: 0] D_iw_memsz;
wire    [  5: 0] D_iw_op;
wire    [  5: 0] D_iw_opx;
wire    [  4: 0] D_iw_shift_imm5;
wire    [  4: 0] D_iw_trap_break_imm5;
wire    [ 22: 0] D_jmp_direct_target_waddr;
wire    [  1: 0] D_logic_op;
wire    [  1: 0] D_logic_op_raw;
wire            D_mem16;
wire            D_mem32;
wire            D_mem8;
wire            D_op_add;
wire            D_op_addi;
wire            D_op_and;
wire            D_op_andhi;
wire            D_op_andi;
wire            D_op_beq;
wire            D_op_bge;
wire            D_op_bgeu;
wire            D_op_blt;
wire            D_op_bltu;
```

```
wire        D_op_bne;
wire        D_op_br;
wire        D_op_break;
wire        D_op_bret;
wire        D_op_call;
wire        D_op_callr;
wire        D_op_cmpeq;
wire        D_op_cmpeqi;
wire        D_op_cmpge;
wire        D_op_cmpgei;
wire        D_op_cmpgeu;
wire        D_op_cmpgeui;
wire        D_op_cmplt;
wire        D_op_cmplti;
wire        D_op_cmpltu;
wire        D_op_cmpltui;
wire        D_op_cmpne;
wire        D_op_cmpnei;
wire        D_op_crst;
wire        D_op_custom;
wire        D_op_div;
wire        D_op_divu;
wire        D_op_eret;
wire        D_op_flushd;
wire        D_op_flushda;
wire        D_op_flushi;
wire        D_op_flushp;
wire        D_op_hbreak;
wire        D_op_initd;
wire        D_op_initda;
wire        D_op_initi;
wire        D_op_intr;
wire        D_op_jmp;
wire        D_op_jmpi;
wire        D_op_ldb;
wire        D_op_ldbio;
wire        D_op_ldbu;
wire        D_op_ldbuio;
wire        D_op_ldh;
wire        D_op_ldhio;
wire        D_op_ldhu;
wire        D_op_ldhuio;
wire        D_op_ldl;
wire        D_op_ldw;
wire        D_op_ldwio;
wire        D_op_mul;
wire        D_op_muli;
wire        D_op_mulxss;
wire        D_op_mulxsu;
wire        D_op_mulxuu;
wire        D_op_nextpc;
wire        D_op_nor;
wire        D_op_opx;
wire        D_op_or;
wire        D_op_orhi;
wire        D_op_ori;
wire        D_op_rdctl;
wire        D_op_rdprs;
```

```
wire            D_op_ret;
wire            D_op_rol;
wire            D_op_roli;
wire            D_op_ror;
wire            D_op_rsv02;
wire            D_op_rsv09;
wire            D_op_rsv10;
wire            D_op_rsv17;
wire            D_op_rsv18;
wire            D_op_rsv25;
wire            D_op_rsv26;
wire            D_op_rsv33;
wire            D_op_rsv34;
wire            D_op_rsv41;
wire            D_op_rsv42;
wire            D_op_rsv49;
wire            D_op_rsv57;
wire            D_op_rsv61;
wire            D_op_rsv62;
wire            D_op_rsv63;
wire            D_op_rsvx00;
wire            D_op_rsvx10;
wire            D_op_rsvx15;
wire            D_op_rsvx17;
wire            D_op_rsvx21;
wire            D_op_rsvx25;
wire            D_op_rsvx33;
wire            D_op_rsvx34;
wire            D_op_rsvx35;
wire            D_op_rsvx42;
wire            D_op_rsvx43;
wire            D_op_rsvx44;
wire            D_op_rsvx47;
wire            D_op_rsvx50;
wire            D_op_rsvx51;
wire            D_op_rsvx55;
wire            D_op_rsvx56;
wire            D_op_rsvx60;
wire            D_op_rsvx63;
wire            D_op_sll;
wire            D_op_slli;
wire            D_op_sra;
wire            D_op_srai;
wire            D_op_srl;
wire            D_op_srli;
wire            D_op_stb;
wire            D_op_stbio;
wire            D_op_stc;
wire            D_op_sth;
wire            D_op_sthio;
wire            D_op_stw;
wire            D_op_stwio;
wire            D_op_sub;
wire            D_op_sync;
wire            D_op_trap;
wire            D_op_wrctl;
wire            D_op_wrprs;
wire            D_op_xor;
```

```
wire            D_op_xorhi;
wire            D_op_xori;
reg             D_valid;
wire    [ 55: 0] D_vinst;
wire            D_wr_dst_reg;
wire    [ 31: 0] E_alu_result;
reg             E_alu_sub;
wire    [ 32: 0] E_arith_result;
wire    [ 31: 0] E_arith_src1;
wire    [ 31: 0] E_arith_src2;
wire            E_ci_multi_stall;
wire    [ 31: 0] E_ci_result;
wire            E_cmp_result;
wire    [ 31: 0] E_control_rd_data;
wire            E_eq;
reg             E_invert_arith_src_msb;
wire            E_ld_stall;
wire    [ 31: 0] E_logic_result;
wire            E_logic_result_is_0;
wire            E_lt;
wire    [ 24: 0] E_mem_baddr;
wire    [  3: 0] E_mem_byte_en;
reg             E_new_inst;
reg     [  4: 0] E_shift_rot_cnt;
wire    [  4: 0] E_shift_rot_cnt_nxt;
wire            E_shift_rot_done;
wire            E_shift_rot_fill_bit;
reg     [ 31: 0] E_shift_rot_result;
wire    [ 31: 0] E_shift_rot_result_nxt;
wire            E_shift_rot_stall;
reg     [ 31: 0] E_src1;
reg     [ 31: 0] E_src2;
wire    [ 31: 0] E_st_data;
wire            E_st_stall;
wire            E_stall;
reg             E_valid;
wire    [ 55: 0] E_vinst;
wire            E_wrctl_bstatus;
wire            E_wrctl_estatus;
wire            E_wrctl_ienable;
wire            E_wrctl_status;
wire    [ 31: 0] F_av_iw;
wire    [  4: 0] F_av_iw_a;
wire    [  4: 0] F_av_iw_b;
wire    [  4: 0] F_av_iw_c;
wire    [  2: 0] F_av_iw_control_regnum;
wire    [  7: 0] F_av_iw_custom_n;
wire            F_av_iw_custom_readra;
wire            F_av_iw_custom_readrb;
wire            F_av_iw_custom_writerc;
wire    [ 15: 0] F_av_iw_imm16;
wire    [ 25: 0] F_av_iw_imm26;
wire    [  4: 0] F_av_iw_imm5;
wire    [  1: 0] F_av_iw_memsz;
wire    [  5: 0] F_av_iw_op;
wire    [  5: 0] F_av_iw_opx;
wire    [  4: 0] F_av_iw_shift_imm5;
wire    [  4: 0] F_av_iw_trap_break_imm5;
```

```
wire            F_av_mem16;
wire            F_av_mem32;
wire            F_av_mem8;
wire    [ 55: 0] F_inst;
wire    [ 31: 0] F_iw;
wire    [  4: 0] F_iw_a;
wire    [  4: 0] F_iw_b;
wire    [  4: 0] F_iw_c;
wire    [  2: 0] F_iw_control_regnum;
wire    [  7: 0] F_iw_custom_n;
wire            F_iw_custom_readra;
wire            F_iw_custom_readrb;
wire            F_iw_custom_writerc;
wire    [ 15: 0] F_iw_imm16;
wire    [ 25: 0] F_iw_imm26;
wire    [  4: 0] F_iw_imm5;
wire    [  1: 0] F_iw_memsz;
wire    [  5: 0] F_iw_op;
wire    [  5: 0] F_iw_opx;
wire    [  4: 0] F_iw_shift_imm5;
wire    [  4: 0] F_iw_trap_break_imm5;
wire            F_mem16;
wire            F_mem32;
wire            F_mem8;
wire            F_op_add;
wire            F_op_addi;
wire            F_op_and;
wire            F_op_andhi;
wire            F_op_andi;
wire            F_op_beq;
wire            F_op_bge;
wire            F_op_bgeu;
wire            F_op_blt;
wire            F_op_bltu;
wire            F_op_bne;
wire            F_op_br;
wire            F_op_break;
wire            F_op_bret;
wire            F_op_call;
wire            F_op_callr;
wire            F_op_cmpeq;
wire            F_op_cmpeqi;
wire            F_op_cmpge;
wire            F_op_cmpgei;
wire            F_op_cmpgeu;
wire            F_op_cmpgeui;
wire            F_op_cmplt;
wire            F_op_cmplti;
wire            F_op_cmpltu;
wire            F_op_cmpltui;
wire            F_op_cmpne;
wire            F_op_cmpnei;
wire            F_op_crst;
wire            F_op_custom;
wire            F_op_div;
wire            F_op_divu;
wire            F_op_eret;
wire            F_op_flushd;
```

```
wire        F_op_flushda;
wire        F_op_flushi;
wire        F_op_flushp;
wire        F_op_hbreak;
wire        F_op_initd;
wire        F_op_initda;
wire        F_op_initi;
wire        F_op_intr;
wire        F_op_jmp;
wire        F_op_jmpi;
wire        F_op_ldb;
wire        F_op_ldbio;
wire        F_op_ldbu;
wire        F_op_ldbuio;
wire        F_op_ldh;
wire        F_op_ldhio;
wire        F_op_ldhu;
wire        F_op_ldhuio;
wire        F_op_ldl;
wire        F_op_ldw;
wire        F_op_ldwio;
wire        F_op_mul;
wire        F_op_muli;
wire        F_op_mulxss;
wire        F_op_mulxsu;
wire        F_op_mulxuu;
wire        F_op_nextpc;
wire        F_op_nor;
wire        F_op_opx;
wire        F_op_or;
wire        F_op_orhi;
wire        F_op_ori;
wire        F_op_rdctl;
wire        F_op_rdprs;
wire        F_op_ret;
wire        F_op_rol;
wire        F_op_roli;
wire        F_op_ror;
wire        F_op_rsv02;
wire        F_op_rsv09;
wire        F_op_rsv10;
wire        F_op_rsv17;
wire        F_op_rsv18;
wire        F_op_rsv25;
wire        F_op_rsv26;
wire        F_op_rsv33;
wire        F_op_rsv34;
wire        F_op_rsv41;
wire        F_op_rsv42;
wire        F_op_rsv49;
wire        F_op_rsv57;
wire        F_op_rsv61;
wire        F_op_rsv62;
wire        F_op_rsv63;
wire        F_op_rsvx00;
wire        F_op_rsvx10;
wire        F_op_rsvx15;
wire        F_op_rsvx17;
```

```
wire            F_op_rsvx21;
wire            F_op_rsvx25;
wire            F_op_rsvx33;
wire            F_op_rsvx34;
wire            F_op_rsvx35;
wire            F_op_rsvx42;
wire            F_op_rsvx43;
wire            F_op_rsvx44;
wire            F_op_rsvx47;
wire            F_op_rsvx50;
wire            F_op_rsvx51;
wire            F_op_rsvx55;
wire            F_op_rsvx56;
wire            F_op_rsvx60;
wire            F_op_rsvx63;
wire            F_op_sll;
wire            F_op_slli;
wire            F_op_sra;
wire            F_op_srai;
wire            F_op_srl;
wire            F_op_srli;
wire            F_op_stb;
wire            F_op_stbio;
wire            F_op_stc;
wire            F_op_sth;
wire            F_op_sthio;
wire            F_op_stw;
wire            F_op_stwio;
wire            F_op_sub;
wire            F_op_sync;
wire            F_op_trap;
wire            F_op_wrctl;
wire            F_op_wrprs;
wire            F_op_xor;
wire            F_op_xorhi;
wire            F_op_xori;
reg     [ 22: 0] F_pc /* synthesis ALTERA_IP_DEBUG_VISIBLE = 1 */;
wire            F_pc_en;
wire    [ 22: 0] F_pc_no_crst_nxt;
wire    [ 22: 0] F_pc_nxt;
wire    [ 22: 0] F_pc_plus_one;
wire    [  1: 0] F_pc_sel_nxt;
wire    [ 24: 0] F_pcb;
wire    [ 24: 0] F_pcb_nxt;
wire    [ 24: 0] F_pcb_plus_four;
wire            F_valid;
wire    [ 55: 0] F_vinst;
reg     [  1: 0] R_compare_op;
reg             R_ctrl_alu_force_xor;
wire            R_ctrl_alu_force_xor_nxt;
reg             R_ctrl_alu_signed_comparison;
wire            R_ctrl_alu_signed_comparison_nxt;
reg             R_ctrl_alu_subtract;
wire            R_ctrl_alu_subtract_nxt;
reg             R_ctrl_b_is_dst;
wire            R_ctrl_b_is_dst_nxt;
reg             R_ctrl_br;
reg             R_ctrl_br_cmp;
```

```
wire        R_ctrl_br_cmp_nxt;
wire        R_ctrl_br_nxt;
reg         R_ctrl_br_uncond;
wire        R_ctrl_br_uncond_nxt;
reg         R_ctrl_break;
wire        R_ctrl_break_nxt;
reg         R_ctrl_crst;
wire        R_ctrl_crst_nxt;
reg         R_ctrl_custom;
reg         R_ctrl_custom_multi;
wire        R_ctrl_custom_multi_nxt;
wire        R_ctrl_custom_nxt;
reg         R_ctrl_exception;
wire        R_ctrl_exception_nxt;
reg         R_ctrl_force_src2_zero;
wire        R_ctrl_force_src2_zero_nxt;
reg         R_ctrl_hi_imm16;
wire        R_ctrl_hi_imm16_nxt;
reg         R_ctrl_ignore_dst;
wire        R_ctrl_ignore_dst_nxt;
reg         R_ctrl_implicit_dst_eretaddr;
wire        R_ctrl_implicit_dst_eretaddr_nxt;
reg         R_ctrl_implicit_dst_retaddr;
wire        R_ctrl_implicit_dst_retaddr_nxt;
reg         R_ctrl_jmp_direct;
wire        R_ctrl_jmp_direct_nxt;
reg         R_ctrl_jmp_indirect;
wire        R_ctrl_jmp_indirect_nxt;
reg         R_ctrl_ld;
reg         R_ctrl_ld_io;
wire        R_ctrl_ld_io_nxt;
reg         R_ctrl_ld_non_io;
wire        R_ctrl_ld_non_io_nxt;
wire        R_ctrl_ld_nxt;
reg         R_ctrl_ld_signed;
wire        R_ctrl_ld_signed_nxt;
reg         R_ctrl_logic;
wire        R_ctrl_logic_nxt;
reg         R_ctrl_rdctl_inst;
wire        R_ctrl_rdctl_inst_nxt;
reg         R_ctrl_retaddr;
wire        R_ctrl_retaddr_nxt;
reg         R_ctrl_rot_right;
wire        R_ctrl_rot_right_nxt;
reg         R_ctrl_shift_logical;
wire        R_ctrl_shift_logical_nxt;
reg         R_ctrl_shift_right_arith;
wire        R_ctrl_shift_right_arith_nxt;
reg         R_ctrl_shift_rot;
wire        R_ctrl_shift_rot_nxt;
reg         R_ctrl_shift_rot_right;
wire        R_ctrl_shift_rot_right_nxt;
reg         R_ctrl_src2_choose_imm;
wire        R_ctrl_src2_choose_imm_nxt;
reg         R_ctrl_st;
wire        R_ctrl_st_nxt;
reg         R_ctrl_uncond_cti_non_br;
wire        R_ctrl_uncond_cti_non_br_nxt;
```

```
reg             R_ctrl_unsigned_lo_imm16;
wire            R_ctrl_unsigned_lo_imm16_nxt;
reg             R_ctrl_wrctl_inst;
wire            R_ctrl_wrctl_inst_nxt;
reg     [  4: 0] R_dst_regnum /* synthesis ALTERA_IP_DEBUG_VISIBLE = 1 */;
wire            R_en;
reg     [  1: 0] R_logic_op;
wire    [ 31: 0] R_rf_a;
wire    [ 31: 0] R_rf_b;
wire    [ 31: 0] R_src1;
wire    [ 31: 0] R_src2;
wire    [ 15: 0] R_src2_hi;
wire    [ 15: 0] R_src2_lo;
reg             R_src2_use_imm;
wire    [  7: 0] R_stb_data;
wire    [ 15: 0] R_sth_data;
reg             R_valid;
wire    [ 55: 0] R_vinst;
reg             R_wr_dst_reg;
reg     [ 31: 0] W_alu_result;
wire            W_br_taken;
reg             W_bstatus_reg;
wire            W_bstatus_reg_inst_nxt;
wire            W_bstatus_reg_nxt;
reg             W_cmp_result;
reg     [ 31: 0] W_control_rd_data;
reg             W_estatus_reg;
wire            W_estatus_reg_inst_nxt;
wire            W_estatus_reg_nxt;
reg     [ 31: 0] W_ienable_reg;
wire    [ 31: 0] W_ienable_reg_nxt;
reg     [ 31: 0] W_ipending_reg;
wire    [ 31: 0] W_ipending_reg_nxt;
wire    [ 24: 0] W_mem_baddr;
wire    [ 31: 0] W_rf_wr_data;
wire            W_rf_wren;
wire            W_status_reg;
reg             W_status_reg_pie;
wire            W_status_reg_pie_inst_nxt;
wire            W_status_reg_pie_nxt;
reg             W_valid /* synthesis ALTERA_IP_DEBUG_VISIBLE = 1 */;
wire    [ 55: 0] W_vinst;
wire    [ 31: 0] W_wr_data;
wire    [ 31: 0] W_wr_data_non_zero;
wire            av_fill_bit;
reg     [  1: 0] av_ld_align_cycle;
wire    [  1: 0] av_ld_align_cycle_nxt;
wire            av_ld_align_one_more_cycle;
reg             av_ld_aligning_data;
wire            av_ld_aligning_data_nxt;
reg     [  7: 0] av_ld_byte0_data;
wire    [  7: 0] av_ld_byte0_data_nxt;
reg     [  7: 0] av_ld_byte1_data;
wire            av_ld_byte1_data_en;
wire    [  7: 0] av_ld_byte1_data_nxt;
reg     [  7: 0] av_ld_byte2_data;
wire    [  7: 0] av_ld_byte2_data_nxt;
reg     [  7: 0] av_ld_byte3_data;
```

```
wire       [    7: 0] av_ld_byte3_data_nxt;
wire       [ 31: 0] av_ld_data_aligned_filtered;
wire       [ 31: 0] av_ld_data_aligned_unfiltered;
wire                av_ld_done;
wire                av_ld_extend;
wire                av_ld_getting_data;
wire                av_ld_rshift8;
reg                 av_ld_waiting_for_data;
wire                av_ld_waiting_for_data_nxt;
wire                av_sign_bit;
wire       [ 24: 0] d_address;
reg        [    3: 0] d_byteenable;
reg                 d_read;
wire                d_read_nxt;
wire                d_write;
wire                d_write_nxt;
reg        [ 31: 0] d_writedata;
reg                 hbreak_enabled;
reg                 hbreak_pending;
wire                hbreak_pending_nxt;
wire                hbreak_req;
wire       [ 24: 0] i_address;
reg                 i_read;
wire                i_read_nxt;
wire       [ 31: 0] iactive;
wire                intr_req;
wire                jtag_debug_module_clk;
wire                jtag_debug_module_debugaccess_to_roms;
wire       [ 31: 0] jtag_debug_module_readdata;
wire                jtag_debug_module_reset;
wire                jtag_debug_module_resetrequest;
wire                oci_hbreak_req;
wire       [ 31: 0] oci_ienable;
wire                oci_single_step_mode;
wire                oci_tb_hbreak_req;
wire                test_ending;
wire                test_has_ended;
reg                 wait_for_one_post_bret_inst;
//the_cpu_0_test_bench, which is an e_instance
cpu_0_test_bench the_cpu_0_test_bench
  (
    .D_iw                               (D_iw),
    .D_iw_op                            (D_iw_op),
    .D_iw_opx                           (D_iw_opx),
    .D_valid                           (D_valid),
    .E_alu_result                      (E_alu_result),
    .E_mem_byte_en                        (E_mem_byte_en),
    .E_st_data                         (E_st_data),
    .E_valid                           (E_valid),
    .F_pcb                              (F_pcb),
    .F_valid                           (F_valid),
    .R_ctrl_exception                  (R_ctrl_exception),
    .R_ctrl_ld                         (R_ctrl_ld),
    .R_ctrl_ld_non_io                  (R_ctrl_ld_non_io),
    .R_dst_regnum                         (R_dst_regnum),
    .R_wr_dst_reg                      (R_wr_dst_reg),
    .W_bstatus_reg                     (W_bstatus_reg),
    .W_cmp_result                       (W_cmp_result),
```

```
        .W_estatus_reg                      (W_estatus_reg),
        .W_ienable_reg                      (W_ienable_reg),
        .W_ipending_reg                     (W_ipending_reg),
        .W_mem_baddr                        (W_mem_baddr),
        .W_rf_wr_data                       (W_rf_wr_data),
        .W_status_reg                       (W_status_reg),
        .W_valid                            (W_valid),
        .W_vinst                            (W_vinst),
        .W_wr_data                          (W_wr_data),
        .av_ld_data_aligned_filtered    (av_ld_data_aligned_filtered),
        .av_ld_data_aligned_unfiltered (av_ld_data_aligned_unfiltered),
        .clk                                (clk),
        .d_address                          (d_address),
        .d_byteenable                       (d_byteenable),
        .d_read                             (d_read),
        .d_write                            (d_write),
        .d_write_nxt                        (d_write_nxt),
        .i_address                          (i_address),
        .i_read                             (i_read),
        .i_readdata                         (i_readdata),
        .i_waitrequest                      (i_waitrequest),
        .reset_n                            (reset_n),
        .test_has_ended                     (test_has_ended)
    );

assign F_av_iw_a = F_av_iw[31 : 27];
assign F_av_iw_b = F_av_iw[26 : 22];
assign F_av_iw_c = F_av_iw[21 : 17];
assign F_av_iw_custom_n = F_av_iw[13 : 6];
assign F_av_iw_custom_readra = F_av_iw[16];
assign F_av_iw_custom_readrb = F_av_iw[15];
assign F_av_iw_custom_writerc = F_av_iw[14];
assign F_av_iw_opx = F_av_iw[16 : 11];
assign F_av_iw_op = F_av_iw[5 : 0];
assign F_av_iw_shift_imm5 = F_av_iw[10 : 6];
assign F_av_iw_trap_break_imm5 = F_av_iw[10 : 6];
assign F_av_iw_imm5 = F_av_iw[10 : 6];
assign F_av_iw_imm16 = F_av_iw[21 : 6];
assign F_av_iw_imm26 = F_av_iw[31 : 6];
assign F_av_iw_memsz = F_av_iw[4 : 3];
assign F_av_iw_control_regnum = F_av_iw[8 : 6];
assign F_av_mem8 = F_av_iw_memsz == 2'b00;
assign F_av_mem16 = F_av_iw_memsz == 2'b01;
assign F_av_mem32 = F_av_iw_memsz[1] == 1'b1;
assign F_iw_a = F_iw[31 : 27];
assign F_iw_b = F_iw[26 : 22];
assign F_iw_c = F_iw[21 : 17];
assign F_iw_custom_n = F_iw[13 : 6];
assign F_iw_custom_readra = F_iw[16];
assign F_iw_custom_readrb = F_iw[15];
assign F_iw_custom_writerc = F_iw[14];
assign F_iw_opx = F_iw[16 : 11];
assign F_iw_op = F_iw[5 : 0];
assign F_iw_shift_imm5 = F_iw[10 : 6];
assign F_iw_trap_break_imm5 = F_iw[10 : 6];
assign F_iw_imm5 = F_iw[10 : 6];
assign F_iw_imm16 = F_iw[21 : 6];
assign F_iw_imm26 = F_iw[31 : 6];
```

```
assign F_iw_memsz = F_iw[4 : 3];
assign F_iw_control_regnum = F_iw[8 : 6];
assign F_mem8 = F_iw_memsz == 2'b00;
assign F_mem16 = F_iw_memsz == 2'b01;
assign F_mem32 = F_iw_memsz[1] == 1'b1;
assign D_iw_a = D_iw[31 : 27];
assign D_iw_b = D_iw[26 : 22];
assign D_iw_c = D_iw[21 : 17];
assign D_iw_custom_n = D_iw[13 : 6];
assign D_iw_custom_readra = D_iw[16];
assign D_iw_custom_readrb = D_iw[15];
assign D_iw_custom_writerc = D_iw[14];
assign D_iw_opx = D_iw[16 : 11];
assign D_iw_op = D_iw[5 : 0];
assign D_iw_shift_imm5 = D_iw[10 : 6];
assign D_iw_trap_break_imm5 = D_iw[10 : 6];
assign D_iw_imm5 = D_iw[10 : 6];
assign D_iw_imm16 = D_iw[21 : 6];
assign D_iw_imm26 = D_iw[31 : 6];
assign D_iw_memsz = D_iw[4 : 3];
assign D_iw_control_regnum = D_iw[8 : 6];
assign D_mem8 = D_iw_memsz == 2'b00;
assign D_mem16 = D_iw_memsz == 2'b01;
assign D_mem32 = D_iw_memsz[1] == 1'b1;
assign F_op_call = F_iw_op == 0;
assign F_op_jmpi = F_iw_op == 1;
assign F_op_ldbu = F_iw_op == 3;
assign F_op_addi = F_iw_op == 4;
assign F_op_stb = F_iw_op == 5;
assign F_op_br = F_iw_op == 6;
assign F_op_ldb = F_iw_op == 7;
assign F_op_cmpgei = F_iw_op == 8;
assign F_op_ldhu = F_iw_op == 11;
assign F_op_andi = F_iw_op == 12;
assign F_op_sth = F_iw_op == 13;
assign F_op_bge = F_iw_op == 14;
assign F_op_ldh = F_iw_op == 15;
assign F_op_cmplti = F_iw_op == 16;
assign F_op_initda = F_iw_op == 19;
assign F_op_ori = F_iw_op == 20;
assign F_op_stw = F_iw_op == 21;
assign F_op_blt = F_iw_op == 22;
assign F_op_ldw = F_iw_op == 23;
assign F_op_cmpnei = F_iw_op == 24;
assign F_op_flushda = F_iw_op == 27;
assign F_op_xori = F_iw_op == 28;
assign F_op_stc = F_iw_op == 29;
assign F_op_bne = F_iw_op == 30;
assign F_op_ldl = F_iw_op == 31;
assign F_op_cmpeqi = F_iw_op == 32;
assign F_op_ldbuio = F_iw_op == 35;
assign F_op_muli = F_iw_op == 36;
assign F_op_stbio = F_iw_op == 37;
assign F_op_beq = F_iw_op == 38;
assign F_op_ldbio = F_iw_op == 39;
assign F_op_cmpgeui = F_iw_op == 40;
assign F_op_ldhuio = F_iw_op == 43;
assign F_op_andhi = F_iw_op == 44;
```

```
assign F_op_sthio = F_iw_op == 45;
assign F_op_bgeu = F_iw_op == 46;
assign F_op_ldhio = F_iw_op == 47;
assign F_op_cmpltui = F_iw_op == 48;
assign F_op_initd = F_iw_op == 51;
assign F_op_orhi = F_iw_op == 52;
assign F_op_stwio = F_iw_op == 53;
assign F_op_bltu = F_iw_op == 54;
assign F_op_ldwio = F_iw_op == 55;
assign F_op_rdprs = F_iw_op == 56;
assign F_op_flushd = F_iw_op == 59;
assign F_op_xorhi = F_iw_op == 60;
assign F_op_rsv02 = F_iw_op == 2;
assign F_op_rsv09 = F_iw_op == 9;
assign F_op_rsv10 = F_iw_op == 10;
assign F_op_rsv17 = F_iw_op == 17;
assign F_op_rsv18 = F_iw_op == 18;
assign F_op_rsv25 = F_iw_op == 25;
assign F_op_rsv26 = F_iw_op == 26;
assign F_op_rsv33 = F_iw_op == 33;
assign F_op_rsv34 = F_iw_op == 34;
assign F_op_rsv41 = F_iw_op == 41;
assign F_op_rsv42 = F_iw_op == 42;
assign F_op_rsv49 = F_iw_op == 49;
assign F_op_rsv57 = F_iw_op == 57;
assign F_op_rsv61 = F_iw_op == 61;
assign F_op_rsv62 = F_iw_op == 62;
assign F_op_rsv63 = F_iw_op == 63;
assign F_op_eret = F_op_opx & (F_iw_opx == 1);
assign F_op_roli = F_op_opx & (F_iw_opx == 2);
assign F_op_rol = F_op_opx & (F_iw_opx == 3);
assign F_op_flushp = F_op_opx & (F_iw_opx == 4);
assign F_op_ret = F_op_opx & (F_iw_opx == 5);
assign F_op_nor = F_op_opx & (F_iw_opx == 6);
assign F_op_mulxuu = F_op_opx & (F_iw_opx == 7);
assign F_op_cmpge = F_op_opx & (F_iw_opx == 8);
assign F_op_bret = F_op_opx & (F_iw_opx == 9);
assign F_op_ror = F_op_opx & (F_iw_opx == 11);
assign F_op_flushi = F_op_opx & (F_iw_opx == 12);
assign F_op_jmp = F_op_opx & (F_iw_opx == 13);
assign F_op_and = F_op_opx & (F_iw_opx == 14);
assign F_op_cmplt = F_op_opx & (F_iw_opx == 16);
assign F_op_slli = F_op_opx & (F_iw_opx == 18);
assign F_op_sll = F_op_opx & (F_iw_opx == 19);
assign F_op_wrprs = F_op_opx & (F_iw_opx == 20);
assign F_op_or = F_op_opx & (F_iw_opx == 22);
assign F_op_mulxsu = F_op_opx & (F_iw_opx == 23);
assign F_op_cmpne = F_op_opx & (F_iw_opx == 24);
assign F_op_srli = F_op_opx & (F_iw_opx == 26);
assign F_op_srl = F_op_opx & (F_iw_opx == 27);
assign F_op_nextpc = F_op_opx & (F_iw_opx == 28);
assign F_op_callr = F_op_opx & (F_iw_opx == 29);
assign F_op_xor = F_op_opx & (F_iw_opx == 30);
assign F_op_mulxss = F_op_opx & (F_iw_opx == 31);
assign F_op_cmpeq = F_op_opx & (F_iw_opx == 32);
assign F_op_divu = F_op_opx & (F_iw_opx == 36);
assign F_op_div = F_op_opx & (F_iw_opx == 37);
assign F_op_rdctl = F_op_opx & (F_iw_opx == 38);
```

```
assign F_op_mul = F_op_opx & (F_iw_opx == 39);
assign F_op_cmpgeu = F_op_opx & (F_iw_opx == 40);
assign F_op_initi = F_op_opx & (F_iw_opx == 41);
assign F_op_trap = F_op_opx & (F_iw_opx == 45);
assign F_op_wrctl = F_op_opx & (F_iw_opx == 46);
assign F_op_cmpltu = F_op_opx & (F_iw_opx == 48);
assign F_op_add = F_op_opx & (F_iw_opx == 49);
assign F_op_break = F_op_opx & (F_iw_opx == 52);
assign F_op_hbreak = F_op_opx & (F_iw_opx == 53);
assign F_op_sync = F_op_opx & (F_iw_opx == 54);
assign F_op_sub = F_op_opx & (F_iw_opx == 57);
assign F_op_srai = F_op_opx & (F_iw_opx == 58);
assign F_op_sra = F_op_opx & (F_iw_opx == 59);
assign F_op_intr = F_op_opx & (F_iw_opx == 61);
assign F_op_crst = F_op_opx & (F_iw_opx == 62);
assign F_op_rsvx00 = F_op_opx & (F_iw_opx == 0);
assign F_op_rsvx10 = F_op_opx & (F_iw_opx == 10);
assign F_op_rsvx15 = F_op_opx & (F_iw_opx == 15);
assign F_op_rsvx17 = F_op_opx & (F_iw_opx == 17);
assign F_op_rsvx21 = F_op_opx & (F_iw_opx == 21);
assign F_op_rsvx25 = F_op_opx & (F_iw_opx == 25);
assign F_op_rsvx33 = F_op_opx & (F_iw_opx == 33);
assign F_op_rsvx34 = F_op_opx & (F_iw_opx == 34);
assign F_op_rsvx35 = F_op_opx & (F_iw_opx == 35);
assign F_op_rsvx42 = F_op_opx & (F_iw_opx == 42);
assign F_op_rsvx43 = F_op_opx & (F_iw_opx == 43);
assign F_op_rsvx44 = F_op_opx & (F_iw_opx == 44);
assign F_op_rsvx47 = F_op_opx & (F_iw_opx == 47);
assign F_op_rsvx50 = F_op_opx & (F_iw_opx == 50);
assign F_op_rsvx51 = F_op_opx & (F_iw_opx == 51);
assign F_op_rsvx55 = F_op_opx & (F_iw_opx == 55);
assign F_op_rsvx56 = F_op_opx & (F_iw_opx == 56);
assign F_op_rsvx60 = F_op_opx & (F_iw_opx == 60);
assign F_op_rsvx63 = F_op_opx & (F_iw_opx == 63);
assign F_op_opx = F_iw_op == 58;
assign F_op_custom = F_iw_op == 50;
assign D_op_call = D_iw_op == 0;
assign D_op_jmpi = D_iw_op == 1;
assign D_op_ldbu = D_iw_op == 3;
assign D_op_addi = D_iw_op == 4;
assign D_op_stb = D_iw_op == 5;
assign D_op_br = D_iw_op == 6;
assign D_op_ldb = D_iw_op == 7;
assign D_op_cmpgei = D_iw_op == 8;
assign D_op_ldhu = D_iw_op == 11;
assign D_op_andi = D_iw_op == 12;
assign D_op_sth = D_iw_op == 13;
assign D_op_bge = D_iw_op == 14;
assign D_op_ldh = D_iw_op == 15;
assign D_op_cmplti = D_iw_op == 16;
assign D_op_initda = D_iw_op == 19;
assign D_op_ori = D_iw_op == 20;
assign D_op_stw = D_iw_op == 21;
assign D_op_blt = D_iw_op == 22;
assign D_op_ldw = D_iw_op == 23;
assign D_op_cmpnei = D_iw_op == 24;
assign D_op_flushda = D_iw_op == 27;
assign D_op_xori = D_iw_op == 28;
```

```
assign D_op_stc = D_iw_op == 29;
assign D_op_bne = D_iw_op == 30;
assign D_op_ldl = D_iw_op == 31;
assign D_op_cmpeqi = D_iw_op == 32;
assign D_op_ldbuio = D_iw_op == 35;
assign D_op_muli = D_iw_op == 36;
assign D_op_stbio = D_iw_op == 37;
assign D_op_beq = D_iw_op == 38;
assign D_op_ldbio = D_iw_op == 39;
assign D_op_cmpgeui = D_iw_op == 40;
assign D_op_ldhuio = D_iw_op == 43;
assign D_op_andhi = D_iw_op == 44;
assign D_op_sthio = D_iw_op == 45;
assign D_op_bgeu = D_iw_op == 46;
assign D_op_ldhio = D_iw_op == 47;
assign D_op_cmpltui = D_iw_op == 48;
assign D_op_initd = D_iw_op == 51;
assign D_op_orhi = D_iw_op == 52;
assign D_op_stwio = D_iw_op == 53;
assign D_op_bltu = D_iw_op == 54;
assign D_op_ldwio = D_iw_op == 55;
assign D_op_rdprs = D_iw_op == 56;
assign D_op_flushd = D_iw_op == 59;
assign D_op_xorhi = D_iw_op == 60;
assign D_op_rsv02 = D_iw_op == 2;
assign D_op_rsv09 = D_iw_op == 9;
assign D_op_rsv10 = D_iw_op == 10;
assign D_op_rsv17 = D_iw_op == 17;
assign D_op_rsv18 = D_iw_op == 18;
assign D_op_rsv25 = D_iw_op == 25;
assign D_op_rsv26 = D_iw_op == 26;
assign D_op_rsv33 = D_iw_op == 33;
assign D_op_rsv34 = D_iw_op == 34;
assign D_op_rsv41 = D_iw_op == 41;
assign D_op_rsv42 = D_iw_op == 42;
assign D_op_rsv49 = D_iw_op == 49;
assign D_op_rsv57 = D_iw_op == 57;
assign D_op_rsv61 = D_iw_op == 61;
assign D_op_rsv62 = D_iw_op == 62;
assign D_op_rsv63 = D_iw_op == 63;
assign D_op_eret = D_op_opx & (D_iw_opx == 1);
assign D_op_roli = D_op_opx & (D_iw_opx == 2);
assign D_op_rol = D_op_opx & (D_iw_opx == 3);
assign D_op_flushp = D_op_opx & (D_iw_opx == 4);
assign D_op_ret = D_op_opx & (D_iw_opx == 5);
assign D_op_nor = D_op_opx & (D_iw_opx == 6);
assign D_op_mulxuu = D_op_opx & (D_iw_opx == 7);
assign D_op_cmpge = D_op_opx & (D_iw_opx == 8);
assign D_op_bret = D_op_opx & (D_iw_opx == 9);
assign D_op_ror = D_op_opx & (D_iw_opx == 11);
assign D_op_flushi = D_op_opx & (D_iw_opx == 12);
assign D_op_jmp = D_op_opx & (D_iw_opx == 13);
assign D_op_and = D_op_opx & (D_iw_opx == 14);
assign D_op_cmplt = D_op_opx & (D_iw_opx == 16);
assign D_op_slli = D_op_opx & (D_iw_opx == 18);
assign D_op_sll = D_op_opx & (D_iw_opx == 19);
assign D_op_wrprs = D_op_opx & (D_iw_opx == 20);
assign D_op_or = D_op_opx & (D_iw_opx == 22);
```

```
assign D_op_mulxsu = D_op_opx & (D_iw_opx == 23);
assign D_op_cmpne = D_op_opx & (D_iw_opx == 24);
assign D_op_srli = D_op_opx & (D_iw_opx == 26);
assign D_op_srl = D_op_opx & (D_iw_opx == 27);
assign D_op_nextpc = D_op_opx & (D_iw_opx == 28);
assign D_op_callr = D_op_opx & (D_iw_opx == 29);
assign D_op_xor = D_op_opx & (D_iw_opx == 30);
assign D_op_mulxss = D_op_opx & (D_iw_opx == 31);
assign D_op_cmpeq = D_op_opx & (D_iw_opx == 32);
assign D_op_divu = D_op_opx & (D_iw_opx == 36);
assign D_op_div = D_op_opx & (D_iw_opx == 37);
assign D_op_rdctl = D_op_opx & (D_iw_opx == 38);
assign D_op_mul = D_op_opx & (D_iw_opx == 39);
assign D_op_cmpgeu = D_op_opx & (D_iw_opx == 40);
assign D_op_initi = D_op_opx & (D_iw_opx == 41);
assign D_op_trap = D_op_opx & (D_iw_opx == 45);
assign D_op_wrctl = D_op_opx & (D_iw_opx == 46);
assign D_op_cmpltu = D_op_opx & (D_iw_opx == 48);
assign D_op_add = D_op_opx & (D_iw_opx == 49);
assign D_op_break = D_op_opx & (D_iw_opx == 52);
assign D_op_hbreak = D_op_opx & (D_iw_opx == 53);
assign D_op_sync = D_op_opx & (D_iw_opx == 54);
assign D_op_sub = D_op_opx & (D_iw_opx == 57);
assign D_op_srai = D_op_opx & (D_iw_opx == 58);
assign D_op_sra = D_op_opx & (D_iw_opx == 59);
assign D_op_intr = D_op_opx & (D_iw_opx == 61);
assign D_op_crst = D_op_opx & (D_iw_opx == 62);
assign D_op_rsvx00 = D_op_opx & (D_iw_opx == 0);
assign D_op_rsvx10 = D_op_opx & (D_iw_opx == 10);
assign D_op_rsvx15 = D_op_opx & (D_iw_opx == 15);
assign D_op_rsvx17 = D_op_opx & (D_iw_opx == 17);
assign D_op_rsvx21 = D_op_opx & (D_iw_opx == 21);
assign D_op_rsvx25 = D_op_opx & (D_iw_opx == 25);
assign D_op_rsvx33 = D_op_opx & (D_iw_opx == 33);
assign D_op_rsvx34 = D_op_opx & (D_iw_opx == 34);
assign D_op_rsvx35 = D_op_opx & (D_iw_opx == 35);
assign D_op_rsvx42 = D_op_opx & (D_iw_opx == 42);
assign D_op_rsvx43 = D_op_opx & (D_iw_opx == 43);
assign D_op_rsvx44 = D_op_opx & (D_iw_opx == 44);
assign D_op_rsvx47 = D_op_opx & (D_iw_opx == 47);
assign D_op_rsvx50 = D_op_opx & (D_iw_opx == 50);
assign D_op_rsvx51 = D_op_opx & (D_iw_opx == 51);
assign D_op_rsvx55 = D_op_opx & (D_iw_opx == 55);
assign D_op_rsvx56 = D_op_opx & (D_iw_opx == 56);
assign D_op_rsvx60 = D_op_opx & (D_iw_opx == 60);
assign D_op_rsvx63 = D_op_opx & (D_iw_opx == 63);
assign D_op_opx = D_iw_op == 58;
assign D_op_custom = D_iw_op == 50;
assign R_en = 1'b1;
assign E_ci_result = 0;
assign E_ci_multi_stall = 1'b0;
assign iactive = d_irq[31 : 0] & 32'b00000000000000000000000000000111;
assign F_pc_sel_nxt = R_ctrl_exception                                  ? 2'b00 :
   R_ctrl_break                                 ? 2'b01 :
   (W_br_taken | R_ctrl_uncond_cti_non_br)      ? 2'b10 :
   2'b11;

assign F_pc_no_crst_nxt = (F_pc_sel_nxt == 2'b00)? 2097160 :
```

```
      (F_pc_sel_nxt == 2'b01)? 4194824 :
      (F_pc_sel_nxt == 2'b10)? E_arith_result[24 : 2] :
      F_pc_plus_one;

   assign F_pc_nxt = F_pc_no_crst_nxt;
   assign F_pcb_nxt = {F_pc_nxt, 2'b00};
   assign F_pc_en = W_valid;
   assign F_pc_plus_one = F_pc + 1;
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               F_pc <= 2097152;
         else if (F_pc_en)
               F_pc <= F_pc_nxt;
      end


   assign F_pcb = {F_pc, 2'b00};
   assign F_pcb_plus_four = {F_pc_plus_one, 2'b00};
   assign F_valid = i_read & ~i_waitrequest;
   assign i_read_nxt = W_valid | (i_read & i_waitrequest);
   assign i_address = {F_pc, 2'b00};
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               i_read <= 1'b1;
         else
            i_read <= i_read_nxt;
      end


   assign oci_tb_hbreak_req = oci_hbreak_req;
   assign hbreak_req = (oci_tb_hbreak_req | hbreak_pending) & hbreak_enabled &
~(wait_for_one_post_bret_inst & ~W_valid);
   assign hbreak_pending_nxt = hbreak_pending ? hbreak_enabled
      : hbreak_req;

   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               wait_for_one_post_bret_inst <= 1'b0;
         else
            wait_for_one_post_bret_inst <= (~hbreak_enabled & oci_single_step_mode) ? 1'b1    :
(F_valid | ~oci_single_step_mode) ? 1'b0    : wait_for_one_post_bret_inst;
      end


   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               hbreak_pending <= 1'b0;
         else
            hbreak_pending <= hbreak_pending_nxt;
      end


   assign intr_req = W_status_reg_pie & (W_ipending_reg != 0);
   assign F_av_iw = i_readdata;
```

```
assign F_iw = hbreak_req          ? 4040762 :
   1'b0      ? 127034 :
   intr_req             ? 3926074 :
   F_av_iw;

always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            D_iw <= 0;
      else if (F_valid)
            D_iw <= F_iw;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            D_valid <= 0;
      else
         D_valid <= F_valid;
   end


assign D_dst_regnum = D_ctrl_implicit_dst_retaddr        ? 5'd31 :
   D_ctrl_implicit_dst_eretaddr      ? 5'd29 :
   D_ctrl_b_is_dst                          ? D_iw_b :
   D_iw_c;

assign D_wr_dst_reg = (D_dst_regnum != 0) & ~D_ctrl_ignore_dst;
assign D_logic_op_raw = D_op_opx ? D_iw_opx[4 : 3] :
   D_iw_op[4 : 3];

assign D_logic_op = D_ctrl_alu_force_xor ? 2'b11 : D_logic_op_raw;
assign D_compare_op = D_op_opx ? D_iw_opx[4 : 3] :
   D_iw_op[4 : 3];

assign D_jmp_direct_target_waddr = D_iw[31 : 6];
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_valid <= 0;
      else
         R_valid <= D_valid;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_wr_dst_reg <= 0;
      else
         R_wr_dst_reg <= D_wr_dst_reg;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
```

```
            R_dst_regnum <= 0;
        else
            R_dst_regnum <= D_dst_regnum;
    end


  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            R_logic_op <= 0;
      else
        R_logic_op <= D_logic_op;
    end


  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            R_compare_op <= 0;
      else
        R_compare_op <= D_compare_op;
    end


  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            R_src2_use_imm <= 0;
      else
        R_src2_use_imm <= D_ctrl_src2_choose_imm | (D_ctrl_br & R_valid);
    end


  assign W_rf_wren = (R_wr_dst_reg & W_valid) | ~reset_n;
  assign W_rf_wr_data = R_ctrl_ld ? av_ld_data_aligned_filtered : W_wr_data;
//cpu_0_register_bank_a, which is an nios_sdp_ram
cpu_0_register_bank_a_module cpu_0_register_bank_a
  (
    .clock      (clk),
    .data       (W_rf_wr_data),
    .q          (R_rf_a),
    .rdaddress (D_iw_a),
    .wraddress (R_dst_regnum),
    .wren       (W_rf_wren)
  );

//synthesis translate_off
`ifdef NO_PLI
defparam cpu_0_register_bank_a.lpm_file = "cpu_0_rf_ram_a.dat";
`else
defparam cpu_0_register_bank_a.lpm_file = "cpu_0_rf_ram_a.hex";
`endif
//synthesis translate_on
//synthesis read_comments_as_HDL on
//defparam cpu_0_register_bank_a.lpm_file = "cpu_0_rf_ram_a.mif";
//synthesis read_comments_as_HDL off
//cpu_0_register_bank_b, which is an nios_sdp_ram
cpu_0_register_bank_b_module cpu_0_register_bank_b
```

```
   (
      .clock         (clk),
      .data          (W_rf_wr_data),
      .q             (R_rf_b),
      .rdaddress (D_iw_b),
      .wraddress (R_dst_regnum),
      .wren          (W_rf_wren)
   );

//synthesis translate_off
`ifdef NO_PLI
defparam cpu_0_register_bank_b.lpm_file = "cpu_0_rf_ram_b.dat";
`else
defparam cpu_0_register_bank_b.lpm_file = "cpu_0_rf_ram_b.hex";
`endif
//synthesis translate_on
//synthesis read_comments_as_HDL on
//defparam cpu_0_register_bank_b.lpm_file = "cpu_0_rf_ram_b.mif";
//synthesis read_comments_as_HDL off
   assign R_src1 = (((R_ctrl_br & E_valid) | (R_ctrl_retaddr & R_valid)))? {F_pc_plus_one, 2'b00} :
      ((R_ctrl_jmp_direct & E_valid))? {D_jmp_direct_target_waddr, 2'b00} :
      R_rf_a;

   assign R_src2_lo = ((R_ctrl_force_src2_zero|R_ctrl_hi_imm16))? 16'b0 :
      (R_src2_use_imm)? D_iw_imm16 :
      R_rf_b[15 : 0];

   assign R_src2_hi = ((R_ctrl_force_src2_zero|R_ctrl_unsigned_lo_imm16))? 16'b0 :
      (R_ctrl_hi_imm16)? D_iw_imm16 :
      (R_src2_use_imm)? {16 {D_iw_imm16[15]}} :
      R_rf_b[31 : 16];

   assign R_src2 = {R_src2_hi, R_src2_lo};
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               E_valid <= 0;
         else
            E_valid <= R_valid | E_stall;
      end


   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               E_new_inst <= 0;
         else
            E_new_inst <= R_valid;
      end


   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               E_src1 <= 0;
         else
            E_src1 <= R_src1;
      end
```

```
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            E_src2 <= 0;
      else
         E_src2 <= R_src2;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            E_invert_arith_src_msb <= 0;
      else
         E_invert_arith_src_msb <= D_ctrl_alu_signed_comparison & R_valid;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            E_alu_sub <= 0;
      else
         E_alu_sub <= D_ctrl_alu_subtract & R_valid;
   end


assign E_stall = E_shift_rot_stall | E_ld_stall | E_st_stall | E_ci_multi_stall;
assign E_arith_src1 = { E_src1[31] ^ E_invert_arith_src_msb,
   E_src1[30 : 0]};

assign E_arith_src2 = { E_src2[31] ^ E_invert_arith_src_msb,
   E_src2[30 : 0]};

assign E_arith_result = E_alu_sub ?
   E_arith_src1 - E_arith_src2 :
   E_arith_src1 + E_arith_src2;

assign E_mem_baddr = E_arith_result[24 : 0];
assign E_logic_result = (R_logic_op == 2'b00)? (~(E_src1 | E_src2)) :
   (R_logic_op == 2'b01)? (E_src1 & E_src2) :
   (R_logic_op == 2'b10)? (E_src1 | E_src2) :
   (E_src1 ^ E_src2);

assign E_logic_result_is_0 = E_logic_result == 0;
assign E_eq = E_logic_result_is_0;
assign E_lt = E_arith_result[32];
assign E_cmp_result = (R_compare_op == 2'b00)? E_eq :
   (R_compare_op == 2'b01)? ~E_lt :
   (R_compare_op == 2'b10)? E_lt :
   ~E_eq;

assign E_shift_rot_cnt_nxt = E_new_inst ? E_src2[4 : 0] : E_shift_rot_cnt-1;
assign E_shift_rot_done = (E_shift_rot_cnt == 0) & ~E_new_inst;
assign E_shift_rot_stall = R_ctrl_shift_rot & E_valid & ~E_shift_rot_done;
assign E_shift_rot_fill_bit = R_ctrl_shift_logical ? 1'b0 :
```

```
    (R_ctrl_rot_right ? E_shift_rot_result[0] :
    E_shift_rot_result[31]);

assign E_shift_rot_result_nxt = (E_new_inst)? E_src1 :
    (R_ctrl_shift_rot_right)? {E_shift_rot_fill_bit, E_shift_rot_result[31 : 1]} :
    {E_shift_rot_result[30 : 0], E_shift_rot_fill_bit};

always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            E_shift_rot_result <= 0;
      else
         E_shift_rot_result <= E_shift_rot_result_nxt;
    end


always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            E_shift_rot_cnt <= 0;
      else
         E_shift_rot_cnt <= E_shift_rot_cnt_nxt;
    end


assign E_control_rd_data = (D_iw_control_regnum == 3'd0)? W_status_reg :
    (D_iw_control_regnum == 3'd1)? W_estatus_reg :
    (D_iw_control_regnum == 3'd2)? W_bstatus_reg :
    (D_iw_control_regnum == 3'd3)? W_ienable_reg :
    (D_iw_control_regnum == 3'd4)? W_ipending_reg :
    0;

assign E_alu_result = ((R_ctrl_br_cmp | R_ctrl_rdctl_inst))? 0 :
    (R_ctrl_shift_rot)? E_shift_rot_result :
    (R_ctrl_logic)? E_logic_result :
    (R_ctrl_custom)? E_ci_result :
    E_arith_result;

assign R_stb_data = R_rf_b[7 : 0];
assign R_sth_data = R_rf_b[15 : 0];
assign E_st_data = (D_mem8)? {R_stb_data, R_stb_data, R_stb_data, R_stb_data} :
    (D_mem16)? {R_sth_data, R_sth_data} :
    R_rf_b;

assign E_mem_byte_en = ({D_iw_memsz, E_mem_baddr[1 : 0]} == {2'b00, 2'b00})? 4'b0001 :
    ({D_iw_memsz, E_mem_baddr[1 : 0]} == {2'b00, 2'b01})? 4'b0010 :
    ({D_iw_memsz, E_mem_baddr[1 : 0]} == {2'b00, 2'b10})? 4'b0100 :
    ({D_iw_memsz, E_mem_baddr[1 : 0]} == {2'b00, 2'b11})? 4'b1000 :
    ({D_iw_memsz, E_mem_baddr[1 : 0]} == {2'b01, 2'b00})? 4'b0011 :
    ({D_iw_memsz, E_mem_baddr[1 : 0]} == {2'b01, 2'b01})? 4'b0011 :
    ({D_iw_memsz, E_mem_baddr[1 : 0]} == {2'b01, 2'b10})? 4'b1100 :
    ({D_iw_memsz, E_mem_baddr[1 : 0]} == {2'b01, 2'b11})? 4'b1100 :
    4'b1111;

assign d_read_nxt = (R_ctrl_ld & E_new_inst) | (d_read & d_waitrequest);
assign E_ld_stall = R_ctrl_ld & ((E_valid & ~av_ld_done) | E_new_inst);
assign d_write_nxt = (R_ctrl_st & E_new_inst) | (d_write & d_waitrequest);
assign E_st_stall = d_write_nxt;
```

```
assign d_address = W_mem_baddr;
assign av_ld_getting_data = d_read & ~d_waitrequest;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            d_read <= 0;
      else
         d_read <= d_read_nxt;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            d_writedata <= 0;
      else
         d_writedata <= E_st_data;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            d_byteenable <= 0;
      else
         d_byteenable <= E_mem_byte_en;
   end


assign av_ld_align_cycle_nxt = av_ld_getting_data ? 0 : (av_ld_align_cycle+1);
assign av_ld_align_one_more_cycle = av_ld_align_cycle == (D_mem16 ? 2 : 3);
assign av_ld_aligning_data_nxt = av_ld_aligning_data ?
   ~av_ld_align_one_more_cycle :
   (~D_mem32 & av_ld_getting_data);

assign av_ld_waiting_for_data_nxt = av_ld_waiting_for_data ?
   ~av_ld_getting_data :
   (R_ctrl_ld & E_new_inst);

assign av_ld_done = ~av_ld_waiting_for_data_nxt & (D_mem32 | ~av_ld_aligning_data_nxt);
assign av_ld_rshift8 = av_ld_aligning_data &
   (av_ld_align_cycle < (W_mem_baddr[1 : 0]));

assign av_ld_extend = av_ld_aligning_data;
assign av_ld_byte0_data_nxt = av_ld_rshift8          ? av_ld_byte1_data :
   av_ld_extend          ? av_ld_byte0_data :
   d_readdata[7 : 0];

assign av_ld_byte1_data_nxt = av_ld_rshift8          ? av_ld_byte2_data :
   av_ld_extend          ? {8 {av_fill_bit}} :
   d_readdata[15 : 8];

assign av_ld_byte2_data_nxt = av_ld_rshift8          ? av_ld_byte3_data :
   av_ld_extend          ? {8 {av_fill_bit}} :
   d_readdata[23 : 16];

assign av_ld_byte3_data_nxt = av_ld_rshift8          ? av_ld_byte3_data :
   av_ld_extend          ? {8 {av_fill_bit}} :
```

```
   d_readdata[31 : 24];

assign av_ld_byte1_data_en = ~(av_ld_extend & D_mem16 & ~av_ld_rshift8);
assign av_ld_data_aligned_unfiltered = {av_ld_byte3_data, av_ld_byte2_data,
   av_ld_byte1_data, av_ld_byte0_data};

assign av_sign_bit = D_mem16 ? av_ld_byte1_data[7] : av_ld_byte0_data[7];
assign av_fill_bit = av_sign_bit & R_ctrl_ld_signed;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            av_ld_align_cycle <= 0;
      else
         av_ld_align_cycle <= av_ld_align_cycle_nxt;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            av_ld_waiting_for_data <= 0;
      else
         av_ld_waiting_for_data <= av_ld_waiting_for_data_nxt;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            av_ld_aligning_data <= 0;
      else
         av_ld_aligning_data <= av_ld_aligning_data_nxt;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            av_ld_byte0_data <= 0;
      else
         av_ld_byte0_data <= av_ld_byte0_data_nxt;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            av_ld_byte1_data <= 0;
      else if (av_ld_byte1_data_en)
            av_ld_byte1_data <= av_ld_byte1_data_nxt;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            av_ld_byte2_data <= 0;
      else
```

```
        av_ld_byte2_data <= av_ld_byte2_data_nxt;
    end


always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            av_ld_byte3_data <= 0;
        else
            av_ld_byte3_data <= av_ld_byte3_data_nxt;
    end


always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            W_valid <= 0;
        else
            W_valid <= E_valid & ~E_stall;
    end


always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            W_control_rd_data <= 0;
        else
            W_control_rd_data <= E_control_rd_data;
    end


always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            W_cmp_result <= 0;
        else
            W_cmp_result <= E_cmp_result;
    end


always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            W_alu_result <= 0;
        else
            W_alu_result <= E_alu_result;
    end


always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            W_status_reg_pie <= 0;
        else
            W_status_reg_pie <= W_status_reg_pie_nxt;
    end
```

```
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            W_estatus_reg <= 0;
      else
         W_estatus_reg <= W_estatus_reg_nxt;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            W_bstatus_reg <= 0;
      else
         W_bstatus_reg <= W_bstatus_reg_nxt;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            W_ienable_reg <= 0;
      else
         W_ienable_reg <= W_ienable_reg_nxt;
   end


always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            W_ipending_reg <= 0;
      else
         W_ipending_reg <= W_ipending_reg_nxt;
   end


assign W_wr_data_non_zero = R_ctrl_br_cmp ? W_cmp_result :
   R_ctrl_rdctl_inst          ? W_control_rd_data :
   W_alu_result[31 : 0];

assign W_wr_data = W_wr_data_non_zero;
assign W_br_taken = R_ctrl_br & W_cmp_result;
assign W_mem_baddr = W_alu_result[24 : 0];
assign W_status_reg = W_status_reg_pie;
assign E_wrctl_status = R_ctrl_wrctl_inst &
   (D_iw_control_regnum == 3'd0);

assign E_wrctl_estatus = R_ctrl_wrctl_inst &
   (D_iw_control_regnum == 3'd1);

assign E_wrctl_bstatus = R_ctrl_wrctl_inst &
   (D_iw_control_regnum == 3'd2);

assign E_wrctl_ienable = R_ctrl_wrctl_inst &
   (D_iw_control_regnum == 3'd3);

assign W_status_reg_pie_inst_nxt = (R_ctrl_exception | R_ctrl_break | R_ctrl_crst) ? 1'b0 :
   (D_op_eret)                          ? W_estatus_reg :
```

```
      (D_op_bret)                              ? W_bstatus_reg :
      (E_wrctl_status)                         ? E_src1[0] :
      W_status_reg_pie;

   assign W_status_reg_pie_nxt = E_valid ? W_status_reg_pie_inst_nxt : W_status_reg_pie;
   assign W_estatus_reg_inst_nxt = (R_ctrl_crst)              ? 0 :
      (R_ctrl_exception)      ? W_status_reg :
      (E_wrctl_estatus)       ? E_src1[0] :
      W_estatus_reg;

   assign W_estatus_reg_nxt = E_valid ? W_estatus_reg_inst_nxt : W_estatus_reg;
   assign W_bstatus_reg_inst_nxt = (R_ctrl_break)             ? W_status_reg :
      (E_wrctl_bstatus)       ? E_src1[0] :
      W_bstatus_reg;

   assign W_bstatus_reg_nxt = E_valid ? W_bstatus_reg_inst_nxt : W_bstatus_reg;
   assign W_ienable_reg_nxt = ((E_wrctl_ienable & E_valid) ?
      E_src1[31 : 0] : W_ienable_reg) & 32'b00000000000000000000000000000111;

   assign W_ipending_reg_nxt = iactive & W_ienable_reg & oci_ienable &
32'b00000000000000000000000000000111;
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               hbreak_enabled <= 1'b1;
         else if (E_valid)
               hbreak_enabled <= R_ctrl_break ? 1'b0 : D_op_bret ? 1'b1 : hbreak_enabled;
      end


   cpu_0_nios2_oci the_cpu_0_nios2_oci
      (
         .D_valid                                (D_valid),
         .E_st_data                              (E_st_data),
         .E_valid                                (E_valid),
         .F_pc                                   (F_pc),
         .address                                (jtag_debug_module_address),
         .av_ld_data_aligned_filtered            (av_ld_data_aligned_filtered),
         .begintransfer                          (jtag_debug_module_begintransfer),
         .byteenable                             (jtag_debug_module_byteenable),
         .chipselect                             (jtag_debug_module_select),
         .clk                                    (jtag_debug_module_clk),
         .d_address                              (d_address),
         .d_read                                 (d_read),
         .d_waitrequest                          (d_waitrequest),
         .d_write                                (d_write),
         .debugaccess                            (jtag_debug_module_debugaccess),
         .hbreak_enabled                         (hbreak_enabled),
         .jtag_debug_module_debugaccess_to_roms
(jtag_debug_module_debugaccess_to_roms),
         .oci_hbreak_req                         (oci_hbreak_req),
         .oci_ienable                            (oci_ienable),
         .oci_single_step_mode                   (oci_single_step_mode),
         .readdata                               (jtag_debug_module_readdata),
         .reset                                  (jtag_debug_module_reset),
         .reset_n                                (reset_n),
         .resetrequest                           (jtag_debug_module_resetrequest),
         .test_ending                            (test_ending),
```

```
      .test_has_ended                       (test_has_ended),
      .write                                (jtag_debug_module_write),
      .writedata                            (jtag_debug_module_writedata)
   );

//jtag_debug_module, which is an e_avalon_slave
assign jtag_debug_module_clk = clk;
assign jtag_debug_module_reset = ~reset_n;
assign D_ctrl_custom = 1'b0;
assign R_ctrl_custom_nxt = D_ctrl_custom;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_custom <= 0;
      else if (R_en)
            R_ctrl_custom <= R_ctrl_custom_nxt;
   end


assign D_ctrl_custom_multi = 1'b0;
assign R_ctrl_custom_multi_nxt = D_ctrl_custom_multi;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_custom_multi <= 0;
      else if (R_en)
            R_ctrl_custom_multi <= R_ctrl_custom_multi_nxt;
   end


assign D_ctrl_jmp_indirect = D_op_eret|
   D_op_bret|
   D_op_rsvx17|
   D_op_rsvx25|
   D_op_ret|
   D_op_jmp|
   D_op_rsvx21|
   D_op_callr;

assign R_ctrl_jmp_indirect_nxt = D_ctrl_jmp_indirect;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_jmp_indirect <= 0;
      else if (R_en)
            R_ctrl_jmp_indirect <= R_ctrl_jmp_indirect_nxt;
   end


assign D_ctrl_jmp_direct = D_op_call|D_op_jmpi;
assign R_ctrl_jmp_direct_nxt = D_ctrl_jmp_direct;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_jmp_direct <= 0;
      else if (R_en)
            R_ctrl_jmp_direct <= R_ctrl_jmp_direct_nxt;
   end
```

```
  assign D_ctrl_implicit_dst_retaddr = D_op_call|D_op_rsv02;
  assign R_ctrl_implicit_dst_retaddr_nxt = D_ctrl_implicit_dst_retaddr;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          R_ctrl_implicit_dst_retaddr <= 0;
      else if (R_en)
          R_ctrl_implicit_dst_retaddr <= R_ctrl_implicit_dst_retaddr_nxt;
    end


  assign                                D_ctrl_implicit_dst_eretaddr                                =
D_op_div|D_op_divu|D_op_mul|D_op_muli|D_op_mulxss|D_op_mulxsu|D_op_mulxuu;
  assign R_ctrl_implicit_dst_eretaddr_nxt = D_ctrl_implicit_dst_eretaddr;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          R_ctrl_implicit_dst_eretaddr <= 0;
      else if (R_en)
          R_ctrl_implicit_dst_eretaddr <= R_ctrl_implicit_dst_eretaddr_nxt;
    end


  assign D_ctrl_exception = D_op_trap|
    D_op_rsvx44|
    D_op_div|
    D_op_divu|
    D_op_mul|
    D_op_muli|
    D_op_mulxss|
    D_op_mulxsu|
    D_op_mulxuu|
    D_op_intr|
    D_op_rsvx60;

  assign R_ctrl_exception_nxt = D_ctrl_exception;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          R_ctrl_exception <= 0;
      else if (R_en)
          R_ctrl_exception <= R_ctrl_exception_nxt;
    end


  assign D_ctrl_break = D_op_break|D_op_hbreak;
  assign R_ctrl_break_nxt = D_ctrl_break;
  always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
          R_ctrl_break <= 0;
      else if (R_en)
          R_ctrl_break <= R_ctrl_break_nxt;
    end
```

```
assign D_ctrl_crst = D_op_crst|D_op_rsvx63;
assign R_ctrl_crst_nxt = D_ctrl_crst;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_crst <= 0;
      else if (R_en)
            R_ctrl_crst <= R_ctrl_crst_nxt;
   end


assign D_ctrl_uncond_cti_non_br = D_op_call|
   D_op_jmpi|
   D_op_eret|
   D_op_bret|
   D_op_rsvx17|
   D_op_rsvx25|
   D_op_ret|
   D_op_jmp|
   D_op_rsvx21|
   D_op_callr;

assign R_ctrl_uncond_cti_non_br_nxt = D_ctrl_uncond_cti_non_br;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_uncond_cti_non_br <= 0;
      else if (R_en)
            R_ctrl_uncond_cti_non_br <= R_ctrl_uncond_cti_non_br_nxt;
   end


assign D_ctrl_retaddr = D_op_call|
   D_op_rsv02|
   D_op_nextpc|
   D_op_callr|
   D_op_trap|
   D_op_rsvx44|
   D_op_div|
   D_op_divu|
   D_op_mul|
   D_op_muli|
   D_op_mulxss|
   D_op_mulxsu|
   D_op_mulxuu|
   D_op_intr|
   D_op_rsvx60|
   D_op_break|
   D_op_hbreak;

assign R_ctrl_retaddr_nxt = D_ctrl_retaddr;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_retaddr <= 0;
      else if (R_en)
            R_ctrl_retaddr <= R_ctrl_retaddr_nxt;
   end
```

```
assign D_ctrl_shift_logical = D_op_slli|D_op_sll|D_op_srli|D_op_srl;
assign R_ctrl_shift_logical_nxt = D_ctrl_shift_logical;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_shift_logical <= 0;
      else if (R_en)
            R_ctrl_shift_logical <= R_ctrl_shift_logical_nxt;
   end


assign D_ctrl_shift_right_arith = D_op_srai|D_op_sra;
assign R_ctrl_shift_right_arith_nxt = D_ctrl_shift_right_arith;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_shift_right_arith <= 0;
      else if (R_en)
            R_ctrl_shift_right_arith <= R_ctrl_shift_right_arith_nxt;
   end


assign D_ctrl_rot_right = D_op_rsvx10|D_op_ror|D_op_rsvx42|D_op_rsvx43;
assign R_ctrl_rot_right_nxt = D_ctrl_rot_right;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_rot_right <= 0;
      else if (R_en)
            R_ctrl_rot_right <= R_ctrl_rot_right_nxt;
   end


assign D_ctrl_shift_rot_right = D_op_srli|
   D_op_srl|
   D_op_srai|
   D_op_sra|
   D_op_rsvx10|
   D_op_ror|
   D_op_rsvx42|
   D_op_rsvx43;

assign R_ctrl_shift_rot_right_nxt = D_ctrl_shift_rot_right;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_shift_rot_right <= 0;
      else if (R_en)
            R_ctrl_shift_rot_right <= R_ctrl_shift_rot_right_nxt;
   end


assign D_ctrl_shift_rot = D_op_slli|
   D_op_rsvx50|
   D_op_sll|
   D_op_rsvx51|
```

```
    D_op_roli|
    D_op_rsvx34|
    D_op_rol|
    D_op_rsvx35|
    D_op_srli|
    D_op_srl|
    D_op_srai|
    D_op_sra|
    D_op_rsvx10|
    D_op_ror|
    D_op_rsvx42|
    D_op_rsvx43;

assign R_ctrl_shift_rot_nxt = D_ctrl_shift_rot;
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            R_ctrl_shift_rot <= 0;
        else if (R_en)
            R_ctrl_shift_rot <= R_ctrl_shift_rot_nxt;
    end


assign D_ctrl_logic = D_op_and|
    D_op_or|
    D_op_xor|
    D_op_nor|
    D_op_andhi|
    D_op_orhi|
    D_op_xorhi|
    D_op_andi|
    D_op_ori|
    D_op_xori;

assign R_ctrl_logic_nxt = D_ctrl_logic;
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            R_ctrl_logic <= 0;
        else if (R_en)
            R_ctrl_logic <= R_ctrl_logic_nxt;
    end


assign D_ctrl_hi_imm16 = D_op_andhi|D_op_orhi|D_op_xorhi;
assign R_ctrl_hi_imm16_nxt = D_ctrl_hi_imm16;
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
            R_ctrl_hi_imm16 <= 0;
        else if (R_en)
            R_ctrl_hi_imm16 <= R_ctrl_hi_imm16_nxt;
    end


assign D_ctrl_unsigned_lo_imm16 = D_op_cmpgeui|
    D_op_cmpltui|
    D_op_andi|
```

```
    D_op_ori|
    D_op_xori|
    D_op_roli|
    D_op_rsvx10|
    D_op_slli|
    D_op_srli|
    D_op_rsvx34|
    D_op_rsvx42|
    D_op_rsvx50|
    D_op_srai;

assign R_ctrl_unsigned_lo_imm16_nxt = D_ctrl_unsigned_lo_imm16;
always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            R_ctrl_unsigned_lo_imm16 <= 0;
      else if (R_en)
            R_ctrl_unsigned_lo_imm16 <= R_ctrl_unsigned_lo_imm16_nxt;
    end


assign D_ctrl_br_uncond = D_op_br|D_op_rsv02;
assign R_ctrl_br_uncond_nxt = D_ctrl_br_uncond;
always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            R_ctrl_br_uncond <= 0;
      else if (R_en)
            R_ctrl_br_uncond <= R_ctrl_br_uncond_nxt;
    end


assign D_ctrl_br = D_op_br|
    D_op_bge|
    D_op_blt|
    D_op_bne|
    D_op_beq|
    D_op_bgeu|
    D_op_bltu|
    D_op_rsv62;

assign R_ctrl_br_nxt = D_ctrl_br;
always @(posedge clk or negedge reset_n)
    begin
      if (reset_n == 0)
            R_ctrl_br <= 0;
      else if (R_en)
            R_ctrl_br <= R_ctrl_br_nxt;
    end


assign D_ctrl_alu_subtract = D_op_sub|
    D_op_rsvx25|
    D_op_cmplti|
    D_op_cmpltui|
    D_op_cmplt|
    D_op_cmpltu|
    D_op_blt|
```

```
      D_op_bltu|
      D_op_cmpgei|
      D_op_cmpgeui|
      D_op_cmpge|
      D_op_cmpgeu|
      D_op_bge|
      D_op_rsv10|
      D_op_bgeu|
      D_op_rsv42;

   assign R_ctrl_alu_subtract_nxt = D_ctrl_alu_subtract;
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               R_ctrl_alu_subtract <= 0;
         else if (R_en)
               R_ctrl_alu_subtract <= R_ctrl_alu_subtract_nxt;
      end


   assign                                D_ctrl_alu_signed_comparison                                =
D_op_cmpge|D_op_cmpgei|D_op_cmplt|D_op_cmplti|D_op_bge|D_op_blt;
   assign R_ctrl_alu_signed_comparison_nxt = D_ctrl_alu_signed_comparison;
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               R_ctrl_alu_signed_comparison <= 0;
         else if (R_en)
               R_ctrl_alu_signed_comparison <= R_ctrl_alu_signed_comparison_nxt;
      end


   assign D_ctrl_br_cmp = D_op_br|
      D_op_bge|
      D_op_blt|
      D_op_bne|
      D_op_beq|
      D_op_bgeu|
      D_op_bltu|
      D_op_rsv62|
      D_op_cmpgei|
      D_op_cmplti|
      D_op_cmpnei|
      D_op_cmpgeui|
      D_op_cmpltui|
      D_op_cmpeqi|
      D_op_rsvx00|
      D_op_cmpge|
      D_op_cmplt|
      D_op_cmpne|
      D_op_cmpgeu|
      D_op_cmpltu|
      D_op_cmpeq|
      D_op_rsvx56;

   assign R_ctrl_br_cmp_nxt = D_ctrl_br_cmp;
   always @(posedge clk or negedge reset_n)
      begin
```

```
    if (reset_n == 0)
        R_ctrl_br_cmp <= 0;
    else if (R_en)
        R_ctrl_br_cmp <= R_ctrl_br_cmp_nxt;
  end


assign D_ctrl_ld_signed = D_op_ldb|
  D_op_ldh|
  D_op_ldl|
  D_op_ldw|
  D_op_ldbio|
  D_op_ldhio|
  D_op_ldwio|
  D_op_rsv63;

assign R_ctrl_ld_signed_nxt = D_ctrl_ld_signed;
always @(posedge clk or negedge reset_n)
  begin
    if (reset_n == 0)
        R_ctrl_ld_signed <= 0;
    else if (R_en)
        R_ctrl_ld_signed <= R_ctrl_ld_signed_nxt;
  end


assign D_ctrl_ld = D_op_ldb|
  D_op_ldh|
  D_op_ldl|
  D_op_ldw|
  D_op_ldbio|
  D_op_ldhio|
  D_op_ldwio|
  D_op_rsv63|
  D_op_ldbu|
  D_op_ldhu|
  D_op_ldbuio|
  D_op_ldhuio;

assign R_ctrl_ld_nxt = D_ctrl_ld;
always @(posedge clk or negedge reset_n)
  begin
    if (reset_n == 0)
        R_ctrl_ld <= 0;
    else if (R_en)
        R_ctrl_ld <= R_ctrl_ld_nxt;
  end


assign D_ctrl_ld_non_io = D_op_ldbu|D_op_ldhu|D_op_ldb|D_op_ldh|D_op_ldw|D_op_ldl;
assign R_ctrl_ld_non_io_nxt = D_ctrl_ld_non_io;
always @(posedge clk or negedge reset_n)
  begin
    if (reset_n == 0)
        R_ctrl_ld_non_io <= 0;
    else if (R_en)
        R_ctrl_ld_non_io <= R_ctrl_ld_non_io_nxt;
  end
```

```
  assign D_ctrl_st = D_op_stb|
     D_op_sth|
     D_op_stw|
     D_op_stc|
     D_op_stbio|
     D_op_sthio|
     D_op_stwio|
     D_op_rsv61;

  assign R_ctrl_st_nxt = D_ctrl_st;
  always @(posedge clk or negedge reset_n)
     begin
        if (reset_n == 0)
              R_ctrl_st <= 0;
        else if (R_en)
              R_ctrl_st <= R_ctrl_st_nxt;
     end


  assign                                    D_ctrl_ld_io                                    =
D_op_ldbuio|D_op_ldhuio|D_op_ldbio|D_op_ldhio|D_op_ldwio|D_op_rsv63;
  assign R_ctrl_ld_io_nxt = D_ctrl_ld_io;
  always @(posedge clk or negedge reset_n)
     begin
        if (reset_n == 0)
              R_ctrl_ld_io <= 0;
        else if (R_en)
              R_ctrl_ld_io <= R_ctrl_ld_io_nxt;
     end


  assign D_ctrl_b_is_dst = D_op_addi|
     D_op_andhi|
     D_op_orhi|
     D_op_xorhi|
     D_op_andi|
     D_op_ori|
     D_op_xori|
     D_op_call|
     D_op_rdprs|
     D_op_cmpgei|
     D_op_cmplti|
     D_op_cmpnei|
     D_op_cmpgeui|
     D_op_cmpltui|
     D_op_cmpeqi|
     D_op_jmpi|
     D_op_rsv09|
     D_op_rsv17|
     D_op_rsv25|
     D_op_rsv33|
     D_op_rsv41|
     D_op_rsv49|
     D_op_rsv57|
     D_op_ldb|
     D_op_ldh|
```

```
    D_op_ldl|
    D_op_ldw|
    D_op_ldbio|
    D_op_ldhio|
    D_op_ldwio|
    D_op_rsv63|
    D_op_ldbu|
    D_op_ldhu|
    D_op_ldbuio|
    D_op_ldhuio|
    D_op_initd|
    D_op_initda|
    D_op_flushd|
    D_op_flushda;

assign R_ctrl_b_is_dst_nxt = D_ctrl_b_is_dst;
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
                R_ctrl_b_is_dst <= 0;
        else if (R_en)
                R_ctrl_b_is_dst <= R_ctrl_b_is_dst_nxt;
    end


assign D_ctrl_ignore_dst = D_op_br|
    D_op_bge|
    D_op_blt|
    D_op_bne|
    D_op_beq|
    D_op_bgeu|
    D_op_bltu|
    D_op_rsv62|
    D_op_stb|
    D_op_sth|
    D_op_stw|
    D_op_stc|
    D_op_stbio|
    D_op_sthio|
    D_op_stwio|
    D_op_rsv61|
    D_op_jmpi|
    D_op_rsv09|
    D_op_rsv17|
    D_op_rsv25|
    D_op_rsv33|
    D_op_rsv41|
    D_op_rsv49|
    D_op_rsv57;

assign R_ctrl_ignore_dst_nxt = D_ctrl_ignore_dst;
always @(posedge clk or negedge reset_n)
    begin
        if (reset_n == 0)
                R_ctrl_ignore_dst <= 0;
        else if (R_en)
                R_ctrl_ignore_dst <= R_ctrl_ignore_dst_nxt;
    end
```

```
assign D_ctrl_src2_choose_imm = D_op_addi|
    D_op_andhi|
    D_op_orhi|
    D_op_xorhi|
    D_op_andi|
    D_op_ori|
    D_op_xori|
    D_op_call|
    D_op_rdprs|
    D_op_cmpgei|
    D_op_cmplti|
    D_op_cmpnei|
    D_op_cmpgeui|
    D_op_cmpltui|
    D_op_cmpeqi|
    D_op_jmpi|
    D_op_rsv09|
    D_op_rsv17|
    D_op_rsv25|
    D_op_rsv33|
    D_op_rsv41|
    D_op_rsv49|
    D_op_rsv57|
    D_op_ldb|
    D_op_ldh|
    D_op_ldl|
    D_op_ldw|
    D_op_ldbio|
    D_op_ldhio|
    D_op_ldwio|
    D_op_rsv63|
    D_op_ldbu|
    D_op_ldhu|
    D_op_ldbuio|
    D_op_ldhuio|
    D_op_initd|
    D_op_initda|
    D_op_flushd|
    D_op_flushda|
    D_op_stb|
    D_op_sth|
    D_op_stw|
    D_op_stc|
    D_op_stbio|
    D_op_sthio|
    D_op_stwio|
    D_op_rsv61|
    D_op_roli|
    D_op_rsvx10|
    D_op_slli|
    D_op_srli|
    D_op_rsvx34|
    D_op_rsvx42|
    D_op_rsvx50|
    D_op_srai;
```

```
assign R_ctrl_src2_choose_imm_nxt = D_ctrl_src2_choose_imm;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_src2_choose_imm <= 0;
      else if (R_en)
            R_ctrl_src2_choose_imm <= R_ctrl_src2_choose_imm_nxt;
   end


assign D_ctrl_wrctl_inst = D_op_wrctl;
assign R_ctrl_wrctl_inst_nxt = D_ctrl_wrctl_inst;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_wrctl_inst <= 0;
      else if (R_en)
            R_ctrl_wrctl_inst <= R_ctrl_wrctl_inst_nxt;
   end


assign D_ctrl_rdctl_inst = D_op_rdctl;
assign R_ctrl_rdctl_inst_nxt = D_ctrl_rdctl_inst;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_rdctl_inst <= 0;
      else if (R_en)
            R_ctrl_rdctl_inst <= R_ctrl_rdctl_inst_nxt;
   end


assign D_ctrl_force_src2_zero = D_op_call|
   D_op_rsv02|
   D_op_nextpc|
   D_op_callr|
   D_op_trap|
   D_op_rsvx44|
   D_op_intr|
   D_op_rsvx60|
   D_op_break|
   D_op_hbreak|
   D_op_eret|
   D_op_bret|
   D_op_rsvx17|
   D_op_rsvx25|
   D_op_ret|
   D_op_jmp|
   D_op_rsvx21|
   D_op_jmpi;

assign R_ctrl_force_src2_zero_nxt = D_ctrl_force_src2_zero;
always @(posedge clk or negedge reset_n)
   begin
      if (reset_n == 0)
            R_ctrl_force_src2_zero <= 0;
      else if (R_en)
            R_ctrl_force_src2_zero <= R_ctrl_force_src2_zero_nxt;
```

```
      end


   assign D_ctrl_alu_force_xor = D_op_cmpgei|
      D_op_cmpgeui|
      D_op_cmpeqi|
      D_op_cmpge|
      D_op_cmpgeu|
      D_op_cmpeq|
      D_op_cmpnei|
      D_op_cmpne|
      D_op_bge|
      D_op_rsv10|
      D_op_bgeu|
      D_op_rsv42|
      D_op_beq|
      D_op_rsv34|
      D_op_bne|
      D_op_rsv62|
      D_op_br|
      D_op_rsv02;

   assign R_ctrl_alu_force_xor_nxt = D_ctrl_alu_force_xor;
   always @(posedge clk or negedge reset_n)
      begin
         if (reset_n == 0)
               R_ctrl_alu_force_xor <= 0;
         else if (R_en)
               R_ctrl_alu_force_xor <= R_ctrl_alu_force_xor_nxt;
      end


   //data_master, which is an e_avalon_master
   //instruction_master, which is an e_avalon_master

//synthesis translate_off
//////////////// SIMULATION-ONLY CONTENTS
   assign F_inst = (F_op_call)? 56'h20202063616c6c :
      (F_op_jmpi)? 56'h2020206a6d7069 :
      (F_op_ldbu)? 56'h2020206c646275 :
      (F_op_addi)? 56'h20202061646469 :
      (F_op_stb)? 56'h20202020737462 :
      (F_op_br)? 56'h20202020206272 :
      (F_op_ldb)? 56'h202020206c6462 :
      (F_op_cmpgei)? 56'h20636d70676569 :
      (F_op_ldhu)? 56'h2020206c646875 :
      (F_op_andi)? 56'h202020616e6469 :
      (F_op_sth)? 56'h20202020737468 :
      (F_op_bge)? 56'h20202020626765 :
      (F_op_ldh)? 56'h202020206c6468 :
      (F_op_cmplti)? 56'h20636d706c7469 :
      (F_op_initda)? 56'h20696e69746461 :
      (F_op_ori)? 56'h202020206f7269 :
      (F_op_stw)? 56'h20202020737477 :
      (F_op_blt)? 56'h20202020626c74 :
      (F_op_ldw)? 56'h202020206c6477 :
      (F_op_cmpnei)? 56'h20636d706e6569 :
      (F_op_flushda)? 56'h666c7573686461 :
```

(F_op_xori)? 56'h202020786f7269 :
(F_op_bne)? 56'h20202020626e65 :
(F_op_cmpeqi)? 56'h20636d70657169 :
(F_op_ldbuio)? 56'h206c646275696f :
(F_op_muli)? 56'h2020206d756c69 :
(F_op_stbio)? 56'h2020737462696f :
(F_op_beq)? 56'h20202020626571 :
(F_op_ldbio)? 56'h20206c6462696f :
(F_op_cmpgeui)? 56'h636d7067657569 :
(F_op_ldhuio)? 56'h206c646875696f :
(F_op_andhi)? 56'h2020616e646869 :
(F_op_sthio)? 56'h2020737468696f :
(F_op_bgeu)? 56'h20202062676575 :
(F_op_ldhio)? 56'h20206c6468696f :
(F_op_cmpltui)? 56'h636d706c747569 :
(F_op_initd)? 56'h2020696e697464 :
(F_op_orhi)? 56'h2020206f726869 :
(F_op_stwio)? 56'h2020737477696f :
(F_op_bltu)? 56'h202020626c7475 :
(F_op_ldwio)? 56'h20206c6477696f :
(F_op_flushd)? 56'h20666c75736864 :
(F_op_xorhi)? 56'h2020786f726869 :
(F_op_eret)? 56'h20202065726574 :
(F_op_roli)? 56'h202020726f6c69 :
(F_op_rol)? 56'h20202020726f6c :
(F_op_flushp)? 56'h20666c75736870 :
(F_op_ret)? 56'h20202020726574 :
(F_op_nor)? 56'h202020206e6f72 :
(F_op_mulxuu)? 56'h206d756c787575 :
(F_op_cmpge)? 56'h2020636d706765 :
(F_op_bret)? 56'h20202062726574 :
(F_op_ror)? 56'h20202020726f72 :
(F_op_flushi)? 56'h20666c75736869 :
(F_op_jmp)? 56'h202020206a6d70 :
(F_op_and)? 56'h20202020616e64 :
(F_op_cmplt)? 56'h2020636d706c74 :
(F_op_slli)? 56'h202020736c6c69 :
(F_op_sll)? 56'h20202020736c6c :
(F_op_or)? 56'h20202020206f72 :
(F_op_mulxsu)? 56'h206d756c787375 :
(F_op_cmpne)? 56'h2020636d706e65 :
(F_op_srli)? 56'h20202073726c69 :
(F_op_srl)? 56'h2020202073726c :
(F_op_nextpc)? 56'h206e6578747063 :
(F_op_callr)? 56'h202063616c6c72 :
(F_op_xor)? 56'h20202020786f72 :
(F_op_mulxss)? 56'h206d756c787373 :
(F_op_cmpeq)? 56'h2020636d706571 :
(F_op_divu)? 56'h20202064697675 :
(F_op_div)? 56'h20202020646976 :
(F_op_rdctl)? 56'h2020726463746c :
(F_op_mul)? 56'h202020206d756c :
(F_op_cmpgeu)? 56'h20636d70676575 :
(F_op_initi)? 56'h2020696e697469 :
(F_op_trap)? 56'h20202074726170 :
(F_op_wrctl)? 56'h2020777263746c :
(F_op_cmpltu)? 56'h20636d706c7475 :
(F_op_add)? 56'h20202020616464 :

```
    (F_op_break)? 56'h2020627265616b :
    (F_op_hbreak)? 56'h2068627265616b :
    (F_op_sync)? 56'h20202073796e63 :
    (F_op_sub)? 56'h20202020737562 :
    (F_op_srai)? 56'h20202073726169 :
    (F_op_sra)? 56'h20202020737261 :
    (F_op_intr)? 56'h202020696e7472 :
    56'h20202020424144;

assign D_inst = (D_op_call)? 56'h20202063616c6c :
    (D_op_jmpi)? 56'h2020206a6d7069 :
    (D_op_ldbu)? 56'h2020206c646275 :
    (D_op_addi)? 56'h20202061646469 :
    (D_op_stb)? 56'h20202020737462 :
    (D_op_br)? 56'h20202020206272 :
    (D_op_ldb)? 56'h202020206c6462 :
    (D_op_cmpgei)? 56'h20636d70676569 :
    (D_op_ldhu)? 56'h2020206c646875 :
    (D_op_andi)? 56'h202020616e6469 :
    (D_op_sth)? 56'h20202020737468 :
    (D_op_bge)? 56'h20202020626765 :
    (D_op_ldh)? 56'h202020206c6468 :
    (D_op_cmplti)? 56'h20636d706c7469 :
    (D_op_initda)? 56'h20696e69746461 :
    (D_op_ori)? 56'h202020206f7269 :
    (D_op_stw)? 56'h20202020737477 :
    (D_op_blt)? 56'h20202020626c74 :
    (D_op_ldw)? 56'h202020206c6477 :
    (D_op_cmpnei)? 56'h20636d706e6569 :
    (D_op_flushda)? 56'h666c7573686461 :
    (D_op_xori)? 56'h202020786f7269 :
    (D_op_bne)? 56'h20202020626e65 :
    (D_op_cmpeqi)? 56'h20636d70657169 :
    (D_op_ldbuio)? 56'h206c646275696f :
    (D_op_muli)? 56'h2020206d756c69 :
    (D_op_stbio)? 56'h20207374626f :
    (D_op_beq)? 56'h20202020626571 :
    (D_op_ldbio)? 56'h20206c6462696f :
    (D_op_cmpgeui)? 56'h636d7067657569 :
    (D_op_ldhuio)? 56'h206c646875696f :
    (D_op_andhi)? 56'h2020616e646869 :
    (D_op_sthio)? 56'h20207374686f :
    (D_op_bgeu)? 56'h20202062676575 :
    (D_op_ldhio)? 56'h20206c6468696f :
    (D_op_cmpltui)? 56'h636d706c747569 :
    (D_op_initd)? 56'h2020696e697464 :
    (D_op_orhi)? 56'h2020206f726869 :
    (D_op_stwio)? 56'h20207374776f :
    (D_op_bltu)? 56'h202020626c7475 :
    (D_op_ldwio)? 56'h20206c6477696f :
    (D_op_flushd)? 56'h20666c75736864 :
    (D_op_xorhi)? 56'h2020786f726869 :
    (D_op_eret)? 56'h20202065726574 :
    (D_op_roli)? 56'h202020726f6c69 :
    (D_op_rol)? 56'h20202020726f6c :
    (D_op_flushp)? 56'h20666c75736870 :
    (D_op_ret)? 56'h20202020726574 :
    (D_op_nor)? 56'h202020206e6f72 :
```

```
      (D_op_mulxuu)? 56'h206d756c787575 :
      (D_op_cmpge)? 56'h2020636d706765 :
      (D_op_bret)? 56'h20202062726574 :
      (D_op_ror)? 56'h20202020726f72 :
      (D_op_flushi)? 56'h20666c75736869 :
      (D_op_jmp)? 56'h202020206a6d70 :
      (D_op_and)? 56'h20202020616e64 :
      (D_op_cmplt)? 56'h2020636d706c74 :
      (D_op_slli)? 56'h202020736c6c69 :
      (D_op_sll)? 56'h20202020736c6c :
      (D_op_or)? 56'h20202020206f72 :
      (D_op_mulxsu)? 56'h206d756c787375 :
      (D_op_cmpne)? 56'h2020636d706e65 :
      (D_op_srli)? 56'h20202073726c69 :
      (D_op_srl)? 56'h2020202073726c :
      (D_op_nextpc)? 56'h206e6578747063 :
      (D_op_callr)? 56'h202063616c6c72 :
      (D_op_xor)? 56'h20202020786f72 :
      (D_op_mulxss)? 56'h206d756c787373 :
      (D_op_cmpeq)? 56'h2020636d706571 :
      (D_op_divu)? 56'h20202064697675 :
      (D_op_div)? 56'h20202020646976 :
      (D_op_rdctl)? 56'h2020726463746c :
      (D_op_mul)? 56'h202020206d756c :
      (D_op_cmpgeu)? 56'h20636d70676575 :
      (D_op_initi)? 56'h2020696e697469 :
      (D_op_trap)? 56'h20202074726170 :
      (D_op_wrctl)? 56'h2020777263746c :
      (D_op_cmpltu)? 56'h20636d706c7475 :
      (D_op_add)? 56'h20202020616464 :
      (D_op_break)? 56'h2020627265616b :
      (D_op_hbreak)? 56'h2068627265616b :
      (D_op_sync)? 56'h20202073796e63 :
      (D_op_sub)? 56'h20202020737562 :
      (D_op_srai)? 56'h20202073726169 :
      (D_op_sra)? 56'h20202020737261 :
      (D_op_intr)? 56'h202020696e7472 :
      56'h20202020424144;

   assign F_vinst = F_valid ? F_inst : {7{8'h2d}};
   assign D_vinst = D_valid ? D_inst : {7{8'h2d}};
   assign R_vinst = R_valid ? D_inst : {7{8'h2d}};
   assign E_vinst = E_valid ? D_inst : {7{8'h2d}};
   assign W_vinst = W_valid ? D_inst : {7{8'h2d}};

//////////////// END SIMULATION-ONLY CONTENTS

//synthesis translate_on

endmodule
```

De2_i2c_av_config.v

```
/*
  * I2C bus control for initializing the audio and video chips on the DE2 board
```

```
 *
 * Adapted by Stephen A. Edwards, Columbia University, sedwards@cs.columbia.edu
 */

module de2_i2c_av_config( iCLK, iRST_N, I2C_SCLK, I2C_SDAT );

// From host

input     iCLK;
input     iRST_N;

// I2C bus

output    I2C_SCLK;
inout     I2C_SDAT;

// Internal Registers/Wires
reg       [15:0]   mI2C_CLK_DIV;
reg       [23:0]   mI2C_DATA;
reg                mI2C_CTRL_CLK;
reg                mI2C_GO;
wire               mI2C_END;
wire               mI2C_ACK;
reg       [15:0]   LUT_DATA;
reg       [5:0]    LUT_INDEX;
reg       [3:0]    mSetup_ST;

// Clock frequencies
parameter CLK_Freq          = 50000000; // 50 MHz
parameter I2C_Freq          = 20000;       // 20 kHz

parameter LUT_SIZE          = 50;

// Audio Data Index
parameter SET_LIN_L         = 0;
parameter SET_LIN_R         = 1;
parameter SET_HEAD_L        = 2;
parameter SET_HEAD_R        = 3;
parameter A_PATH_CTRL       = 4;
parameter D_PATH_CTRL       = 5;
parameter POWER_ON          = 6;
parameter SET_FORMAT        = 7;
parameter SAMPLE_CTRL       = 8;
parameter SET_ACTIVE        = 9;
// Video Data Index
parameter SET_VIDEO         = 10;

// I2C Control Clock
always @(posedge iCLK or negedge iRST_N)
begin
   if (!iRST_N)
      begin
         mI2C_CTRL_CLK <= 0;
         mI2C_CLK_DIV    <= 0;
      end
   else
      begin
        if ( mI2C_CLK_DIV < (CLK_Freq/I2C_Freq) )
```

```
            mI2C_CLK_DIV <= mI2C_CLK_DIV+1;
        else
           begin
              mI2C_CLK_DIV    <= 0;
              mI2C_CTRL_CLK <= ~mI2C_CTRL_CLK;
           end
      end
end


de2_i2c_controller u0 (
   .CLOCK(mI2C_CTRL_CLK), //    Controller Work Clock
   .I2C_SCLK(I2C_SCLK),      //    I2C CLOCK
   .I2C_SDAT(I2C_SDAT),      //    I2C DATA
   .I2C_DATA(mI2C_DATA),    //    DATA:[SLAVE_ADDR,SUB_ADDR,DATA]
   .GO(mI2C_GO),                 //    GO transfor
   .END(mI2C_END),              //    END transfor
   .ACK(mI2C_ACK),              //    ACK
   .RESET(iRST_N)
);

// Configuration control
always @(posedge mI2C_CTRL_CLK or negedge iRST_N)
begin
   if(!iRST_N)
   begin
      LUT_INDEX <= 0;
      mSetup_ST <= 0;
      mI2C_GO      <= 0;
   end
   else
   begin
      if (LUT_INDEX<LUT_SIZE)
      begin
         case(mSetup_ST)
         0:    begin
                  if(LUT_INDEX<SET_VIDEO)
                     mI2C_DATA <= {8'h34,LUT_DATA};
                  else
                     mI2C_DATA <= {8'h40,LUT_DATA};
                  mI2C_GO      <= 1;
                  mSetup_ST <= 1;
               end
         1:    begin
                  if (mI2C_END)
                     begin
                        if (!mI2C_ACK)
                           mSetup_ST <= 2;
                        else
                           mSetup_ST <= 0;
                     mI2C_GO <= 0;
                  end
               end
         2:    begin
                  LUT_INDEX <= LUT_INDEX+1;
                  mSetup_ST <= 0;
               end
         endcase
```

```
      end
   end
end

// Configuration data LUT
always
begin
   case (LUT_INDEX)
   // Audio Config Data
   SET_LIN_L       : LUT_DATA <= 16'h001A;
   SET_LIN_R       : LUT_DATA <= 16'h021A;
   SET_HEAD_L      : LUT_DATA <= 16'h047B;
   SET_HEAD_R      : LUT_DATA <= 16'h067B;
   A_PATH_CTRL     : LUT_DATA <= 16'h08F8;
   D_PATH_CTRL     : LUT_DATA <= 16'h0A06;
   POWER_ON        : LUT_DATA <= 16'h0C00;
   SET_FORMAT      : LUT_DATA <= 16'h0E01;
   SAMPLE_CTRL     : LUT_DATA <= 16'h1002;
   SET_ACTIVE      : LUT_DATA <= 16'h1201;
   // Video Config Data
   SET_VIDEO+0     : LUT_DATA <= 16'h1500;
   SET_VIDEO+1     : LUT_DATA <= 16'h1741;
   SET_VIDEO+2     : LUT_DATA <= 16'h3a16;
   SET_VIDEO+3     : LUT_DATA <= 16'h5004;
   SET_VIDEO+4     : LUT_DATA <= 16'hc305;
   SET_VIDEO+5     : LUT_DATA <= 16'hc480;
   SET_VIDEO+6     : LUT_DATA <= 16'h0e80;
   SET_VIDEO+7     : LUT_DATA <= 16'h5020;
   SET_VIDEO+8     : LUT_DATA <= 16'h5218;
   SET_VIDEO+9     : LUT_DATA <= 16'h58ed;
   SET_VIDEO+10 : LUT_DATA <= 16'h77c5;
   SET_VIDEO+11 : LUT_DATA <= 16'h7c93;
   SET_VIDEO+12 : LUT_DATA <= 16'h7d00;
   SET_VIDEO+13 : LUT_DATA <= 16'hd048;
   SET_VIDEO+14 : LUT_DATA <= 16'hd5a0;
   SET_VIDEO+15 : LUT_DATA <= 16'hd7ea;
   SET_VIDEO+16 : LUT_DATA <= 16'he43e;
   SET_VIDEO+17 : LUT_DATA <= 16'hea0f;
   SET_VIDEO+18 : LUT_DATA <= 16'h3112;
   SET_VIDEO+19 : LUT_DATA <= 16'h3281;
   SET_VIDEO+20 : LUT_DATA <= 16'h3384;
   SET_VIDEO+21 : LUT_DATA <= 16'h37A0;
   SET_VIDEO+22 : LUT_DATA <= 16'he580;
   SET_VIDEO+23 : LUT_DATA <= 16'he603;
   SET_VIDEO+24 : LUT_DATA <= 16'he785;
   SET_VIDEO+25 : LUT_DATA <= 16'h5000;
   SET_VIDEO+26 : LUT_DATA <= 16'h5100;
   SET_VIDEO+27 : LUT_DATA <= 16'h0050;
   SET_VIDEO+28 : LUT_DATA <= 16'h1000;
   SET_VIDEO+29 : LUT_DATA <= 16'h0402;
   SET_VIDEO+30 : LUT_DATA <= 16'h0b00;
   SET_VIDEO+31 : LUT_DATA <= 16'h0a20;
   SET_VIDEO+32 : LUT_DATA <= 16'h1100;
   SET_VIDEO+33 : LUT_DATA <= 16'h2b00;
   SET_VIDEO+34 : LUT_DATA <= 16'h2c8c;
   SET_VIDEO+35 : LUT_DATA <= 16'h2df2;
   SET_VIDEO+36 : LUT_DATA <= 16'h2eee;
   SET_VIDEO+37 : LUT_DATA <= 16'h2ff4;
```

```
   SET_VIDEO+38 : LUT_DATA <= 16'h30d2;
   SET_VIDEO+39 : LUT_DATA <= 16'h0e05;
   default      : LUT_DATA <= 16'hxxxx;
   endcase
end

endmodule
```

De2_i2c_controller.v

```
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//
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//                     356 Fu-Shin E. Rd Sec. 1. JhuBei City,
//                     HsinChu County, Taiwan
//                     302
//
//                     web: http://www.terasic.com/
//                     email: support@terasic.com
//
// --------------------------------------------------------------------
//
// Major Functions:i2c controller
//
// --------------------------------------------------------------------
//
// Revision History :
// --------------------------------------------------------------------
//     Ver  :| Author            :| Mod. Date :| Changes Made:
//     V1.0 :| Joe Yang          :| 05/07/10  :|      Initial Revision
// --------------------------------------------------------------------
module de2_i2c_controller (
   CLOCK,
   I2C_SCLK, // I2C CLOCK
   I2C_SDAT, // I2C DATA
   I2C_DATA, // DATA:[SLAVE_ADDR,SUB_ADDR,DATA]
```

```
   GO,            // GO transfor
   END,           // END transfor
   W_R,           // W_R
   ACK,           // ACK
   RESET,
   // TEST
   SD_COUNTER,
   SDO
);

input    CLOCK;
input    [23:0] I2C_DATA;
input    GO;
input    RESET;
input    W_R;
inout    I2C_SDAT;
output I2C_SCLK;
output END;
output ACK;

// TEST
output [5:0] SD_COUNTER;
output SDO;

reg SDO;
reg SCLK;
reg END;
reg [23:0] SD;
reg [5:0] SD_COUNTER;

wire I2C_SCLK = SCLK | (((SD_COUNTER >= 4) & (SD_COUNTER <= 30))? ~CLOCK : 0);
wire I2C_SDAT = SDO ? 1'bz : 0;

reg ACK1, ACK2, ACK3;
wire ACK = ACK1 | ACK2 | ACK3;

//--I2C COUNTER

always @(negedge RESET or posedge CLOCK)
begin
   if (!RESET)
      SD_COUNTER = 6'b111111;
   else
      begin
         if (GO == 0)
            SD_COUNTER = 0;
         else
            if (SD_COUNTER < 6'b111111)
               SD_COUNTER = SD_COUNTER + 1;
      end
end

always @(negedge RESET or posedge CLOCK )
begin
   if (!RESET)
      begin
         SCLK = 1;
         SDO = 1;
```

```
        ACK1 = 0;
        ACK2 = 0;
        ACK3 = 0;
        END = 1;
      end
else
  case (SD_COUNTER)
  6'd0  : begin ACK1 = 0; ACK2 = 0; ACK3 = 0; END = 0; SDO = 1; SCLK = 1; end

  // Start
  6'd1  : begin SD = I2C_DATA; SDO = 0; end
  6'd2  : SCLK = 0;

  // Slave Address
  6'd3  : SDO = SD[23];
  6'd4  : SDO = SD[22];
  6'd5  : SDO = SD[21];
  6'd6  : SDO = SD[20];
  6'd7  : SDO = SD[19];
  6'd8  : SDO = SD[18];
  6'd9  : SDO = SD[17];
  6'd10 : SDO = SD[16];
  6'd11 : SDO = 1'b1;     //ACK

  // Sub-address
  6'd12  : begin SDO = SD[15]; ACK1 = I2C_SDAT; end
  6'd13  : SDO = SD[14];
  6'd14  : SDO = SD[13];
  6'd15  : SDO = SD[12];
  6'd16  : SDO = SD[11];
  6'd17  : SDO = SD[10];
  6'd18  : SDO = SD[9];
  6'd19  : SDO = SD[8];
  6'd20  : SDO = 1'b1; // ACK

  // Data
  6'd21  : begin SDO = SD[7]; ACK2 = I2C_SDAT; end
  6'd22  : SDO = SD[6];
  6'd23  : SDO = SD[5];
  6'd24  : SDO = SD[4];
  6'd25  : SDO = SD[3];
  6'd26  : SDO = SD[2];
  6'd27  : SDO = SD[1];
  6'd28  : SDO = SD[0];
  6'd29  : SDO = 1'b1;   // ACK

  // Stop
  6'd30 : begin SDO = 1'b0; SCLK = 1'b0; ACK3 = I2C_SDAT; end
  6'd31 : SCLK = 1'b1;
  6'd32 : begin SDO = 1'b1; END = 1; end
  endcase
end

endmodule
```

De2_LTM_Test.v

```
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//                              HsinChu County, Taiwan
//                              302
//
//                              web: http://www.terasic.com/
//                              email: support@terasic.com
//
// --------------------------------------------------------------------
//
// Major Functions: DE2 LTM    Test
//
// --------------------------------------------------------------------
//
// Revision History :
// --------------------------------------------------------------------
//     Ver    :| Author                        :| Mod. Date :| Changes Made:
//     V1.0 :| Joe Yang ,Johnny Fan      :| 07/04/12    :| Initial Revision
//     V1.1 :| ben                             :| 11/03/14    :| Quartus 10.1 sp1
// --------------------------------------------------------------------

module DE2_LTM_Test
    (
        ////////////////////// Clock Input          //////////////////////
        CLOCK_27,                                  //    27 MHz
        CLOCK_50,                                  //    50 MHz
        EXT_CLOCK,                                 //    External Clock
        ////////////////////// Push Button          //////////////////////
        KEY,                                       //    Pushbutton[3:0]
        ////////////////////// DPDT Switch          //////////////////////
        SW,                                        //    Toggle Switch[17:0]
        ////////////////////// 7-SEG Dispaly  //////////////////////
        HEX0,                                            //    Seven Segment Digit 0
        HEX1,                                            //    Seven Segment Digit 1
```

```
HEX2,                                   //  Seven Segment Digit 2
HEX3,                                   //  Seven Segment Digit 3
HEX4,                                   //  Seven Segment Digit 4
HEX5,                                   //  Seven Segment Digit 5
HEX6,                                   //  Seven Segment Digit 6
HEX7,                                   //  Seven Segment Digit 7
//////////////////////  LED     //////////////////////
LEDG,                                   //  LED Green[8:0]
LEDR,                                   //  LED Red[17:0]
//////////////////////  UART    //////////////////////
UART_TXD,                       //  UART Transmitter
UART_RXD,                       //  UART Receiver
//////////////////////  IRDA//////////////////////
IRDA_TXD,                       //  IRDA Transmitter
IRDA_RXD,                       //  IRDA Receiver
////////////////////    SDRAM Interface     ////////////////
DRAM_DQ,                                //  SDRAM Data bus 16 Bits
DRAM_ADDR,                      //  SDRAM Address bus 12 Bits
DRAM_LDQM,                      //  SDRAM Low-byte Data Mask
DRAM_UDQM,                              //  SDRAM High-byte Data Mask
DRAM_WE_N,                      //  SDRAM Write Enable
DRAM_CAS_N,                             //  SDRAM Column Address Strobe
DRAM_RAS_N,                             //  SDRAM Row Address Strobe
DRAM_CS_N,                      //  SDRAM Chip Select
DRAM_BA_0,                      //  SDRAM Bank Address 0
DRAM_BA_1,                      //  SDRAM Bank Address 0
DRAM_CLK,                       //  SDRAM Clock
DRAM_CKE,                       //  SDRAM Clock Enable
////////////////////// Flash Interface  ////////////////
FL_DQ,                          //  FLASH Data bus 8 Bits
FL_ADDR,                        //  FLASH Address bus 22 Bits
FL_WE_N,                                //  FLASH Write Enable
FL_RST_N,                       //  FLASH Reset
FL_OE_N,                        //  FLASH Output Enable
FL_CE_N,                        //  FLASH Chip Enable
////////////////////// SRAM Interface       ////////////////
SRAM_DQ,                                //  SRAM Data bus 16 Bits
SRAM_ADDR,                      //  SRAM Address bus 18 Bits
SRAM_UB_N,                      //  SRAM High-byte Data Mask
SRAM_LB_N,                      //  SRAM Low-byte Data Mask
SRAM_WE_N,                      //  SRAM Write Enable
SRAM_CE_N,                      //  SRAM Chip Enable
SRAM_OE_N,                      //  SRAM Output Enable
////////////////////// ISP1362 Interface    ////////////////
OTG_DATA,                       //  ISP1362 Data bus 16 Bits
OTG_ADDR,                       //  ISP1362 Address 2 Bits
OTG_CS_N,                       //  ISP1362 Chip Select
OTG_RD_N,                       //  ISP1362 Write
OTG_WR_N,                       //  ISP1362 Read
OTG_RST_N,                      //  ISP1362 Reset
OTG_FSPEED,                     //  USB Full Speed,     0 = Enable, Z = Disable
OTG_LSPEED,                     //  USB Low Speed,      0 = Enable, Z = Disable
OTG_INT0,                       //  ISP1362 Interrupt 0
OTG_INT1,                       //  ISP1362 Interrupt 1
OTG_DREQ0,                      //  ISP1362 DMA Request 0
OTG_DREQ1,                      //  ISP1362 DMA Request 1
OTG_DACK0_N,                    //  ISP1362 DMA Acknowledge 0
OTG_DACK1_N,                    //  ISP1362 DMA Acknowledge 1
```

```
        ////////////////////  LCD Module 16X2          ////////////////
        LCD_ON,                                 //    LCD Power ON/OFF
        LCD_BLON,                               //    LCD Back Light ON/OFF
        LCD_RW,                                 //    LCD Read/Write Select, 0 = Write, 1 = Read
        LCD_EN,                                 //    LCD Enable
        LCD_RS,                                 //    LCD Command/Data Select, 0 = Command,
1 = Data
        LCD_DATA,                               //    LCD Data bus 8 bits
        ////////////////////  SD_Card Interface  ////////////////
        SD_DAT,                                 //    SD Card Data
        SD_DAT3,                                      //    SD Card Data 3
        SD_CMD,                                 //    SD Card Command Signal
        SD_CLK,                                 //    SD Card Clock
        ////////////////////  USB JTAG link  ////////////////////
        TDI,                                    // CPLD -> FPGA (data in)
        TCK,                                    // CPLD -> FPGA (clk)
        TCS,                                    // CPLD -> FPGA (CS)
        TDO,                                    // FPGA -> CPLD (data out)
        ////////////////////  I2C         ////////////////////////////
        I2C_SDAT,                               //    I2C Data
        I2C_SCLK,                         //    I2C Clock
        ////////////////////  PS2         ////////////////////////////
        PS2_DAT,                                //    PS2 Data
        PS2_CLK,                                //    PS2 Clock
        ////////////////////  VGA         ////////////////////////////
        VGA_CLK,                                //    VGA Clock
        VGA_HS,                                 //    VGA H_SYNC
        VGA_VS,                                 //    VGA V_SYNC
        VGA_BLANK,                              //    VGA BLANK
        VGA_SYNC,                               //    VGA SYNC
        VGA_R,                                  //    VGA Red[9:0]
        VGA_G,                                  //    VGA Green[9:0]
        VGA_B,                                        //    VGA Blue[9:0]
        ////////////     Ethernet Interface  ////////////////////////
        ENET_DATA,                              //    DM9000A DATA bus 16Bits
        ENET_CMD,                               //    DM9000A    Command/Data    Select,    0    =
Command, 1 = Data
        ENET_CS_N,                              //    DM9000A Chip Select
        ENET_WR_N,                              //    DM9000A Write
        ENET_RD_N,                              //    DM9000A Read
        ENET_RST_N,                             //    DM9000A Reset
        ENET_INT,                               //    DM9000A Interrupt
        ENET_CLK,                               //    DM9000A Clock 25 MHz
        ////////////////      Audio CODEC       ////////////////////////
        AUD_ADCLRCK,                            //    Audio CODEC ADC LR Clock
        AUD_ADCDAT,                             //    Audio CODEC ADC Data
        AUD_DACLRCK,                            //    Audio CODEC DAC LR Clock
        AUD_DACDAT,                             //    Audio CODEC DAC Data
        AUD_BCLK,                               //    Audio CODEC Bit-Stream Clock
        AUD_XCK,                                      //    Audio CODEC Chip Clock
        ////////////////      TV Decoder        ////////////////////////
        TD_DATA,                                //    TV Decoder Data bus 8 bits
        TD_HS,                                  //    TV Decoder H_SYNC
        TD_VS,                                  //    TV Decoder V_SYNC
        TD_RESET,                               //    TV Decoder Reset
        ////////////////////  GPIO        ////////////////////////////
        GPIO_0,                                 //    GPIO Connection 0
        GPIO_1,                                 //    GPIO Connection 1
```

```
    );
//=============================================================================
// PORT declarations
//=============================================================================

///////////////////////  Clock Input          ///////////////////////
input               CLOCK_27;                   //    27 MHz
input               CLOCK_50;                   //    50 MHz
input               EXT_CLOCK;                  //    External Clock
///////////////////////  Push Button          ///////////////////////
input     [3:0]  KEY;                           //    Pushbutton[3:0]
///////////////////////  DPDT Switch          ///////////////////////
input     [17:0]     SW;                        //    Toggle Switch[17:0]
///////////////////////  7-SEG Dispaly  ///////////////////////
output    [6:0]  HEX0;                          //    Seven Segment Digit 0
output    [6:0]  HEX1;                          //    Seven Segment Digit 1
output    [6:0]  HEX2;                          //    Seven Segment Digit 2
output    [6:0]  HEX3;                          //    Seven Segment Digit 3
output    [6:0]  HEX4;                          //    Seven Segment Digit 4
output    [6:0]  HEX5;                          //    Seven Segment Digit 5
output    [6:0]  HEX6;                          //    Seven Segment Digit 6
output    [6:0]  HEX7;                          //    Seven Segment Digit 7
////////////////////////////    LED        ////////////////////////////
output    [8:0]  LEDG;                          //    LED Green[8:0]
output    [17:0]LEDR;                           //    LED Red[17:0]
////////////////////////////    UART       ////////////////////////////
output          UART_TXD;                       //    UART Transmitter
input               UART_RXD;                   //    UART Receiver
////////////////////////////    IRDA////////////////////////////
output          IRDA_TXD;                       //    IRDA Transmitter
input               IRDA_RXD;                   //    IRDA Receiver
///////////////////////         SDRAM Interface    ///////////////////////
inout     [15:0]     DRAM_DQ;                        //    SDRAM Data bus 16 Bits
output[11:0]   DRAM_ADDR;                  //    SDRAM Address bus 12 Bits
output              DRAM_LDQM;                  //    SDRAM Low-byte Data Mask
output              DRAM_UDQM;                      //    SDRAM High-byte Data Mask
output              DRAM_WE_N;                  //    SDRAM Write Enable
output              DRAM_CAS_N;                     //    SDRAM Column Address Strobe
output              DRAM_RAS_N;                     //    SDRAM Row Address Strobe
output              DRAM_CS_N;                  //    SDRAM Chip Select
output              DRAM_BA_0;                  //    SDRAM Bank Address 0
output              DRAM_BA_1;                  //    SDRAM Bank Address 0
output              DRAM_CLK;                   //    SDRAM Clock
output              DRAM_CKE;                   //    SDRAM Clock Enable
///////////////////////  Flash Interface////////////////////////
inout           [7:0]  FL_DQ;                  //    FLASH Data bus 8 Bits
output    [21:0]FL_ADDR;                       //    FLASH Address bus 22 Bits
output              FL_WE_N;                        //    FLASH Write Enable
output              FL_RST_N;                   //    FLASH Reset
output              FL_OE_N;                    //    FLASH Output Enable
output              FL_CE_N;                    //    FLASH Chip Enable
///////////////////////  SRAM Interface     ///////////////////////
inout     [15:0]     SRAM_DQ;                        //    SRAM Data bus 16 Bits
output[17:0]   SRAM_ADDR;                  //    SRAM Address bus 18 Bits
output              SRAM_UB_N;                  //    SRAM High-byte Data Mask
output              SRAM_LB_N;                  //    SRAM Low-byte Data Mask
output              SRAM_WE_N;                  //    SRAM Write Enable
output              SRAM_CE_N;                  //    SRAM Chip Enable
```

```
output              SRAM_OE_N;              //    SRAM Output Enable
//////////////////// ISP1362 Interface   ////////////////////////
inout     [15:0]    OTG_DATA;               //    ISP1362 Data bus 16 Bits
output[1:0]         OTG_ADDR;               //    ISP1362 Address 2 Bits
output              OTG_CS_N;               //    ISP1362 Chip Select
output              OTG_RD_N;               //    ISP1362 Write
output              OTG_WR_N;               //    ISP1362 Read
output              OTG_RST_N;              //    ISP1362 Reset
output              OTG_FSPEED;             //    USB Full Speed,     0 = Enable, Z = Disable
output              OTG_LSPEED;             //    USB Low Speed,      0 = Enable, Z = Disable
input                   OTG_INT0;               //    ISP1362 Interrupt 0
input                   OTG_INT1;               //    ISP1362 Interrupt 1
input                   OTG_DREQ0;              //    ISP1362 DMA Request 0
input                   OTG_DREQ1;              //    ISP1362 DMA Request 1
output              OTG_DACK0_N;            //    ISP1362 DMA Acknowledge 0
output              OTG_DACK1_N;            //    ISP1362 DMA Acknowledge 1
//////////////////// LCD Module 16X2   ////////////////////////////
inout           [7:0]LCD_DATA;              //    LCD Data bus 8 bits
output              LCD_ON;                 //    LCD Power ON/OFF
output              LCD_BLON;               //    LCD Back Light ON/OFF
output              LCD_RW;                 //    LCD Read/Write Select, 0 = Write, 1 = Read
output              LCD_EN;                 //    LCD Enable
output              LCD_RS;                 //    LCD Command/Data Select, 0 = Command,
1 = Data
//////////////////// SD Card Interface   ////////////////////////
inout                   SD_DAT;                 //    SD Card Data
inout                   SD_DAT3;                    //    SD Card Data 3
inout                   SD_CMD;                 //    SD Card Command Signal
output              SD_CLK;                 //    SD Card Clock
////////////////////////  I2C       ////////////////////////////////
inout                   I2C_SDAT;                   //    I2C Data
output              I2C_SCLK;               //    I2C Clock
////////////////////////  PS2       ////////////////////////////////
input                   PS2_DAT;                //    PS2 Data
input                   PS2_CLK;                //    PS2 Clock
//////////////////// USB JTAG link  ////////////////////////////
input               TDI;                    // CPLD -> FPGA (data in)
input               TCK;                    // CPLD -> FPGA (clk)
input               TCS;                    // CPLD -> FPGA (CS)
output              TDO;                        // FPGA -> CPLD (data out)
////////////////////////  VGA           ////////////////////////////
output              VGA_CLK;                //    VGA Clock
output              VGA_HS;                 //    VGA H_SYNC
output              VGA_VS;                 //    VGA V_SYNC
output              VGA_BLANK;              //    VGA BLANK
output              VGA_SYNC;               //    VGA SYNC
output    [9:0]VGA_R;                   //    VGA Red[9:0]
output    [9:0]VGA_G;                   //    VGA Green[9:0]
output    [9:0]VGA_B;                   //    VGA Blue[9:0]
////////////////      Ethernet Interface  ////////////////////////////
inout     [15:0]    ENET_DATA;              //    DM9000A DATA bus 16Bits
output              ENET_CMD;               //    DM9000A    Command/Data    Select,    0    =
Command, 1 = Data
output              ENET_CS_N;              //    DM9000A Chip Select
output              ENET_WR_N;              //    DM9000A Write
output              ENET_RD_N;              //    DM9000A Read
output              ENET_RST_N;             //    DM9000A Reset
input                   ENET_INT;               //    DM9000A Interrupt
```

```
output              ENET_CLK;                   //    DM9000A Clock 25 MHz
////////////////////// Audio CODEC        ////////////////////////////
inout                    AUD_ADCLRCK;           //    Audio CODEC ADC LR Clock
input                    AUD_ADCDAT;                 //    Audio CODEC ADC Data
inout                    AUD_DACLRCK;           //    Audio CODEC DAC LR Clock
output              AUD_DACDAT;                 //    Audio CODEC DAC Data
inout                    AUD_BCLK;              //    Audio CODEC Bit-Stream Clock
output              AUD_XCK;                    //    Audio CODEC Chip Clock
////////////////////// TV Devoder         ////////////////////////////
input          [7:0] TD_DATA;                   //    TV Decoder Data bus 8 bits
input                    TD_HS;                 //    TV Decoder H_SYNC
input                    TD_VS;                 //    TV Decoder V_SYNC
output              TD_RESET;                   //    TV Decoder Reset
////////////////////////   GPIO      ////////////////////////////////
inout     [35:0]    GPIO_0;                     //    GPIO Connection 0
inout     [35:0]    GPIO_1;                     //    GPIO Connection 1

assign    LCD_ON        =    1'b1;
assign    LCD_BLON      =    1'b1;

//    All inout port turn to tri-state
assign    DRAM_DQ           =    16'hzzzz;
assign    FL_DQ             =    8'hzz;
assign    SRAM_DQ           =    16'hzzzz;
assign    OTG_DATA          =    16'hzzzz;
assign    LCD_DATA          =    8'hzz;
assign    SD_DAT        =    1'bz;
assign    ENET_DATA     =    16'hzzzz;
assign    AUD_ADCLRCK       =    1'bz;
assign    AUD_DACLRCK       =    1'bz;
assign    AUD_BCLK          =    1'bz;
assign    GPIO_1        =    36'hzzzzzzzzz;
//=============================================================================
// REG/WIRE declarations
//=============================================================================
// Touch panel signal //
wire [7:0] ltm_r;          //    LTM Red Data 8 Bits
wire [7:0] ltm_g;          //    LTM Green Data 8 Bits
wire [7:0] ltm_b;          //    LTM Blue Data 8 Bits
wire       ltm_nclk; //    LTM Clcok
wire       ltm_hd;
wire       ltm_vd;
wire       ltm_den;
wire       ltm_grst;
// lcd 3wire interface//
wire       ltm_sclk;
wire       ltm_sda;
wire       ltm_scen;
wire            ltm_3wirebusy_n;
// Touch Screen Digitizer ADC
wire            adc_dclk;
wire            adc_cs;
wire            adc_penirq_n;
wire            adc_busy;
wire            adc_din;
wire            adc_dout;
wire            adc_ltm_sclk;
```

```
wire [11:0]      x_coord;
wire [11:0]      y_coord;
wire             new_coord;
wire [1:0] display_mode;
reg  [31:0]      div;

////////////// GPIO_O /////////////////
assign      adc_penirq_n    =GPIO_0[0];
assign      adc_dout        =GPIO_0[1];
assign      adc_busy        =GPIO_0[2];
assign      GPIO_0[3]       =adc_din;
assign      GPIO_0[4]       =adc_ltm_sclk;
assign      GPIO_0[5]       =ltm_b[3];
assign      GPIO_0[6]       =ltm_b[2];
assign      GPIO_0[7]       =ltm_b[1];
assign      GPIO_0[8]       =ltm_b[0];
assign      GPIO_0[9]       =ltm_nclk;
assign      GPIO_0[10]      =ltm_den;
assign      GPIO_0[11]      =ltm_hd;
assign      GPIO_0[12]      =ltm_vd;
assign      GPIO_0[13]      =ltm_b[4];
assign      GPIO_0[14]      =ltm_b[5];
assign      GPIO_0[15]      =ltm_b[6];
assign      GPIO_0[16]      =ltm_b[7];
assign      GPIO_0[17]      =ltm_g[0];
assign      GPIO_0[18]      =ltm_g[1];
assign      GPIO_0[19]      =ltm_g[2];
assign      GPIO_0[20]      =ltm_g[3];
assign      GPIO_0[21]      =ltm_g[4];
assign      GPIO_0[22]      =ltm_g[5];
assign      GPIO_0[23]      =ltm_g[6];
assign      GPIO_0[24]      =ltm_g[7];
assign      GPIO_0[25]      =ltm_r[0];
assign      GPIO_0[26]      =ltm_r[1];
assign      GPIO_0[27]      =ltm_r[2];
assign      GPIO_0[28]      =ltm_r[3];
assign      GPIO_0[29]      =ltm_r[4];
assign      GPIO_0[30]      =ltm_r[5];
assign      GPIO_0[31]      =ltm_r[6];
assign      GPIO_0[32]      =ltm_r[7];
assign      GPIO_0[33]      =ltm_grst;
assign      GPIO_0[34]      =ltm_scen;
assign      GPIO_0[35]      =ltm_sda;

assign adc_ltm_sclk= ( adc_dclk & ltm_3wirebusy_n )    |    ( ~ltm_3wirebusy_n & ltm_sclk );
assign ltm_nclk = div[0]; // 25 Mhz
assign ltm_grst = KEY[0];
always @(posedge CLOCK_50)
      begin
            div <= div+1;
      end

SEG7_LUT_8          u1    (
                          .oSEG0(HEX0),
                          .oSEG1(HEX1),
                          .oSEG2(HEX2),
                          .oSEG3(HEX3),
                          .oSEG4(HEX4),
```

```
                        .oSEG5(HEX5),
                        .oSEG6(HEX6),
                        .oSEG7(HEX7),
                        .iDIG({ 4'h0 , x_coord , 4'h0 , y_coord }),
                        .ON_OFF(8'b01110111)
                        );

// lcd 3 wire interface configuration    //
lcd_spi_cotroller    u2    (
                        // Host Side
                        .iCLK(CLOCK_50),
                        .iRST_n(DLY0),
                        // 3wire Side
                        .o3WIRE_SCLK(ltm_sclk),
                        .io3WIRE_SDAT(ltm_sda),
                        .o3WIRE_SCEN(ltm_scen),
                        .o3WIRE_BUSY_n(ltm_3wirebusy_n)
                        );

// system reset    //
Reset_Delay          u3    (.iCLK(CLOCK_50),
                        .iRST(KEY[0]),
                        .oRST_0(DLY0),
                        .oRST_1(DLY1),
                        .oRST_2(DLY2)
                        );
// Touch Screen Digitizer ADC configuration //
//adc_spi_controller            u4    (
//                        .iCLK(CLOCK_50),
//                        .iRST_n(DLY0),
//                        .oADC_DIN(adc_din),
//                        .oADC_DCLK(adc_dclk),
//                        .oADC_CS(adc_cs),
//                        .iADC_DOUT(adc_dout),
//                        .iADC_BUSY(adc_busy),
//                        .iADC_PENIRQ_n(adc_penirq_n),
//                        .oTOUCH_IRQ(touch_irq),
//                        .oX_COORD(x_coord),
//                        .oY_COORD(y_coord),
//                        .oNEW_COORD(new_coord),
//                        );
//
//touch_irq_detector    u5    (
//                        .clk(CLOCK_50),
//                        .reset_n(DLY0),
//                        .iTOUCH_IRQ(touch_irq),
//                        .iX_COORD(x_coord),
//                        .iY_COORD(y_coord),
//                        .iNEW_COORD(new_coord),
//                        .oDISPLAY_MODE(display_mode),
//                        );
//
//lcd_timing_controller        u6    (
//                        .clk(ltm_nclk),
//                        .reset_n(DLY2),
//                        // lcd side
//                        .oLCD_R(ltm_r),
//                        .oLCD_G(ltm_g),
```

```
//                          .oLCD_B(ltm_b),
//                          .oHD(ltm_hd),
//                          .oVD(ltm_vd),
//                          .oDEN(ltm_den),
//                          .iDISPLAY_MODE(display_mode),
//                          );

nios_system DUT
      (
         .SRAM_ADDR_from_the_sram                                  (SRAM_ADDR),
         .SRAM_CE_N_from_the_sram                                  (SRAM_CE_N),
         .SRAM_DQ_to_and_from_the_sram                             (SRAM_DQ),
         .SRAM_LB_N_from_the_sram                                  (SRAM_LB_N),
         .SRAM_OE_N_from_the_sram                                  (SRAM_OE_N),
         .SRAM_UB_N_from_the_sram                                  (SRAM_UB_N),
         .SRAM_WE_N_from_the_sram                                  (SRAM_WE_N),
         .clk_0                                                    (CLOCK_50),
         .iADC_BUSY_to_the_adc_spi_controller_0                    (GPIO_0[2]),
         .iADC_DOUT_to_the_adc_spi_controller_0                    (GPIO_0[1]),
         .iADC_PENIRQ_n_to_the_adc_spi_controller_0                (GPIO_0[0]),
         .iDISPLAY_MODE_to_the_lcd_timing_controller_0             (display_mode),
         .oADC_CS_from_the_adc_spi_controller_0                    (adc_cs),
         .oADC_DCLK_from_the_adc_spi_controller_0                  (adc_dclk),
         .oADC_DIN_from_the_adc_spi_controller_0                   (adc_din),
         .oDEN_from_the_lcd_timing_controller_0                    (ltm_den),
         .oHD_from_the_lcd_timing_controller_0                     (ltm_hd),
         .oLCD_B_from_the_lcd_timing_controller_0                  (ltm_b),
         .oLCD_G_from_the_lcd_timing_controller_0                  (ltm_g),
         .oLCD_R_from_the_lcd_timing_controller_0                  (ltm_r),
         .oNEW_COORD_from_the_adc_spi_controller_0                 (new_coord),
         .oTOUCH_IRQ_from_the_adc_spi_controller_0                 (touch_irq),
         .oVD_from_the_lcd_timing_controller_0                     (ltm_vd),
         .oX_COORD_from_the_adc_spi_controller_0                   (x_coord),
         .oY_COORD_from_the_adc_spi_controller_0                   (y_coord),
         .reset_n                                                  (1)
      );

endmodule
```

DE2_TOP_PROJECT.v

```
// --------------------------------------------------------------------
// Copyright (c) 2005 by Terasic Technologies Inc.
// --------------------------------------------------------------------
//
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```

```
//      This VHDL/Verilog or C/C++ source code is intended as a design reference
//      which illustrates how these types of functions can be implemented.
//      It is the user's responsibility to verify their design for
//      consistency and functionality through the use of formal
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//
// --------------------------------------------------------------------
//
//                              Terasic Technologies Inc
//                              356 Fu-Shin E. Rd Sec. 1. JhuBei City,
//                              HsinChu County, Taiwan
//                              302
//
//                              web: http://www.terasic.com/
//                              email: support@terasic.com
//
// --------------------------------------------------------------------
//
// Major Functions: DE2 LTM    Test
//
// --------------------------------------------------------------------
//
// Revision History :
// --------------------------------------------------------------------
//      Ver    :| Author                    :| Mod. Date :| Changes Made:
//      V1.0 :| Joe Yang ,Johnny Fan      :| 07/04/12    :| Initial Revision
//      V1.1 :| ben                         :| 11/03/14    :| Quartus 10.1 sp1
// --------------------------------------------------------------------

module DE2_TOP_PROJECT
      (
            ////////////////////// Clock Input           //////////////////////
            CLOCK_27,                                   //    27 MHz
            CLOCK_50,                                   //    50 MHz
            EXT_CLOCK,                                  //    External Clock
            ////////////////////// Push Button           //////////////////////
            KEY,                                        //    Pushbutton[3:0]
            ////////////////////// DPDT Switch           //////////////////////
            SW,                                         //    Toggle Switch[17:0]
            ////////////////////// 7-SEG Dispaly  //////////////////////
            HEX0,                                             //    Seven Segment Digit 0
            HEX1,                                             //    Seven Segment Digit 1
            HEX2,                                             //    Seven Segment Digit 2
            HEX3,                                             //    Seven Segment Digit 3
            HEX4,                                             //    Seven Segment Digit 4
            HEX5,                                             //    Seven Segment Digit 5
            HEX6,                                             //    Seven Segment Digit 6
            HEX7,                                             //    Seven Segment Digit 7
            ////////////////////////   LED        ////////////////////////
            LEDG,                                             //    LED Green[8:0]
            LEDR,                                             //    LED Red[17:0]
            ////////////////////////   UART       ////////////////////////
            UART_TXD,                                   //    UART Transmitter
            UART_RXD,                                   //    UART Receiver
            ////////////////////////   IRDA////////////////////////
            IRDA_TXD,                                   //    IRDA Transmitter
            IRDA_RXD,                                   //    IRDA Receiver
```

```
        ////////////////////     SDRAM Interface        ////////////////
        DRAM_DQ,                                    //    SDRAM Data bus 16 Bits
        DRAM_ADDR,                          //    SDRAM Address bus 12 Bits
        DRAM_LDQM,                          //    SDRAM Low-byte Data Mask
        DRAM_UDQM,                                  //    SDRAM High-byte Data Mask
        DRAM_WE_N,                          //    SDRAM Write Enable
        DRAM_CAS_N,                                 //    SDRAM Column Address Strobe
        DRAM_RAS_N,                                 //    SDRAM Row Address Strobe
        DRAM_CS_N,                          //    SDRAM Chip Select
        DRAM_BA_0,                          //    SDRAM Bank Address 0
        DRAM_BA_1,                          //    SDRAM Bank Address 0
        DRAM_CLK,                           //    SDRAM Clock
        DRAM_CKE,                           //    SDRAM Clock Enable
        ////////////////////// Flash Interface     ////////////////
        FL_DQ,                              //    FLASH Data bus 8 Bits
        FL_ADDR,                            //    FLASH Address bus 22 Bits
        FL_WE_N,                                    //    FLASH Write Enable
        FL_RST_N,                           //    FLASH Reset
        FL_OE_N,                            //    FLASH Output Enable
        FL_CE_N,                            //    FLASH Chip Enable
        ////////////////////// SRAM Interface          ////////////////
        SRAM_DQ,                                    //    SRAM Data bus 16 Bits
        SRAM_ADDR,                          //    SRAM Address bus 18 Bits
        SRAM_UB_N,                          //    SRAM High-byte Data Mask
        SRAM_LB_N,                          //    SRAM Low-byte Data Mask
        SRAM_WE_N,                          //    SRAM Write Enable
        SRAM_CE_N,                          //    SRAM Chip Enable
        SRAM_OE_N,                          //    SRAM Output Enable
        ////////////////////// ISP1362 Interface   ////////////////
        OTG_DATA,                           //    ISP1362 Data bus 16 Bits
        OTG_ADDR,                           //    ISP1362 Address 2 Bits
        OTG_CS_N,                           //    ISP1362 Chip Select
        OTG_RD_N,                           //    ISP1362 Write
        OTG_WR_N,                           //    ISP1362 Read
        OTG_RST_N,                          //    ISP1362 Reset
        OTG_FSPEED,                         //    USB Full Speed,     0 = Enable, Z = Disable
        OTG_LSPEED,                         //    USB Low Speed,      0 = Enable, Z = Disable
        OTG_INT0,                           //    ISP1362 Interrupt 0
        OTG_INT1,                           //    ISP1362 Interrupt 1
        OTG_DREQ0,                          //    ISP1362 DMA Request 0
        OTG_DREQ1,                          //    ISP1362 DMA Request 1
        OTG_DACK0_N,                        //    ISP1362 DMA Acknowledge 0
        OTG_DACK1_N,                        //    ISP1362 DMA Acknowledge 1
        ////////////////////// LCD Module 16X2     ////////////////
        LCD_ON,                             //    LCD Power ON/OFF
        LCD_BLON,                           //    LCD Back Light ON/OFF
        LCD_RW,                             //    LCD Read/Write Select, 0 = Write, 1 = Read
        LCD_EN,                             //    LCD Enable
        LCD_RS,                             //    LCD Command/Data Select, 0 = Command,
1 = Data
        LCD_DATA,                           //    LCD Data bus 8 bits
        ////////////////////// SD_Card Interface   ////////////////
        SD_DAT,                             //    SD Card Data
        SD_DAT3,                                    //    SD Card Data 3
        SD_CMD,                             //    SD Card Command Signal
        SD_CLK,                             //    SD Card Clock
        ////////////////////// USB JTAG link  ////////////////////
        TDI,                                // CPLD -> FPGA (data in)
```

```
        TCK,                                // CPLD -> FPGA (clk)
        TCS,                                // CPLD -> FPGA (CS)
        TDO,                                // FPGA -> CPLD (data out)
        ////////////////// I2C         ////////////////////////////
        I2C_SDAT,                           //    I2C Data
        I2C_SCLK,                       //    I2C Clock
        ////////////////// PS2         ////////////////////////////
        PS2_DAT,                            //    PS2 Data
        PS2_CLK,                            //    PS2 Clock
        ////////////////// VGA         ////////////////////////////
        VGA_CLK,                            //    VGA Clock
        VGA_HS,                             //    VGA H_SYNC
        VGA_VS,                             //    VGA V_SYNC
        VGA_BLANK,                          //    VGA BLANK
        VGA_SYNC,                           //    VGA SYNC
        VGA_R,                              //    VGA Red[9:0]
        VGA_G,                              //    VGA Green[9:0]
        VGA_B,                                  //    VGA Blue[9:0]
        ////////////    Ethernet Interface  ////////////////////////
        ENET_DATA,                          //    DM9000A DATA bus 16Bits
        ENET_CMD,                           //    DM9000A    Command/Data    Select,    0    =
Command, 1 = Data
        ENET_CS_N,                          //    DM9000A Chip Select
        ENET_WR_N,                          //    DM9000A Write
        ENET_RD_N,                          //    DM9000A Read
        ENET_RST_N,                         //    DM9000A Reset
        ENET_INT,                           //    DM9000A Interrupt
        ENET_CLK,                           //    DM9000A Clock 25 MHz
        ////////////////    Audio CODEC     ////////////////////////
        AUD_ADCLRCK,                        //    Audio CODEC ADC LR Clock
        AUD_ADCDAT,                         //    Audio CODEC ADC Data
        AUD_DACLRCK,                        //    Audio CODEC DAC LR Clock
        AUD_DACDAT,                         //    Audio CODEC DAC Data
        AUD_BCLK,                           //    Audio CODEC Bit-Stream Clock
        AUD_XCK,                                //    Audio CODEC Chip Clock
        ////////////////    TV Decoder      ////////////////////////
        TD_DATA,                            //    TV Decoder Data bus 8 bits
        TD_HS,                              //    TV Decoder H_SYNC
        TD_VS,                              //    TV Decoder V_SYNC
        TD_RESET,                           //    TV Decoder Reset
        ////////////////// GPIO        ////////////////////////////
        GPIO_0,                             //    GPIO Connection 0
        GPIO_1,                             //    GPIO Connection 1
    );
//=============================================================================
// PORT declarations
//=============================================================================

////////////////////// Clock Input          ////////////////////////
input               CLOCK_27;               //    27 MHz
input               CLOCK_50;               //    50 MHz
input               EXT_CLOCK;              //    External Clock
////////////////////// Push Button          ////////////////////////
input   [3:0] KEY;                          //    Pushbutton[3:0]
////////////////////// DPDT Switch          ////////////////////////
input   [17:0]  SW;                         //    Toggle Switch[17:0]
////////////////////// 7-SEG Dispaly        ////////////////////////
output  [6:0] HEX0;                         //    Seven Segment Digit 0
```

```
output    [6:0] HEX1;                    //    Seven Segment Digit 1
output    [6:0] HEX2;                    //    Seven Segment Digit 2
output    [6:0] HEX3;                    //    Seven Segment Digit 3
output    [6:0] HEX4;                    //    Seven Segment Digit 4
output    [6:0] HEX5;                    //    Seven Segment Digit 5
output    [6:0] HEX6;                    //    Seven Segment Digit 6
output    [6:0] HEX7;                    //    Seven Segment Digit 7
//////////////////////////    LED    //////////////////////////
output    [8:0] LEDG;                    //    LED Green[8:0]
output    [17:0]LEDR;                    //    LED Red[17:0]
//////////////////////////    UART    //////////////////////////
output          UART_TXD;                //    UART Transmitter
input           UART_RXD;                //    UART Receiver
//////////////////////////    IRDA//////////////////////////
output          IRDA_TXD;                //    IRDA Transmitter
input           IRDA_RXD;                //    IRDA Receiver
//////////////////////        SDRAM Interface    //////////////////////
inout     [15:0]    DRAM_DQ;                    //    SDRAM Data bus 16 Bits
output[11:0]  DRAM_ADDR;                //    SDRAM Address bus 12 Bits
output          DRAM_LDQM;               //    SDRAM Low-byte Data Mask
output          DRAM_UDQM;                    //    SDRAM High-byte Data Mask
output          DRAM_WE_N;               //    SDRAM Write Enable
output          DRAM_CAS_N;                   //    SDRAM Column Address Strobe
output          DRAM_RAS_N;                   //    SDRAM Row Address Strobe
output          DRAM_CS_N;               //    SDRAM Chip Select
output          DRAM_BA_0;               //    SDRAM Bank Address 0
output          DRAM_BA_1;               //    SDRAM Bank Address 0
output          DRAM_CLK;                //    SDRAM Clock
output          DRAM_CKE;                //    SDRAM Clock Enable
//////////////////////  Flash Interface//////////////////////
inout           [7:0] FL_DQ;             //    FLASH Data bus 8 Bits
output    [21:0]FL_ADDR;                 //    FLASH Address bus 22 Bits
output          FL_WE_N;                      //    FLASH Write Enable
output          FL_RST_N;                //    FLASH Reset
output          FL_OE_N;                 //    FLASH Output Enable
output          FL_CE_N;                 //    FLASH Chip Enable
//////////////////////  SRAM Interface    //////////////////////
inout     [15:0]    SRAM_DQ;                    //    SRAM Data bus 16 Bits
output[17:0]  SRAM_ADDR;                //    SRAM Address bus 18 Bits
output          SRAM_UB_N;               //    SRAM High-byte Data Mask
output          SRAM_LB_N;               //    SRAM Low-byte Data Mask
output          SRAM_WE_N;               //    SRAM Write Enable
output          SRAM_CE_N;               //    SRAM Chip Enable
output          SRAM_OE_N;               //    SRAM Output Enable
////////////////////  ISP1362 Interface    //////////////////////
inout     [15:0]    OTG_DATA;                //    ISP1362 Data bus 16 Bits
output[1:0]       OTG_ADDR;                //    ISP1362 Address 2 Bits
output          OTG_CS_N;                //    ISP1362 Chip Select
output          OTG_RD_N;                //    ISP1362 Write
output          OTG_WR_N;                //    ISP1362 Read
output          OTG_RST_N;               //    ISP1362 Reset
output          OTG_FSPEED;              //    USB Full Speed,     0 = Enable, Z = Disable
output          OTG_LSPEED;              //    USB Low Speed,     0 = Enable, Z = Disable
input                OTG_INT0;                   //    ISP1362 Interrupt 0
input                OTG_INT1;                   //    ISP1362 Interrupt 1
input                OTG_DREQ0;                  //    ISP1362 DMA Request 0
input                OTG_DREQ1;                  //    ISP1362 DMA Request 1
output          OTG_DACK0_N;             //    ISP1362 DMA Acknowledge 0
```

```
output              OTG_DACK1_N;                //    ISP1362 DMA Acknowledge 1
////////////////////  LCD Module 16X2  ////////////////////////////
inout         [7:0] LCD_DATA;                   //    LCD Data bus 8 bits
output              LCD_ON;                     //    LCD Power ON/OFF
output              LCD_BLON;                   //    LCD Back Light ON/OFF
output              LCD_RW;                     //    LCD Read/Write Select, 0 = Write, 1 = Read
output              LCD_EN;                     //    LCD Enable
output              LCD_RS;                     //    LCD Command/Data Select, 0 = Command,
1 = Data
////////////////////  SD Card Interface   ////////////////////////
inout                   SD_DAT;                 //    SD Card Data
inout                   SD_DAT3;                //    SD Card Data 3
inout                   SD_CMD;                 //    SD Card Command Signal
output              SD_CLK;                     //    SD Card Clock
////////////////////////  I2C       ////////////////////////////////
inout                   I2C_SDAT;               //    I2C Data
output              I2C_SCLK;               //    I2C Clock
////////////////////////  PS2       ////////////////////////////////
input                   PS2_DAT;                //    PS2 Data
input                   PS2_CLK;                //    PS2 Clock
////////////////////  USB JTAG link  //////////////////////////////
input               TDI;                        // CPLD -> FPGA (data in)
input               TCK;                        // CPLD -> FPGA (clk)
input               TCS;                        // CPLD -> FPGA (CS)
output              TDO;                        // FPGA -> CPLD (data out)
////////////////////////  VGA           ////////////////////////////
output              VGA_CLK;                    //    VGA Clock
output              VGA_HS;                     //    VGA H_SYNC
output              VGA_VS;                     //    VGA V_SYNC
output              VGA_BLANK;                  //    VGA BLANK
output              VGA_SYNC;                   //    VGA SYNC
output    [9:0]     VGA_R;                  //    VGA Red[9:0]
output    [9:0]     VGA_G;                  //    VGA Green[9:0]
output    [9:0]     VGA_B;                  //    VGA Blue[9:0]
////////////////     Ethernet Interface  ////////////////////////////
inout     [15:0]    ENET_DATA;                  //    DM9000A DATA bus 16Bits
output              ENET_CMD;                   //    DM9000A   Command/Data   Select,   0   =
Command, 1 = Data
output              ENET_CS_N;                  //    DM9000A Chip Select
output              ENET_WR_N;                  //    DM9000A Write
output              ENET_RD_N;                  //    DM9000A Read
output              ENET_RST_N;                 //    DM9000A Reset
input                   ENET_INT;               //    DM9000A Interrupt
output              ENET_CLK;                   //    DM9000A Clock 25 MHz
////////////////////  Audio CODEC       ////////////////////////////
inout                   AUD_ADCLRCK;            //    Audio CODEC ADC LR Clock
input                   AUD_ADCDAT;             //    Audio CODEC ADC Data
inout                   AUD_DACLRCK;            //    Audio CODEC DAC LR Clock
output              AUD_DACDAT;                 //    Audio CODEC DAC Data
inout                   AUD_BCLK;               //    Audio CODEC Bit-Stream Clock
output              AUD_XCK;                    //    Audio CODEC Chip Clock
////////////////////  TV Devoder        ////////////////////////////
input         [7:0] TD_DATA;                    //    TV Decoder Data bus 8 bits
input                   TD_HS;                  //    TV Decoder H_SYNC
input                   TD_VS;                  //    TV Decoder V_SYNC
output              TD_RESET;                   //    TV Decoder Reset
////////////////////////  GPIO      ////////////////////////////////
inout     [35:0]    GPIO_0;                     //    GPIO Connection 0
```

```
inout     [35:0]    GPIO_1;                    //    GPIO Connection 1

assign    LCD_ON        =    1'b1;
assign    LCD_BLON      =    1'b1;

//    All inout port turn to tri-state
assign    DRAM_DQ           =    16'hzzzz;
assign    FL_DQ             =    8'hzz;
assign    SRAM_DQ           =    16'hzzzz;
assign    OTG_DATA          =    16'hzzzz;
assign    LCD_DATA          =    8'hzz;
assign    SD_DAT        =    1'bz;
assign    ENET_DATA     =    16'hzzzz;
assign    AUD_ADCLRCK       =    1'bz;
assign    AUD_DACLRCK       =    1'bz;
assign    AUD_BCLK          =    1'bz;
assign    GPIO_1        =    36'hzzzzzzzzz;
//=============================================================================
// REG/WIRE declarations
//=============================================================================
// Touch panel signal //
wire [7:0] ltm_r;          //    LTM Red Data 8 Bits
wire [7:0] ltm_g;          //    LTM Green Data 8 Bits
wire [7:0] ltm_b;          //    LTM Blue Data 8 Bits
wire       ltm_nclk; //    LTM Clcok
wire       ltm_hd;
wire       ltm_vd;
wire       ltm_den;
wire       ltm_grst;
// lcd 3wire interface//
wire       ltm_sclk;
wire       ltm_sda;
wire       ltm_scen;
wire            ltm_3wirebusy_n;
// Touch Screen Digitizer ADC
wire            adc_dclk;
wire            adc_cs;
wire            adc_penirq_n;
wire            adc_busy;
wire            adc_din;
wire            adc_dout;
wire            adc_ltm_sclk;
wire [11:0]     x_coord;
wire [11:0]     y_coord;
wire       new_coord;
wire touch_irq;
wire display_mode;
reg  [31:0]     div;
reg     [2:0] irq_num;
wire pll_c1;
wire [17:0] VGA_ADDR;
wire [15:0] VGA_DQ;
wire VGA_WE_N;
wire VGA_OE_N;
wire [10:0] x_cnt;
wire [9:0] y_cnt;
wire [31:0]Panel_command;
wire OverridePANEL;
```

```
wire [17:0]PANEL_ADDR;
wire [31:0]Mole_command;
wire OverrideMOLE;
wire [17:0]MOLE_ADDR;
wire [11:0] x_coord1;
wire [11:0] y_coord1;
wire [3:0] state;
wire clk_18;
wire irq;
reg [1:0] interrupt;

////////////// GPIO_O /////////////////
assign      adc_penirq_n    =GPIO_0[0];
assign      adc_dout        =GPIO_0[1];
assign      adc_busy        =GPIO_0[2];
assign      GPIO_0[3]       =adc_din;
assign      GPIO_0[4]       =adc_ltm_sclk;
assign      GPIO_0[5]       =ltm_b[3];
assign      GPIO_0[6]       =ltm_b[2];
assign      GPIO_0[7]       =ltm_b[1];
assign      GPIO_0[8]       =ltm_b[0];
assign      GPIO_0[9]       =ltm_nclk;
assign      GPIO_0[10]      =ltm_den;
assign      GPIO_0[11]      =ltm_hd;
assign      GPIO_0[12]      =ltm_vd;
assign      GPIO_0[13]      =ltm_b[4];
assign      GPIO_0[14]      =ltm_b[5];
assign      GPIO_0[15]      =ltm_b[6];
assign      GPIO_0[16]      =ltm_b[7];
assign      GPIO_0[17]      =ltm_g[0];
assign      GPIO_0[18]      =ltm_g[1];
assign      GPIO_0[19]      =ltm_g[2];
assign      GPIO_0[20]      =ltm_g[3];
assign      GPIO_0[21]      =ltm_g[4];
assign      GPIO_0[22]      =ltm_g[5];
assign      GPIO_0[23]      =ltm_g[6];
assign      GPIO_0[24]      =ltm_g[7];
assign      GPIO_0[25]      =ltm_r[0];
assign      GPIO_0[26]      =ltm_r[1];
assign      GPIO_0[27]      =ltm_r[2];
assign      GPIO_0[28]      =ltm_r[3];
assign      GPIO_0[29]      =ltm_r[4];
assign      GPIO_0[30]      =ltm_r[5];
assign      GPIO_0[31]      =ltm_r[6];
assign      GPIO_0[32]      =ltm_r[7];
assign      GPIO_0[33]      =ltm_grst;
assign      GPIO_0[34]      =ltm_scen;
assign      GPIO_0[35]      =ltm_sda;

assign adc_ltm_sclk= ( adc_dclk & ltm_3wirebusy_n )    |    ( ~ltm_3wirebusy_n & ltm_sclk );
assign ltm_nclk = div[0]; // 25 Mhz
assign ltm_grst = KEY[0];

assign LEDR[17] = display_mode;
assign LEDR[16] = irq;
assign LEDR[15] = irq_num[2];
assign LEDR[14] = irq_num[1];
assign LEDR[13] = irq_num[0];
```

```
assign VGA_R[9] = ltm_r[7];
assign VGA_R[8] = ltm_r[6];
assign VGA_R[7] = ltm_r[5];
assign VGA_R[6] = ltm_r[4];
assign VGA_R[5] = ltm_r[3];
assign VGA_R[4] = ltm_r[2];
assign VGA_R[3] = ltm_r[1];
assign VGA_R[2] = ltm_r[0];
assign VGA_R[1] = 0;
assign VGA_R[0] = 0;

assign VGA_B[9] = ltm_b[7];
assign VGA_B[8] = ltm_b[6];
assign VGA_B[7] = ltm_b[5];
assign VGA_B[6] = ltm_b[4];
assign VGA_B[5] = ltm_b[3];
assign VGA_B[4] = ltm_b[2];
assign VGA_B[3] = ltm_b[1];
assign VGA_B[2] = ltm_b[0];
assign VGA_B[1] = 0;
assign VGA_B[0] = 0;

assign VGA_G[9] = ltm_g[7];
assign VGA_G[8] = ltm_g[6];
assign VGA_G[7] = ltm_g[5];
assign VGA_G[6] = ltm_g[4];
assign VGA_G[5] = ltm_g[3];
assign VGA_G[4] = ltm_g[2];
assign VGA_G[3] = ltm_g[1];
assign VGA_G[2] = ltm_g[0];
assign VGA_G[1] = 0;
assign VGA_G[0] = 0;

assign      VGA_HS   =ltm_hd;
assign      VGA_VS   =ltm_vd;
assign      VGA_CLK    = ltm_nclk;
assign      VGA_SYNC = 0;

always @(posedge pll_c1)
      begin
            div <= div+1;
      end

always@(posedge pll_c1)
begin
if(touch_irq)
begin
irq_num <= irq_num +1;
interrupt <= interrupt +1;
end
else
begin
irq_num <= irq_num;
interrupt <= irq_num;
end
end
```

```
de2_i2c_av_config de2_i2c_av_config1 (
      .iCLK(pll_c1),
      .iRST_N(1'b1),
      .I2C_SCLK(I2C_SCLK),
      .I2C_SDAT(I2C_SDAT)
   );

double_pll pll1(
      .inclk0(CLOCK_50),
      .c0(DRAM_CLK),
      .c1(pll_c1),
      .c2(clk_18));

SEG7_LUT_8        u1   (
                       .oSEG0(HEX0),
                       .oSEG1(HEX1),
                       .oSEG2(HEX2),
                       .oSEG3(HEX3),
                       .oSEG4(HEX4),
                       .oSEG5(HEX5),
                       .oSEG6(HEX6),
                       .oSEG7(HEX7),
                       .iDIG({ 4'h0 , x_coord , 4'h0 , y_coord }),
                       .ON_OFF(8'b01110111)
                       );

// lcd 3 wire interface configuration    //
lcd_spi_cotroller    u2   (
                       // Host Side
                       .iCLK(pll_c1),
                       .iRST_n(DLY0),
                       // 3wire Side
                       .o3WIRE_SCLK(ltm_sclk),
                       .io3WIRE_SDAT(ltm_sda),
                       .o3WIRE_SCEN(ltm_scen),
                       .o3WIRE_BUSY_n(ltm_3wirebusy_n)
                       );

// system reset    //
Reset_Delay          u3   (.iCLK(pll_c1),
                       .iRST(KEY[0]),
                       .oRST_0(DLY0),
                       .oRST_1(DLY1),
                       .oRST_2(DLY2)
                       );

// Touch Screen Digitizer ADC configuration //
adc_spi_controller  u4   (
                       .iCLK(pll_c1),
                       .iRST_n(DLY0),
                       .oADC_DIN(adc_din),
                       .oADC_DCLK(adc_dclk),
                       .oADC_CS(adc_cs),
                       .iADC_DOUT(adc_dout),
                       .iADC_BUSY(adc_busy),
                       .iADC_PENIRQ_n(adc_penirq_n),
```

```
                        .oTOUCH_IRQ(touch_irq),
                        .oX_COORD(x_coord),
                        .oY_COORD(y_coord),
                        .oNEW_COORD(new_coord),
                        );

touch_irq_detector detector1(
                        .clk(pll_c1),
                        .reset_n(DLY0),
                        .iTOUCH_IRQ(touch_irq),
                        .iX_COORD(x_coord),
                        .iY_COORD(y_coord),
                        .iNEW_COORD(new_coord),
                        .oDISPLAY_MODE(display_mode)
                        );

single_clk_irq single_clk_irq1(
                        .clk(pll_c1),
                        .reset_n(DLY0),
                        .idisplay_mode(display_mode),
                        .irq(irq));

lcd_controller u5(
        .clk(pll_c1),
        .clk_ltm(ltm_nclk),
        .reset_n(DLY2),
        .iMOLECTRL(Mole_command),
        .iPANELCTRL(Panel_command),
        .oHD(ltm_hd),                   // LCD Horizontal sync
        .oVD(ltm_vd),                   // LCD Vertical sync
        .oDEN(ltm_den),                     // LCD Data Enable
        .oLCD_R(ltm_r),                     // LCD Red color data
        .oLCD_G(ltm_g),                   // LCD Green color data
        .oLCD_B(ltm_b),                   // LCD Blue color data
        .oVGA_ADDR(VGA_ADDR),
        .oVGA_WE_N(VGA_WE_N),
        .oVGA_OE_N(VGA_OE_N),
        .iVGA_DQ(VGA_DQ)
        );

assign LEDG[0] = Mole_command[0];
assign LEDG[1] = Mole_command[1];
assign LEDG[2] = Mole_command[2];
assign LEDG[3] = Mole_command[3];
assign LEDG[4] = Mole_command[8];
assign LEDG[5] = Mole_command[9];
assign LEDG[6] = Mole_command[10];
assign LEDG[7] = Mole_command[11];


nios_system DUT
    (
        .AUD_ADCDAT_to_the_musiccontroller_0          (AUD_ADCDAT),
      .AUD_ADCLRCK_from_the_musiccontroller_0      (AUD_ADCLRCK),
      .AUD_BCLK_to_and_from_the_musiccontroller_0 (AUD_BCLK),
      .AUD_DACDAT_from_the_musiccontroller_0       (AUD_DACDAT),
      .AUD_DACLRCK_from_the_musiccontroller_0      (AUD_DACLRCK),
        .AUD_XCK_from_the_musiccontroller_0          (AUD_XCK),
```

```
        .SRAM_ADDR_from_the_sram_mux_0                  (SRAM_ADDR),
        .SRAM_CE_N_from_the_sram_mux_0                  (SRAM_CE_N),
        .SRAM_DQ_to_and_from_the_sram_mux_0             (SRAM_DQ),
        .SRAM_LB_N_from_the_sram_mux_0                  (SRAM_LB),
        .SRAM_OE_N_from_the_sram_mux_0                  (SRAM_OE_N),
        .SRAM_UB_N_from_the_sram_mux_0                  (SRAM_UB_N),
        .SRAM_WE_N_from_the_sram_mux_0                  (SRAM_WE_N),
        .VGA_ADDR_to_the_sram_mux_0                     (VGA_ADDR),
        .VGA_DQ_from_the_sram_mux_0                     (VGA_DQ),
        .VGA_OE_N_to_the_sram_mux_0                     (VGA_OE_N),
        .VGA_WE_N_to_the_sram_mux_0                     (VGA_WE_N),
        .clk_0                                          (pll_c1),
            .clk_18_to_the_musiccontroller_0          (clk_18),
        .iX_COORD_to_the_xycoord_interface_0          (x_coord),
        .iY_COORD_to_the_xycoord_interface_0          (y_coord),
           .irq_adc_to_the_interrupt_0                (display_mode),
        .oMOLECTRL_from_the_command_0                       (Mole_command),
        .oPANELCTRL_from_the_command_0                  (Panel_command),
        .reset_n                                        (DLY0),
           .zs_addr_from_the_sdram_0                    (DRAM_ADDR),
        .zs_ba_from_the_sdram_0                         ({DRAM_BA_1,DRAM_BA_0}),
        .zs_cas_n_from_the_sdram_0                      (DRAM_CAS_N),
        .zs_cke_from_the_sdram_0                        (DRAM_CKE),
        .zs_cs_n_from_the_sdram_0                       (DRAM_CS_N),
        .zs_dq_to_and_from_the_sdram_0                  (DRAM_DQ),
        .zs_dqm_from_the_sdram_0                        ({DRAM_UDQM,DRAM_LDQM}),
        .zs_ras_n_from_the_sdram_0                      (DRAM_RAS_N),
        .zs_we_n_from_the_sdram_0                       (DRAM_WE_N)
    );
endmodule
```

interrupt.v

```
module interrupt(
                clk,
                reset_n,
                chipselect,
                read,
                write,
                address,
                readdata,
                writedata,
                irq,
                irq_adc
                );

//================================
//IO PORT
//================================
input clk;
input reset_n;
input chipselect;
input read;
input write;
input [4:0] address;
```

```
output [31:0] readdata;
input [31:0] writedata;
output irq;
input irq_adc;
//==================================
//REG and WIRE
//==================================
reg irq;


//==================================
//STRUCTURE LOGIC
//==================================
always@(posedge clk or negedge reset_n)
begin
	if(!reset_n)
		begin
		irq <= 0;
		end
	else if(irq_adc == 1)
		irq <= 1;
	else if(write && chipselect)
		irq <= 0;
end

endmodule
```

irq_gen.v

```
module irq_gen(
			iclk,
			ireset,
			xcoord,
			ycoord,
			irq);

input iclk;
input ireset;
input [11:0] xcoord;
input [11:0] ycoord;
output irq;

reg [11:0] prex;
reg [11:0] prey;
reg irq;

always@(posedge iclk or negedge ireset)
begin
	if(!ireset)
	begin
		irq <= 0;
		prex<= 0;
		prey <= 0;
	end
	else
	begin
```

```
            if((prex != xcoord)|| (prey != ycoord))
            begin
                  irq <= 1;
                  prex<= xcoord;
                  prey <= ycoord;
            end
            else
                  irq <=0;
      end
end

endmodule
```

lcd_controller.v

```
module lcd_controller(
            clk, //50M
            clk_ltm, //25M
            reset_n,
            iMOLECTRL,
            iPANELCTRL,
            oHD,                        // LCD Horizontal sync
            oVD,                  // LCD Vertical sync
            oDEN,                       // LCD Data Enable
            oLCD_R,                     // LCD Red color data
            oLCD_G,                     // LCD Green color data
            oLCD_B,                     // LCD Blue color data
            oVGA_ADDR,
            oVGA_WE_N,
            oVGA_OE_N,
            iVGA_DQ,
            );

//=============================================================================
// PARAMETER declarations
//=============================================================================
parameter H_LINE = 1056;
parameter V_LINE = 525;
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
parameter Vertical_Front_Porch = 10;
//=============================================================================

////IO PORT DECLARATION
//=============================================================================
input clk;
input clk_ltm;
input reset_n;
input [31:0] iMOLECTRL;
input [31:0] iPANELCTRL;
output     [7:0] oLCD_R;
output    [7:0]  oLCD_G;
output    [7:0]  oLCD_B;
output     oHD;
output     oVD;
```

```
output     oDEN;
output [17:0] oVGA_ADDR;
output oVGA_WE_N;
output oVGA_OE_N;
input [15:0]iVGA_DQ;


///reg and wire
reg         [10:0]    x_cnt;
reg         [9:0] y_cnt;
wire [7:0] mred;
wire [7:0] mgreen;
wire [7:0] mblue;
wire                display_area;
reg                       mhd;
reg                       mvd;
reg                       mden;
reg                       oHD;
reg                       oVD;
reg                       oDEN;
reg         [7:0] oLCD_R;
reg         [7:0] oLCD_G;
reg         [7:0] oLCD_B;
reg         [7:0] red_1;
reg   [7:0] green_1;
reg   [7:0] blue_1;

reg [17:0] BACK_ADDR;
wire [17:0] WELCOME_ADDR;
wire [17:0] PLAY_ADDR;
wire [17:0] WIN_ADDR;
wire [17:0] LOSE_ADDR;
reg [17:0] address;
reg [3:0] state;
reg [31:0] mole_ctrl;
reg [31:0] panel_ctrl;

assign oVGA_ADDR = BACK_ADDR;
assign oVGA_WE_N = 1'b0;
assign oVGA_OE_N = display_area ? 1'b1 : 1'b0;
//assign state = iPANELCTRL[3:0];

always@(posedge clk_ltm or negedge reset_n)
      begin
            if (!reset_n)
            begin
            state <= 4'b0;
            mole_ctrl <= 32'b0;
            panel_ctrl <= 32'b0;
            end
            else if(mvd == 1)
            begin
            state <= iPANELCTRL[3:0];
            mole_ctrl <= iMOLECTRL;
            panel_ctrl <= iPANELCTRL;
            end
            else
            begin
```

```
            state <= state;
            mole_ctrl <= mole_ctrl;
            panel_ctrl <= panel_ctrl;
            end
      end

// This signal indicate the lcd display area .
assign      display_area = ((x_cnt>(Hsync_Blank-1)&& //>215
                              (x_cnt<(H_LINE-Hsync_Front_Porch))&& //< 1016
                              (y_cnt>(Vertical_Back_Porch-1))&&
                              (y_cnt<(V_LINE - Vertical_Front_Porch))
                              ))    ? 1'b1 : 1'b0;


////////////////////////// x    y counter    and lcd hd generator ///////////////////
always@(posedge clk_ltm or negedge reset_n)
      begin
            if (!reset_n)
            begin
                  x_cnt <= 11'd0;
                  mhd    <= 1'd0;
            end
            else if (x_cnt == (H_LINE-1))
            begin
                  x_cnt <= 11'd0;
                  mhd    <= 1'd0;
            end
            else
            begin
                  x_cnt <= x_cnt + 11'd1;
                  mhd    <= 1'd1;
            end
      end

always@(posedge clk_ltm or negedge reset_n)
      begin
            if (!reset_n)
                  y_cnt <= 10'd0;
            else if (x_cnt == (H_LINE-1))
            begin
                  if (y_cnt == (V_LINE-1))
                        y_cnt <= 10'd0;
                  else
                        y_cnt <= y_cnt + 10'd1;
            end
      end
////////////////////////////// touch panel timing ///////////////////

always@(posedge clk_ltm    or negedge reset_n)
      begin
            if (!reset_n)
                  mvd    <= 1'b1;
            else if (y_cnt == 10'd0)
                  mvd    <= 1'b0;
            else
                  mvd    <= 1'b1;
      end
```

```
always@(posedge clk_ltm    or negedge reset_n)
      begin
            if (!reset_n)
                  mden    <= 1'b0;
            else if (display_area)
                  mden    <= 1'b1;
            else
                  mden    <= 1'b0;
      end

//=============================================================
//Assigning Address=============================================
//=============================================================
always@(posedge clk_ltm or negedge reset_n)
begin
      if(!reset_n)
            BACK_ADDR <= 18'bZ;
      else if (state == 4'b0000 || state==4'b0001 || state ==4'b0010 || state == 4'b0011)
            BACK_ADDR <= WELCOME_ADDR;
      else if (state == 4'b0100 || state==4'b0101 || state ==4'b0110 || state == 4'b0111)
            BACK_ADDR <= PLAY_ADDR;
      else if (state == 4'b1000 || state==4'b1001 || state ==4'b1010 || state == 4'b1011)
            BACK_ADDR <= WIN_ADDR;
      else if (state == 4'b1100 || state==4'b1101 || state ==4'b1110 || state == 4'b1111)
            BACK_ADDR <= LOSE_ADDR;
end




//=============================================================
//Welcome Mode==================================================
//=============================================================
welcome welcome1(
                        .iclk(clk_ltm),
                        .ireset_n(reset_n),
                        .ix_cnt(x_cnt),
                        .iy_cnt(y_cnt),
                        .istate(state),
                        .oADDR(WELCOME_ADDR));

//=============================================================
//Running Mode==================================================
//=============================================================
play play1(
                        .iclk(clk_ltm),
                        .ireset_n(reset_n),
                        .ix_cnt(x_cnt), // input from lcd controlelr
                        .iy_cnt(y_cnt), // input from lcd controller
                        .iPANELCTRL(panel_ctrl), // command from nios containing 32 bits
                        .iMOLECTRL(mole_ctrl),
                        .oADDR(PLAY_ADDR), //the output address to the lcd controller
                              );
//=============================================================
//Win Mode======================================================
//=============================================================
win win1(
                        .iclk(clk_ltm),
```

```
                        .ireset_n(reset_n),
                        .ix_cnt(x_cnt),
                        .iy_cnt(y_cnt),
                        .oADDR(WIN_ADDR));
//=============================================================
//Lose Mode=================================================
//=============================================================
lose lose1(
                        .iclk(clk_ltm),
                        .ireset_n(reset_n),
                        .ix_cnt(x_cnt),
                        .iy_cnt(y_cnt),
                        .oADDR(LOSE_ADDR));

//=============================================================
//OUTPUT LOGIC==============================================
//=============================================================
always@(posedge clk_ltm or negedge reset_n)
      begin
            if (!reset_n)
                  begin
                  red_1 <= 8'd255;
                  green_1 <= 8'd255;
                  blue_1 <= 8'd255;
                  end
            else
                  begin
                  red_1 <= (iVGA_DQ[15:11]<<3);
                  green_1 <= (iVGA_DQ[10:5]<<2);
                  blue_1 <= (iVGA_DQ[4:0]<<3);
                  end
      end

///Assign RGB to OUPUT BLOCK
assign mred = red_1;
assign mgreen = green_1;
assign mblue    = blue_1;

////////////////////////////////////OUTPUT BLOCK///    ///////////////
always@(posedge clk_ltm or negedge reset_n)
      begin
            if (!reset_n)
                  begin
                        oHD <= 1'd0;
                        oVD <= 1'd0;
                        oDEN <= 1'd0;
                        oLCD_R <= 8'd0;
                        oLCD_G <= 8'd0;
                        oLCD_B <= 8'd0;
                  end
            else
                  begin
                        oHD <= mhd;
                        oVD <= mvd;
                        oDEN <= display_area;
                        oLCD_R <= mred;
                        oLCD_G <= mgreen;
                        oLCD_B <= mblue;
```

```
                end
        end

endmodule
```

lcd_spi_controller.v

```
// --------------------------------------------------------------------

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// --------------------------------------------------------------------

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//     consistency and functionality through the use of formal

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//

// --------------------------------------------------------------------

//

//                                 Terasic Technologies Inc

//                                 356 Fu-Shin E. Rd Sec. 1. JhuBei City,

//                                 HsinChu County, Taiwan
```

```
//                              302
//
//                              web: http://www.terasic.com/
//                              email: support@terasic.com
//
// ---------------------------------------------------------------------
//
// Major Functions: This function will transmit the lcd register setting
//
// ---------------------------------------------------------------------
//
// Revision History :
// ---------------------------------------------------------------------
//     Ver   :| Author                    :| Mod. Date :| Changes Made:
//     V1.0 :| Johnny Fan                 :| 07/06/30   :| Initial Revision
// ---------------------------------------------------------------------
module lcd_spi_cotroller (//  Host Side
                          iCLK,
                          iRST_n,
                          //    3wire interface side
                          o3WIRE_SCLK,
                          io3WIRE_SDAT,
                          o3WIRE_SCEN,
                          o3WIRE_BUSY_n
                          );
//=============================================================================
// PARAMETER declarations
//=============================================================================
```

```
parameter      LUT_SIZE =      20; // Total setting register numbers
//=============================================================================
// PORT declarations
//=============================================================================
//     Host Side
output          o3WIRE_BUSY_n;
input           iCLK;
input           iRST_n;
//     3wire interface side
output          o3WIRE_SCLK;
inout           io3WIRE_SDAT;
output          o3WIRE_SCEN;
//     Internal Registers/Wires
//=============================================================================
// REG/WIRE declarations
//=============================================================================
reg             m3wire_str;
wire        m3wire_rdy;
wire        m3wire_ack;
wire        m3wire_clk;
reg   [15:0]    m3wire_data;
reg   [15:0]    lut_data;
reg   [5:0] lut_index;
reg   [3:0] msetup_st;
reg             o3WIRE_BUSY_n;
wire        v_reverse; // display Vertical reverse function
wire        h_reverse; // display Horizontal reverse function
wire [9:0] g0;
wire [9:0] g1;
```

```
wire [9:0] g2;
wire [9:0] g3;
wire [9:0] g4;
wire [9:0] g5;
wire [9:0] g6;
wire [9:0] g7;
wire [9:0] g8;
wire [9:0] g9;
wire [9:0] g10;
wire [9:0] g11;

//=============================================================================
// Structural coding
//=============================================================================

assign      h_reverse = 1'b1;
assign      v_reverse = 1'b0;

three_wire_controller    u0   (      //     Host Side
                                 .iCLK(iCLK),
                                 .iRST(iRST_n),
                                 .iDATA(m3wire_data),
                                 .iSTR(m3wire_str),
                                 .oACK(m3wire_ack),
                                 .oRDY(m3wire_rdy),
                                 .oCLK(m3wire_clk),
                                 //     Serial Side
                                 .oSCEN(o3WIRE_SCEN),
                                 .SDA(io3WIRE_SDAT),
```

```
                .oSCLK(o3WIRE_SCLK)
            );
//////////////////////  Config Control //////////////////////////
always@(posedge m3wire_clk or negedge iRST_n)
begin
    if(!iRST_n)
    begin
        lut_index <=  0;
        msetup_st   <=  0;
        m3wire_str  <=  0;
        o3WIRE_BUSY_n  <=  0;
    end
    else
    begin
        if(lut_index<LUT_SIZE)
        begin
        o3WIRE_BUSY_n  <=  0;
            case(msetup_st)
            0:  begin
                    msetup_st   <=  1;
                end
            1:  begin
                    msetup_st   <=  2;
                end

            2:  begin
                    m3wire_data <=  lut_data;
                    m3wire_str  <=  1;
                    msetup_st   <=  3;
```

```
                    end
                3:  begin
                        if(m3wire_rdy)
                        begin
                            if(m3wire_ack)
                            msetup_st     <=  4;
                            else
                            msetup_st     <=  0;
                            m3wire_str    <=  0;
                        end
                    end
                4:  begin
                        lut_index <=  lut_index+1;
                        msetup_st     <=  0;
                    end
                endcase
            end
            else            o3WIRE_BUSY_n   <=  1;
        end
end

assign    g0 =106;
assign    g1 =200;
assign    g2 =289;
assign    g3 =375;
assign    g4 =460;
assign    g5 =543;
assign    g6 =625;
assign    g7 =705;
```

```
assign     g8 =785;

assign     g9 =864;

assign     g10 = 942;

assign     g11 = 1020;


////////////////////     Config Data LUT        ////////////////////////

always

begin

      case(lut_index)


      0          :     lut_data  <=   {6'h11,2'b01,g0[9:8],g1[9:8],g2[9:8],g3[9:8]};

      1          :     lut_data  <=   {6'h12,2'b01,g4[9:8],g5[9:8],g6[9:8],g7[9:8]};

      2          :     lut_data  <=   {6'h13,2'b01,g8[9:8],g9[9:8],g10[9:8],g11[9:8]};

      3          :     lut_data  <=   {6'h14,2'b01,g0[7:0]};

      4          :     lut_data  <=   {6'h15,2'b01,g1[7:0]};

      5          :     lut_data  <=   {6'h16,2'b01,g2[7:0]};

      6          :     lut_data  <=   {6'h17,2'b01,g3[7:0]};

      7          :     lut_data  <=   {6'h18,2'b01,g4[7:0]};

      8          :     lut_data  <=   {6'h19,2'b01,g5[7:0]};

      9          :     lut_data  <=   {6'h1a,2'b01,g6[7:0]};

      10         :     lut_data  <=   {6'h1b,2'b01,g7[7:0]};

      11         :     lut_data  <=   {6'h1c,2'b01,g8[7:0]};

      12         :     lut_data  <=   {6'h1d,2'b01,g9[7:0]};

      13         :     lut_data  <=   {6'h1e,2'b01,g10[7:0]};

      14         :     lut_data  <=   {6'h1f,2'b01,g11[7:0]};

      15         :     lut_data  <=   {6'h20,2'b01,4'hf,4'h0};

      16         :     lut_data  <=   {6'h21,2'b01,4'hf,4'h0};

      17         :     lut_data  <=   {6'h03, 2'b01, 8'hdf};

      18         :     lut_data  <=   {6'h02, 2'b01, 8'h07};
```

```
    19      :   lut_data  <=  {6'h04, 2'b01, 6'b000101,!v_reverse,!h_reverse};
    default :   lut_data  <=  16'h0000;
    endcase
end
////////////////////////////////////////////////////////////////////

endmodule
```

lcd_timing_controller.v

```
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//   This VHDL/Verilog or C/C++ source code is intended as a design reference
//   which illustrates how these types of functions can be implemented.
//   It is the user's responsibility to verify their design for
//   consistency and functionality through the use of formal
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//
```

```
// --------------------------------------------------------------------
//
//                          Terasic Technologies Inc
//                          356 Fu-Shin E. Rd Sec. 1. JhuBei City,
//                          HsinChu County, Taiwan
//                          302
//
//                          web: http://www.terasic.com/
//                          email: support@terasic.com
//
// --------------------------------------------------------------------
//
// Major Functions: DE2 LTM module Timing control and color pattern
//                          generator
//
// --------------------------------------------------------------------
//
// Revision History :
// --------------------------------------------------------------------
//     Ver  :| Author                :| Mod. Date :| Changes Made:
//     V1.0 :| Johnny Fan            :| 07/06/30  :| Initial Revision
// --------------------------------------------------------------------
module lcd_timing_controller        (
                                    clk,            // LCD display clock
                                    reset_n,        // systen reset
                                    read,
                                    write,
                                    chipselect,
                                    address,
```

```
                        readdata,
                        writedata,
                        //LCD SIDE
                        oHD,                    // LCD Horizontal sync
                        oVD,                  // LCD Vertical sync
                        oDEN,                   // LCD Data Enable
                        oLCD_R,                 // LCD Red color data
                        oLCD_G,                 // LCD Green color data
                        oLCD_B,                 // LCD Blue color data
                        oVGA_ADDR,
                        oVGA_WE_N,
                        oVGA_OE_N,
                        iVGA_DQ,
                        iDISPLAY_MODE
                        );
//=============================================================================
// PARAMETER declarations
//=============================================================================
parameter H_LINE = 1056;
parameter V_LINE = 525;
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
parameter Vertical_Front_Porch = 10;
//=============================================================================
// PORT declarations
//=============================================================================
input           clk;
input           reset_n;
```

```
input              read;
input              write;
input              chipselect;
input [4:0]address;
output [15:0]readdata;
input [15:0]writedata;
output     [7:0] oLCD_R;
output    [7:0]  oLCD_G;
output    [7:0]  oLCD_B;
output                   oHD;
output                   oVD;
output                   oDEN;
input       [1:0] iDISPLAY_MODE;
output [17:0] oVGA_ADDR;
output oVGA_WE_N;
output oVGA_OE_N;
input [15:0] iVGA_DQ;
//=============================================================================
// REG/WIRE declarations
//=============================================================================
reg          [10:0]    x_cnt;
reg          [9:0] y_cnt;
wire [7:0] mred;
wire [7:0] mgreen;
wire [7:0] mblue;
wire               display_area;
reg                      mhd;
reg                      mvd;
reg                      mden;
```

```
reg                 oHD;
reg                 oVD;
reg                 oDEN;
reg       [7:0] oLCD_R;
reg       [7:0] oLCD_G;
reg       [7:0] oLCD_B;
wire [1:0] msel;
reg       [7:0] red_1;
reg   [7:0] green_1;
reg   [7:0] blue_1;
reg   [7:0] graycnt;
reg       [7:0] pattern_data;
reg [31:0] div;
wire [15:0] area;
reg [23:0]oRGB_DATA; //information containing mole state
reg [2:0]mole0;
reg [2:0]mole1;
reg [2:0]mole2;
reg [2:0]mole3;
reg [2:0]mole4;
reg [2:0]mole5;
reg [2:0]mole6;
reg [2:0]mole7;
reg [2:0]mole8;
reg [2:0]mole9;
wire [7:0]LED1_R;
wire [7:0]LED1_G;
wire [7:0]LED1_B;
wire [7:0]LED2_R;
```

```
wire [7:0]LED2_G;

wire [7:0]LED2_B;

wire [7:0]LED0_R;

wire [7:0]LED0_G;

wire [7:0]LED0_B;

wire [2:0]oOVERRIDE;

reg [3:0] inumber_s;

reg [3:0] inumber_ts;

reg [3:0] inumber_min;

reg [26:0] counter;


wire [3:0] num_input_s;

wire [3:0] num_input_ts;

wire [3:0] num_input_min;

wire [26:0] oCNT;

wire flag1;

wire flag2;

wire clk_ltm;

assign clk_ltm = div[0]; // 25 Mhz

reg [14:0] area_counter[0:14];

//=============================================================================

// Structural coding

//=============================================================================

always @(posedge clk)

	begin

		div <= div+1;

	end


// This signal indicate the lcd display area .
```

```
assign      display_area = ((x_cnt>(Hsync_Blank-1)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0;



////////////////////////// x    y counter    and lcd hd generator //////////////////

always@(posedge clk_ltm or negedge reset_n)
      begin
            if (!reset_n)
            begin
                  x_cnt <= 11'd0;
                  mhd    <= 1'd0;
            end
            else if (x_cnt == (H_LINE-1))
            begin
                  x_cnt <= 11'd0;
                  mhd    <= 1'd0;
            end
            else
            begin
                  x_cnt <= x_cnt + 11'd1;
                  mhd    <= 1'd1;
            end
      end


always@(posedge clk_ltm or negedge reset_n)
      begin
```

```
        if (!reset_n)
            y_cnt <= 10'd0;
        else if (x_cnt == (H_LINE-1))
        begin
            if (y_cnt == (V_LINE-1))
                y_cnt <= 10'd0;
            else
                y_cnt <= y_cnt + 10'd1;
        end
    end
////////////////////////////// touch panel timing ///////////////////

always@(posedge clk_ltm   or negedge reset_n)
    begin
        if (!reset_n)
            mvd   <= 1'b1;
        else if (y_cnt == 10'd0)
            mvd   <= 1'b0;
        else
            mvd   <= 1'b1;
    end

always@(posedge clk_ltm   or negedge reset_n)
    begin
        if (!reset_n)
            mden   <= 1'b0;
        else if (display_area)
            mden   <= 1'b1;
        else
```

```
            mden    <= 1'b0;
    end



//Detect which area you are in// 0~14 different areas//offset corrected
assign area[0] = ((x_cnt>(Hsync_Blank-2+400)&& //>214
                        (x_cnt<(H_LINE-Hsync_Front_Porch-1-200))&& //< 1015
                        (y_cnt>(Vertical_Back_Porch-1))&&
                        (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                        ))    ? 1'b1 : 1'b0 ; //mole0
assign area[1] = ((x_cnt>(Hsync_Blank-2+200)&& //>215
                        (x_cnt<(H_LINE-Hsync_Front_Porch-1-400))&& //< 1016
                        (y_cnt>(Vertical_Back_Porch-1))&&
                        (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                        ))    ? 1'b1 : 1'b0;//mole1
assign area[2] = ((x_cnt>(Hsync_Blank-2)&& //>215
                        (x_cnt<(H_LINE-Hsync_Front_Porch-1-600))&& //< 1016
                        (y_cnt>(Vertical_Back_Porch-1))&&
                        (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                        ))    ? 1'b1 : 1'b0 ;//mole2
assign area[3] = ((x_cnt>(Hsync_Blank-2+400)&& //>215
                        (x_cnt<(H_LINE-Hsync_Front_Porch-1-200))&& //< 1016
                        (y_cnt>(Vertical_Back_Porch-1+160))&&
                        (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                        ))    ? 1'b1 : 1'b0 ;    //mole3
assign area[4] = ((x_cnt>(Hsync_Blank-2+200)&& //>215
                        (x_cnt<(H_LINE-Hsync_Front_Porch-1-400))&& //< 1016
                        (y_cnt>(Vertical_Back_Porch-1+160))&&
```

```
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                                ))    ? 1'b1 : 1'b0 ; //mole4
assign area[5] = ((x_cnt>(Hsync_Blank-2)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-600))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                                ))    ? 1'b1 : 1'b0 ;//mole5
assign area[6] = ((x_cnt>(Hsync_Blank-2+400)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-200))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0 ;    //mole6
assign area[7] = ((x_cnt>(Hsync_Blank-2+200)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-400))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0; //mole7
assign area[8] = ((x_cnt>(Hsync_Blank-2)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-600))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0 ;//mole8
assign area[9] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-400))
                                ))    ? 1'b1 : 1'b0 ;//area 9 Time
assign area[10] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
```

```
                                (y_cnt>(Vertical_Back_Porch-1+80))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                                ))    ? 1'b1 : 1'b0 ;//area 10 life
assign area[11] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-240))
                                ))    ? 1'b1 : 1'b0 ;//area 11 score
assign area[12] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+240))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                                ))    ? 1'b1 : 1'b0 ;//area 12 start/pause
assign area[13] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-80))
                                ))    ? 1'b1 : 1'b0 ;//area 13 exit
assign area[14] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+400))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0 ;//area 14 label
assign area[15] = 1'b0;
//area 15 is the logo of the team defalt black

//////////////////////Timmer//////////////////////////
No_GEN LED0(
                        .iclk(clk_ltm),
```

```
                .iReset_n(reset_n),
                .ixcount(x_cnt),
                .iycount(y_cnt),
                .iled_pos_x(Hsync_Blank-1+600),
                .iled_pos_y(Vertical_Back_Porch),
                .inumber(num_input_s),
                .oOVERRIDE(oOVERRIDE[0]),
                .oR(LED0_R),
                .oG(LED0_G),
                .oB(LED0_B)
);

No_GEN LED1(
                .iclk(clk_ltm),
                .iReset_n(reset_n),
                .ixcount(x_cnt),
                .iycount(y_cnt),
                .iled_pos_x(Hsync_Blank-1+640),
                .iled_pos_y(Vertical_Back_Porch),
                .inumber(num_input_ts),
                .oOVERRIDE(oOVERRIDE[1]),
                .oR(LED1_R),
                .oG(LED1_G),
                .oB(LED1_B)
);

No_GEN LED2(
                .iclk(clk_ltm),
                .iReset_n(reset_n),
```

```
                        .ixcount(x_cnt),
                        .iycount(y_cnt),
                        .iled_pos_x(Hsync_Blank-1+680),
                        .iled_pos_y(Vertical_Back_Porch),
                        .inumber(num_input_min),
                        .oOVERRIDE(oOVERRIDE[2]),
                        .oR(LED2_R),
                        .oG(LED2_G),
                        .oB(LED2_B)
);

assign flag1 = (oCNT == 26'd24999999) ? 1'b1 : 1'b0;
assign flag2 = (inumber_s == 0) ? 1'b1 : 1'b0;
assign num_input_s = inumber_s;
assign num_input_ts = inumber_ts;
assign num_input_min = inumber_min;
assign oCNT = counter;

always@(posedge clk_ltm or negedge reset_n)
begin
    if(!reset_n)
    begin
    inumber_min <= 4'd2;
    inumber_ts <= 4'd0;
    inumber_s <= 4'd0;
    counter <= 26'b0;
    end
    else if(flag1)
        begin
```

```
if(flag2)
    begin
        if(inumber_ts != 0)
            begin
                inumber_ts <= inumber_ts - 1;
                inumber_s <= 4'd9;
                counter <= 26'b0;
            end
        else
            begin
                if(inumber_min != 0)
                    begin
                        inumber_min <= inumber_min -1;
                        inumber_ts    <= 4'd5;
                        inumber_s     <= 4'd9;
                        counter <= 26'b0;
                    end
                else
                    begin
                        inumber_min <= 4'd2;
                        inumber_ts <= 4'd0;
                        inumber_s <= 4'd0;
                        counter <= 26'b0;
                    end
            end
    end
else
begin
inumber_s <= inumber_s-1;
```

```
                counter <= 26'b0;
                end
            end
        else
            counter <= counter +1;
end

assign oVGA_ADDR = area[0] ? area_counter[0] : 18'bZ;
assign oVGA_OE_N = area[0] ? 1'b1 : 1'b0;
assign oVGA_WE_N = 0;

///////////////Test --Allocate color to each block//////////////////////
always@(posedge clk_ltm or negedge reset_n)
    begin
    if (!reset_n)
        begin
        red_1 <= 8'd255;
        green_1 <= 8'd255;
        blue_1 <= 8'd255;
        end
    else if (!(oOVERRIDE[2] || oOVERRIDE[1] || oOVERRIDE[0]))
        case(area)
            16'b0000000000000001:
            begin
            if(area_counter[0] == 15'd31999)
                area_counter[0] <= 0;
            else
                area_counter[0] <= area_counter[0] +1;
            red_1 <= (iVGA_DQ[15:11]<<3);
```

```
                green_1 <= (iVGA_DQ[10:5]<<2);
                blue_1 <= (iVGA_DQ[4:0]<<3);
                end//area 1
                16'b0000000000000010: begin red_1 <= 8'd255;green_1 <= 8'd128;blue_1 <=
8'd0;end
                16'b0000000000000100: begin red_1 <= 8'd255;green_1 <= 8'd255;blue_1 <=
8'd0;end
               16'b0000000000001000: begin red_1 <= 8'd128;green_1 <= 8'd255;blue_1 <= 8'd0;
end
                16'b0000000000010000: begin red_1 <= 8'd0;green_1 <= 8'd255;blue_1 <=
8'd0;end
                16'b0000000000100000: begin red_1 <= 8'd0;green_1 <= 8'd255;blue_1 <=
8'd128;end
                16'b0000000001000000: begin red_1 <= 8'd0;green_1 <= 8'd255;blue_1 <=
8'd255;end
                16'b0000000010000000: begin red_1 <= 8'd0;green_1 <= 8'd128;blue_1 <=
8'd255;end
                16'b0000000100000000: begin red_1 <= 8'd0;green_1 <= 8'd0;blue_1 <=
8'd255;end
                16'b0000001000000000: begin red_1 <= 8'd127;green_1 <= 8'd0;blue_1 <=
8'd255;end
                16'b0000010000000000: begin red_1 <= 8'd255;green_1 <= 8'd0;blue_1 <=
8'd255;end
                16'b0000100000000000: begin red_1 <= 8'd255;green_1 <= 8'd0;blue_1 <=
8'd127;end
                16'b0001000000000000: begin red_1 <= 8'd128;green_1 <= 8'd128;blue_1 <=
8'd128;end
                16'b0010000000000000: begin red_1 <= 8'd0;green_1 <= 8'd0;blue_1 <= 8'd0;end
                16'b0100000000000000: begin red_1 <= 8'd255;green_1 <= 8'd255;blue_1 <=
8'd255;end
                16'b1000000000000000: begin red_1 <= 8'd255;green_1 <= 8'd204;blue_1 <=
8'd204;end
                default: begin red_1 <= 8'd255;green_1 <= 8'd255;blue_1 <= 8'd255; end
            endcase
        else
            begin
```

```
                case(oOVERRIDE)
                    3'b001:
                        begin
                            red_1 <= LED0_R;
                            green_1 <= LED0_G;
                            blue_1 <= LED0_B;
                        end
                    3'b010:
                        begin
                            red_1 <= LED1_R;
                            green_1 <= LED1_G;
                            blue_1 <= LED1_B;
                        end
                    3'b100:
                        begin
                            red_1 <= LED2_R;
                            green_1 <= LED2_G;
                            blue_1 <= LED2_B;
                        end
                endcase
            end
        end

assign mred = red_1;
assign mgreen = green_1;
assign mblue    = blue_1;


always@(posedge clk_ltm or negedge reset_n)
```

```
    begin
        if (!reset_n)
            begin
                oHD <= 1'd0;
                oVD <= 1'd0;
                oDEN <= 1'd0;
                oLCD_R <= 8'd0;
                oLCD_G <= 8'd0;
                oLCD_B <= 8'd0;
            end
        else
            begin
                oHD <= mhd;
                oVD <= mvd;
                oDEN <= display_area;
                oLCD_R <= mred;
                oLCD_G <= mgreen;
                oLCD_B <= mblue;
            end
    end

endmodule




//////////////////////Number Display Module//////////////////////////
module No_GEN(
                iclk,
                iReset_n,
```

```
                ixcount,
                iycount,
                iled_pos_x,
                iled_pos_y,
                inumber,
                oOVERRIDE,
                oR,
                oG,
                oB
                );

//Port IO
input iclk;
input iReset_n;
input [3:0]inumber;
input [10:0] ixcount;
input [9:0]    iycount;
input [10:0] iled_pos_x;
input [10:0] iled_pos_y;
output oOVERRIDE;
output [7:0] oR;
output [7:0] oG;
output [7:0] oB;

//Wire & Reg
reg [7:0]    oR;
reg [7:0]    oG;
reg [7:0]    oB;
reg oOVERRIDE;
```

```
wire display_area;

wire number_area;

wire a;

wire b;

wire c;

wire d;

wire e;

wire f;

wire g;

wire a_en;

wire b_en;

wire c_en;

wire d_en;

wire e_en;

wire f_en;

wire g_en;


//Structure

assign display_area = ((ixcount > (iled_pos_x -1))
                                        && (ixcount < (iled_pos_x+ 60) )
                                        && (iycount > (iled_pos_y -1))
                                        && (iycount < (iled_pos_y +80))) ? 1'b1:1'b0;


assign number_area = ((ixcount > (iled_pos_x +4))
                                        && (ixcount < (iled_pos_x+ 35) )
                                        && (iycount > (iled_pos_y + 9))
                                        && (iycount < (iled_pos_y +70))) ? 1'b1:1'b0;


assign a = ((ixcount > (iled_pos_x + 4))
```

```
                    && (ixcount < (iled_pos_x + 35))
                    &&(iycount > (iled_pos_y + 9))
                    &&(iycount < (iled_pos_y + 18))) ? 1'b1 : 1'b0;
assign b =      ((ixcount > (iled_pos_x + 4))
                    && (ixcount < (iled_pos_x + 13))
                    &&(iycount > (iled_pos_y + 9))
                    &&(iycount < (iled_pos_y + 40))) ? 1'b1 : 1'b0;
assign c =   ((ixcount > (iled_pos_x + 4))
                    && (ixcount < (iled_pos_x + 13))
                    &&(iycount > (iled_pos_y + 39))
                    &&(iycount < (iled_pos_y + 70))) ? 1'b1 : 1'b0;
assign d =      ((ixcount > (iled_pos_x + 4))
                    && (ixcount < (iled_pos_x + 35))
                    &&(iycount > (iled_pos_y + 61))
                    &&(iycount < (iled_pos_y + 70))) ? 1'b1 : 1'b0;
assign e =      ((ixcount > (iled_pos_x + 26))
                    && (ixcount < (iled_pos_x + 35))
                    &&(iycount > (iled_pos_y + 39))
                    &&(iycount < (iled_pos_y + 70))) ? 1'b1 : 1'b0;
assign f =      ((ixcount > (iled_pos_x + 26))
                    && (ixcount < (iled_pos_x + 35))
                    &&(iycount > (iled_pos_y + 9))
                    &&(iycount < (iled_pos_y + 40))) ? 1'b1 : 1'b0;
assign g =      ((ixcount > (iled_pos_x + 4))
                    && (ixcount < (iled_pos_x + 35))
                    &&(iycount > (iled_pos_y + 35))
                    &&(iycount < (iled_pos_y + 44))) ? 1'b1 : 1'b0;

//assign a_en = ((inumber != 1) && (inumber != 4)) ? 1'b1 : 1'b0;
```

```
//assign b_en = ((inumber != 5) && (inumber != 6)) ? 1'b1 : 1'b0;

//assign c_en = ((inumber != 2)) ? 1'b1 : 1'b0;

//assign d_en = ((inumber != 1) && (inumber != 4) && (inumber != 7)) ? 1'b1 : 1'b0;

//assign e_en = ((inumber == 2) || (inumber == 6) || (inumber == 8) || (inumber == 0)) ? 1'b1:
1'b0;

//assign f_en = ((inumber == 4) || (inumber == 5) || (inumber == 6) || (inumber == 8)

//                              || (inumber == 9) || (inumber == 0)) ? 1'b1: 1'b0;

//assign g_en = ((inumber != 1) && (inumber != 7) && (inumber != 0)) ? 1'b1 : 1'b0;


always @(posedge iclk or negedge iReset_n)

begin

    if(!iReset_n)

            oOVERRIDE <= 1'b0;

    else

    case(inumber)

        0: oOVERRIDE <= (a||b||c||d||e||f);

        1: oOVERRIDE <= (b||c);

        2: oOVERRIDE <= (a||b||g||e||d);

        3: oOVERRIDE <= (a||b||c||d||g);

        4: oOVERRIDE <= (b||c||f||g);

        5: oOVERRIDE <= (a||c||d||f||g);

        6: oOVERRIDE <= (a||c||d||e||f||g);

        7: oOVERRIDE <= (a||b||c);

        8: oOVERRIDE <= (a||b||c||d||e||f||g);

        9: oOVERRIDE <= (a||b||c||d||f||g);

        default : oOVERRIDE <= 1'b0;

    endcase

    oR <= 8'd255;

    oG <= 8'd255;

    oB <= 8'd255;
```

```
end

endmodule
```

letter.v

```
module letter(
                        iclk,
                        ireset_n,
                        ix_cnt,
                        iy_cnt,
                        iletter_pos_x,
                        iletter_pos_y,
                        iletter,
                        oOVERRIDE,
                        oADDR
                        );

//=============================================
//Parameter================================
//=============================================
parameter A_base = 62400;
parameter B_base = 63424;
parameter C_base = 64448;
parameter D_base = 65472;
parameter E_base = 66496;
parameter F_base = 67520;
parameter G_base = 68544;
parameter H_base = 69568;
parameter I_base = 70592;
parameter J_base = 71616;
parameter K_base = 72640;
parameter L_base = 73664;
parameter M_base = 74688;
parameter N_base = 75712;
parameter O_base = 76736;
parameter P_base = 77760;
parameter Q_base = 78784;
parameter R_base = 79808;
parameter S_base = 80832;
parameter T_base = 81856;
parameter U_base = 82880;
parameter V_base = 83904;
parameter W_base = 84928;
parameter X_base = 85952;
parameter Y_base = 86976;
parameter Z_base = 88000;

parameter A = 5'd1;
parameter B = 5'd2;
parameter C = 5'd3;
parameter D = 5'd4;
parameter E = 5'd5;
parameter F = 5'd6;
```

```
parameter G = 5'd7;
parameter H = 5'd8;
parameter I = 5'd9;
parameter J = 5'd10;
parameter K = 5'd11;
parameter L = 5'd12;
parameter M = 5'd13;
parameter N = 5'd14;
parameter O = 5'd15;
parameter P = 5'd16;
parameter Q = 5'd17;
parameter R = 5'd18;
parameter S = 5'd19;
parameter T = 5'd20;
parameter U = 5'd21;
parameter V = 5'd22;
parameter W = 5'd23;
parameter X = 5'd24;
parameter Y = 5'd25;
parameter Z = 5'd26;

//=============================================
//I/O DECALARATION=============================
//=============================================
input iclk;
input ireset_n;
input [10:0] ix_cnt;
input [9:0] iy_cnt;
input [10:0]iletter_pos_x;
input [9:0]iletter_pos_y;
input [4:0] iletter;
output oOVERRIDE;
output [17:0] oADDR;


//=============================================
//WIRE & REG==================================
//=============================================
reg    oOVERRIDE;
reg [17:0] oADDR;
reg [4:0] counter;
reg [17:0] address;
wire display_area;
reg white[1024];


//=============================================
//Structured logic============================
//=============================================
assign display_area = ((ix_cnt > iletter_pos_x-1) && (ix_cnt < iletter_pos_x + 32)
                                        && (iy_cnt > iletter_pos_y -1) && (iy_cnt < iletter_pos_y
+ 32)) ? 1'b1:1'b0;


always@(negedge ireset_n)
begin
      if(!ireset_n)
            begin
```

```
case(iletter)
A: begin
        white[ 0 ]<=0;
        white[ 1 ]<=0;
        white[ 2 ]<=0;
        white[ 3 ]<=0;
        white[ 4 ]<=0;
        white[ 5 ]<=0;
        white[ 6 ]<=0;
        white[ 7 ]<=0;
        white[ 8 ]<=0;
        white[ 9 ]<=0;
        white[ 10 ]<=0;
        white[ 11 ]<=0;
        white[ 12 ]<=0;
        white[ 13 ]<=0;
        white[ 14 ]<=0;
        white[ 15 ]<=0;
        white[ 16 ]<=0;
        white[ 17 ]<=0;
        white[ 18 ]<=0;
        white[ 19 ]<=0;
        white[ 20 ]<=0;
        white[ 21 ]<=0;
        white[ 22 ]<=0;
        white[ 23 ]<=0;
        white[ 24 ]<=0;
        white[ 25 ]<=0;
        white[ 26 ]<=0;
        white[ 27 ]<=0;
        white[ 28 ]<=0;
        white[ 29 ]<=0;
        white[ 30 ]<=0;
        white[ 31 ]<=0;
        white[ 32 ]<=0;
        white[ 33 ]<=0;
        white[ 34 ]<=0;
        white[ 35 ]<=0;
        white[ 36 ]<=0;
        white[ 37 ]<=0;
        white[ 38 ]<=0;
        white[ 39 ]<=0;
        white[ 40 ]<=0;
        white[ 41 ]<=0;
        white[ 42 ]<=0;
        white[ 43 ]<=0;
        white[ 44 ]<=0;
        white[ 45 ]<=0;
        white[ 46 ]<=0;
        white[ 47 ]<=0;
        white[ 48 ]<=0;
        white[ 49 ]<=0;
        white[ 50 ]<=0;
        white[ 51 ]<=0;
        white[ 52 ]<=0;
        white[ 53 ]<=0;
        white[ 54 ]<=0;
        white[ 55 ]<=0;
```

```
white[ 56 ]<=0;
white[ 57 ]<=0;
white[ 58 ]<=0;
white[ 59 ]<=0;
white[ 60 ]<=0;
white[ 61 ]<=0;
white[ 62 ]<=0;
white[ 63 ]<=0;
white[ 64 ]<=0;
white[ 65 ]<=0;
white[ 66 ]<=0;
white[ 67 ]<=0;
white[ 68 ]<=0;
white[ 69 ]<=0;
white[ 70 ]<=0;
white[ 71 ]<=0;
white[ 72 ]<=0;
white[ 73 ]<=0;
white[ 74 ]<=0;
white[ 75 ]<=0;
white[ 76 ]<=0;
white[ 77 ]<=0;
white[ 78 ]<=0;
white[ 79 ]<=0;
white[ 80 ]<=0;
white[ 81 ]<=0;
white[ 82 ]<=0;
white[ 83 ]<=0;
white[ 84 ]<=0;
white[ 85 ]<=0;
white[ 86 ]<=0;
white[ 87 ]<=0;
white[ 88 ]<=0;
white[ 89 ]<=0;
white[ 90 ]<=0;
white[ 91 ]<=0;
white[ 92 ]<=0;
white[ 93 ]<=0;
white[ 94 ]<=0;
white[ 95 ]<=0;
white[ 96 ]<=0;
white[ 97 ]<=0;
white[ 98 ]<=0;
white[ 99 ]<=0;
white[ 100 ]<=0;
white[ 101 ]<=0;
white[ 102 ]<=0;
white[ 103 ]<=0;
white[ 104 ]<=0;
white[ 105 ]<=0;
white[ 106 ]<=0;
white[ 107 ]<=0;
white[ 108 ]<=0;
white[ 109 ]<=1;
white[ 110 ]<=1;
white[ 111 ]<=1;
white[ 112 ]<=1;
white[ 113 ]<=1;
```

```
white[ 114 ]<=1;
white[ 115 ]<=1;
white[ 116 ]<=1;
white[ 117 ]<=0;
white[ 118 ]<=0;
white[ 119 ]<=0;
white[ 120 ]<=0;
white[ 121 ]<=0;
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white[ 982 ]<=1;
white[ 983 ]<=1;
```

```
        white[ 984 ]<=1;
        white[ 985 ]<=1;
        white[ 986 ]<=1;
        white[ 987 ]<=1;
        white[ 988 ]<=1;
        white[ 989 ]<=1;
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        white[ 994 ]<=0;
        white[ 995 ]<=0;
        white[ 996 ]<=0;
        white[ 997 ]<=0;
        white[ 998 ]<=0;
        white[ 999 ]<=0;
        white[ 1000 ]<=0;
        white[ 1001 ]<=0;
        white[ 1002 ]<=0;
        white[ 1003 ]<=0;
        white[ 1004 ]<=0;
        white[ 1005 ]<=0;
        white[ 1006 ]<=0;
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        white[ 1008 ]<=0;
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        white[ 1012 ]<=0;
        white[ 1013 ]<=0;
        white[ 1014 ]<=0;
        white[ 1015 ]<=0;
        white[ 1016 ]<=0;
        white[ 1017 ]<=0;
        white[ 1018 ]<=0;
        white[ 1019 ]<=0;
        white[ 1020 ]<=0;
        white[ 1021 ]<=0;
        white[ 1022 ]<=0;
        white[ 1023 ]<=0;
        end

    B: begin
        white[ 0 ]<=0;
        white[ 1 ]<=0;
        white[ 2 ]<=0;
        white[ 3 ]<=0;
        white[ 4 ]<=0;
        white[ 5 ]<=0;
        white[ 6 ]<=0;
        white[ 7 ]<=0;
        white[ 8 ]<=0;
        white[ 9 ]<=0;
        white[ 10 ]<=0;
        white[ 11 ]<=0;
        white[ 12 ]<=0;
        white[ 13 ]<=0;
        white[ 14 ]<=0;
```

```
white[ 15 ]<=0;
white[ 16 ]<=0;
white[ 17 ]<=0;
white[ 18 ]<=0;
white[ 19 ]<=0;
white[ 20 ]<=0;
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white[ 66 ]<=0;
white[ 67 ]<=0;
white[ 68 ]<=0;
white[ 69 ]<=0;
white[ 70 ]<=0;
white[ 71 ]<=0;
white[ 72 ]<=0;
```

```
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white[ 75 ]<=0;
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white[ 77 ]<=0;
white[ 78 ]<=0;
white[ 79 ]<=0;
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white[ 126 ]<=0;
white[ 127 ]<=0;
white[ 128 ]<=0;
white[ 129 ]<=0;
white[ 130 ]<=1;
```

```
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white[ 182 ]<=0;
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white[ 184 ]<=0;
white[ 185 ]<=0;
white[ 186 ]<=0;
white[ 187 ]<=0;
white[ 188 ]<=0;
```

```
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```

```
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white[ 254 ]<=0;
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white[ 300 ]<=1;
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```

```
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white[ 358 ]<=1;
white[ 359 ]<=1;
white[ 360 ]<=1;
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white[ 362 ]<=1;
```

```
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white[ 414 ]<=0;
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white[ 416 ]<=0;
white[ 417 ]<=0;
white[ 418 ]<=0;
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white[ 420 ]<=1;
```

```
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white[ 474 ]<=0;
white[ 475 ]<=0;
white[ 476 ]<=0;
white[ 477 ]<=0;
white[ 478 ]<=0;
```

```
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white[ 486 ]<=1;
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```

```
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white[ 590 ]<=1;
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white[ 592 ]<=1;
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white[ 594 ]<=1;
```

```
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white[ 647 ]<=1;
white[ 648 ]<=1;
white[ 649 ]<=1;
white[ 650 ]<=1;
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white[ 652 ]<=1;
```

```
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white[ 705 ]<=0;
white[ 706 ]<=0;
white[ 707 ]<=1;
white[ 708 ]<=1;
white[ 709 ]<=1;
white[ 710 ]<=1;
```

```
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white[ 716 ]<=1;
white[ 717 ]<=1;
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white[ 763 ]<=1;
white[ 764 ]<=1;
white[ 765 ]<=1;
white[ 766 ]<=0;
white[ 767 ]<=0;
white[ 768 ]<=0;
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white[ 774 ]<=1;
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white[ 818 ]<=1;
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white[ 820 ]<=1;
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white[ 824 ]<=1;
white[ 825 ]<=1;
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white[ 995 ]<=0;
white[ 996 ]<=0;
white[ 997 ]<=0;
white[ 998 ]<=0;
white[ 999 ]<=0;
white[ 1000 ]<=0;
```

```
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        white[ 1003 ]<=0;
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        white[ 1005 ]<=0;
        white[ 1006 ]<=0;
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        white[ 1019 ]<=0;
        white[ 1020 ]<=0;
        white[ 1021 ]<=0;
        white[ 1022 ]<=0;
        white[ 1023 ]<=0;
        end

    C: begin
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        white[ 3 ]<=0;
        white[ 4 ]<=0;
        white[ 5 ]<=0;
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        white[ 25 ]<=0;
        white[ 26 ]<=0;
        white[ 27 ]<=0;
        white[ 28 ]<=0;
        white[ 29 ]<=0;
        white[ 30 ]<=0;
        white[ 31 ]<=0;
```

```
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white[ 85 ]<=1;
white[ 86 ]<=0;
white[ 87 ]<=0;
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white[ 89 ]<=0;
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white[ 143 ]<=1;
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white[ 145 ]<=1;
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white[ 147 ]<=1;
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```

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```

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```
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white[ 662 ]<=1;
white[ 663 ]<=1;
white[ 664 ]<=1;
white[ 665 ]<=1;
white[ 666 ]<=1;
white[ 667 ]<=1;
white[ 668 ]<=1;
white[ 669 ]<=1;
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```
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white[ 671 ]<=0;
white[ 672 ]<=0;
white[ 673 ]<=0;
white[ 674 ]<=0;
white[ 675 ]<=0;
white[ 676 ]<=1;
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white[ 682 ]<=1;
white[ 683 ]<=1;
white[ 684 ]<=1;
white[ 685 ]<=1;
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white[ 698 ]<=1;
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white[ 722 ]<=1;
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white[ 724 ]<=1;
white[ 725 ]<=1;
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white[ 780 ]<=1;
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white[ 782 ]<=1;
white[ 783 ]<=1;
white[ 784 ]<=1;
white[ 785 ]<=1;
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white[ 896 ]<=0;
white[ 897 ]<=0;
white[ 898 ]<=0;
white[ 899 ]<=0;
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white[ 901 ]<=0;
```

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white[ 907 ]<=1;
white[ 908 ]<=1;
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white[ 955 ]<=0;
white[ 956 ]<=0;
white[ 957 ]<=0;
white[ 958 ]<=0;
white[ 959 ]<=0;
```

```
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white[ 963 ]<=0;
white[ 964 ]<=0;
white[ 965 ]<=0;
white[ 966 ]<=0;
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white[ 1005 ]<=0;
white[ 1006 ]<=0;
white[ 1007 ]<=0;
white[ 1008 ]<=0;
white[ 1009 ]<=0;
white[ 1010 ]<=0;
white[ 1011 ]<=0;
white[ 1012 ]<=0;
white[ 1013 ]<=0;
white[ 1014 ]<=0;
white[ 1015 ]<=0;
white[ 1016 ]<=0;
white[ 1017 ]<=0;
```

```
white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

D:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 43 ]<=0;
white[ 44 ]<=0;
white[ 45 ]<=0;
white[ 46 ]<=0;
white[ 47 ]<=0;
white[ 48 ]<=0;
```

```
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white[ 53 ]<=0;
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white[ 55 ]<=0;
white[ 56 ]<=0;
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white[ 99 ]<=1;
white[ 100 ]<=1;
white[ 101 ]<=1;
white[ 102 ]<=1;
white[ 103 ]<=1;
white[ 104 ]<=1;
white[ 105 ]<=1;
white[ 106 ]<=1;
```

```
white[ 107 ]<=1;
white[ 108 ]<=1;
white[ 109 ]<=1;
white[ 110 ]<=1;
white[ 111 ]<=1;
white[ 112 ]<=1;
white[ 113 ]<=0;
white[ 114 ]<=0;
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white[ 159 ]<=0;
white[ 160 ]<=0;
white[ 161 ]<=0;
white[ 162 ]<=1;
white[ 163 ]<=1;
white[ 164 ]<=1;
```

```
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white[ 171 ]<=1;
white[ 172 ]<=1;
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white[ 218 ]<=0;
white[ 219 ]<=0;
white[ 220 ]<=0;
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```

```
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```

```
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white[ 333 ]<=1;
white[ 334 ]<=0;
white[ 335 ]<=0;
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```

```
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white[ 390 ]<=1;
white[ 391 ]<=1;
white[ 392 ]<=1;
white[ 393 ]<=1;
white[ 394 ]<=1;
white[ 395 ]<=1;
white[ 396 ]<=1;
```

```
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white[ 403 ]<=1;
white[ 404 ]<=1;
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```
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white[ 495 ]<=0;
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white[ 502 ]<=1;
white[ 503 ]<=1;
white[ 504 ]<=1;
white[ 505 ]<=1;
white[ 506 ]<=1;
white[ 507 ]<=1;
white[ 508 ]<=1;
white[ 509 ]<=1;
white[ 510 ]<=0;
white[ 511 ]<=0;
white[ 512 ]<=0;
```

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```
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white[ 577 ]<=0;
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white[ 623 ]<=0;
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white[ 856 ]<=1;
white[ 857 ]<=1;
white[ 858 ]<=1;
white[ 859 ]<=0;
white[ 860 ]<=0;
```

```
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white[ 866 ]<=1;
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white[ 915 ]<=1;
white[ 916 ]<=1;
white[ 917 ]<=1;
white[ 918 ]<=1;
```

```
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white[ 923 ]<=0;
white[ 924 ]<=0;
white[ 925 ]<=0;
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white[ 972 ]<=0;
white[ 973 ]<=0;
white[ 974 ]<=0;
white[ 975 ]<=0;
white[ 976 ]<=0;
```

```
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white[ 981 ]<=0;
white[ 982 ]<=0;
white[ 983 ]<=0;
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white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

E:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
white[ 7 ]<=0;
```

```
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white[ 13 ]<=0;
white[ 14 ]<=0;
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white[ 59 ]<=0;
white[ 60 ]<=0;
white[ 61 ]<=0;
white[ 62 ]<=0;
white[ 63 ]<=0;
white[ 64 ]<=0;
white[ 65 ]<=0;
```

```
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white[ 117 ]<=1;
white[ 118 ]<=1;
white[ 119 ]<=0;
white[ 120 ]<=0;
white[ 121 ]<=0;
white[ 122 ]<=0;
white[ 123 ]<=0;
```

```
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white[ 175 ]<=1;
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white[ 177 ]<=1;
white[ 178 ]<=1;
white[ 179 ]<=1;
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white[ 181 ]<=1;
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white[ 239 ]<=1;
```

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white[ 293 ]<=1;
white[ 294 ]<=1;
white[ 295 ]<=1;
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```
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white[ 349 ]<=0;
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white[ 351 ]<=0;
white[ 352 ]<=0;
white[ 353 ]<=0;
white[ 354 ]<=0;
white[ 355 ]<=1;
```

```
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white[ 407 ]<=1;
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white[ 409 ]<=0;
white[ 410 ]<=0;
white[ 411 ]<=0;
white[ 412 ]<=0;
white[ 413 ]<=0;
```

```
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```

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```

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white[ 582 ]<=1;
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white[ 584 ]<=1;
white[ 585 ]<=1;
white[ 586 ]<=1;
white[ 587 ]<=1;
```

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white[ 593 ]<=1;
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white[ 816 ]<=1;
white[ 817 ]<=1;
white[ 818 ]<=1;
white[ 819 ]<=1;
```

```
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white[ 875 ]<=1;
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```

```
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white[ 933 ]<=0;
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white[ 935 ]<=0;
```

```
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white[ 989 ]<=0;
white[ 990 ]<=0;
white[ 991 ]<=0;
white[ 992 ]<=0;
white[ 993 ]<=0;
```

```
white[ 994 ]<=0;
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white[ 997 ]<=0;
white[ 998 ]<=0;
white[ 999 ]<=0;
white[ 1000 ]<=0;
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white[ 1009 ]<=0;
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white[ 1012 ]<=0;
white[ 1013 ]<=0;
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white[ 1018 ]<=0;
white[ 1019 ]<=1;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

F:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 12 ]<=0;
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white[ 14 ]<=0;
white[ 15 ]<=0;
white[ 16 ]<=0;
white[ 17 ]<=0;
white[ 18 ]<=0;
white[ 19 ]<=0;
white[ 20 ]<=0;
white[ 21 ]<=0;
white[ 22 ]<=0;
white[ 23 ]<=0;
white[ 24 ]<=0;
```

```
white[ 25 ]<=0;
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white[ 30 ]<=0;
white[ 31 ]<=0;
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white[ 76 ]<=0;
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white[ 78 ]<=0;
white[ 79 ]<=0;
white[ 80 ]<=0;
white[ 81 ]<=0;
white[ 82 ]<=0;
```

```
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white[ 134 ]<=1;
white[ 135 ]<=1;
white[ 136 ]<=1;
white[ 137 ]<=1;
white[ 138 ]<=1;
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white[ 140 ]<=1;
```

```
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white[ 1016 ]<=0;
white[ 1017 ]<=0;
white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

G:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 35 ]<=0;
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white[ 37 ]<=0;
white[ 38 ]<=0;
white[ 39 ]<=0;
white[ 40 ]<=0;
white[ 41 ]<=0;
```

```
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white[ 99 ]<=0;
```

```
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```

```
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white[ 385 ]<=0;
white[ 386 ]<=1;
white[ 387 ]<=1;
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```

```
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white[ 499 ]<=1;
white[ 500 ]<=1;
white[ 501 ]<=1;
white[ 502 ]<=1;
white[ 503 ]<=1;
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```

```
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```

```
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```

```
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white[ 865 ]<=0;
white[ 866 ]<=0;
white[ 867 ]<=0;
white[ 868 ]<=0;
white[ 869 ]<=0;
white[ 870 ]<=0;
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white[ 906 ]<=1;
white[ 907 ]<=1;
white[ 908 ]<=1;
white[ 909 ]<=1;
white[ 910 ]<=1;
white[ 911 ]<=1;
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white[ 965 ]<=0;
white[ 966 ]<=0;
white[ 967 ]<=0;
white[ 968 ]<=0;
white[ 969 ]<=0;
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```
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white[ 974 ]<=1;
white[ 975 ]<=1;
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white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

H:begin
white[ 0 ]<=0;
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white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
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white[ 54 ]<=0;
white[ 55 ]<=0;
white[ 56 ]<=0;
white[ 57 ]<=0;
white[ 58 ]<=0;
```

```
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white[ 66 ]<=0;
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white[ 110 ]<=0;
white[ 111 ]<=0;
white[ 112 ]<=0;
white[ 113 ]<=1;
white[ 114 ]<=1;
white[ 115 ]<=1;
white[ 116 ]<=1;
```

```
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white[ 171 ]<=1;
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```

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```

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```

```
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```

```
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```

```
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```

```
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white[ 518 ]<=1;
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white[ 520 ]<=1;
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white[ 522 ]<=1;
```

```
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white[ 578 ]<=1;
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white[ 580 ]<=1;
```

```
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white[ 633 ]<=1;
white[ 634 ]<=1;
white[ 635 ]<=1;
white[ 636 ]<=1;
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white[ 638 ]<=1;
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```
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white[ 644 ]<=1;
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white[ 691 ]<=1;
white[ 692 ]<=1;
white[ 693 ]<=1;
white[ 694 ]<=1;
white[ 695 ]<=1;
white[ 696 ]<=1;
```

```
white[ 697 ]<=1;
white[ 698 ]<=1;
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white[ 701 ]<=1;
white[ 702 ]<=1;
white[ 703 ]<=1;
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white[ 809 ]<=1;
white[ 810 ]<=1;
white[ 811 ]<=1;
white[ 812 ]<=1;
```

```
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white[ 818 ]<=1;
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white[ 923 ]<=1;
white[ 924 ]<=1;
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white[ 926 ]<=1;
white[ 927 ]<=1;
white[ 928 ]<=0;
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white[ 984 ]<=0;
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```

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white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

I:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 71 ]<=0;
white[ 72 ]<=0;
white[ 73 ]<=0;
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```

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white[ 130 ]<=0;
white[ 131 ]<=0;
white[ 132 ]<=0;
white[ 133 ]<=0;
```

```
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```

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```
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J:begin
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white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 379 ]<=0;
white[ 380 ]<=0;
white[ 381 ]<=0;
white[ 382 ]<=0;
```

```
white[ 383 ]<=0;
white[ 384 ]<=0;
white[ 385 ]<=0;
white[ 386 ]<=0;
white[ 387 ]<=0;
white[ 388 ]<=0;
white[ 389 ]<=0;
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white[ 434 ]<=1;
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white[ 436 ]<=1;
white[ 437 ]<=1;
white[ 438 ]<=1;
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white[ 440 ]<=1;
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```
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white[ 444 ]<=0;
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white[ 492 ]<=0;
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white[ 494 ]<=0;
white[ 495 ]<=0;
white[ 496 ]<=1;
white[ 497 ]<=1;
white[ 498 ]<=1;
```

```
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white[ 501 ]<=1;
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white[ 503 ]<=1;
white[ 504 ]<=1;
white[ 505 ]<=1;
white[ 506 ]<=0;
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```

```
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white[ 608 ]<=0;
white[ 609 ]<=0;
white[ 610 ]<=0;
white[ 611 ]<=0;
white[ 612 ]<=1;
white[ 613 ]<=1;
white[ 614 ]<=1;
```

```
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white[ 617 ]<=1;
white[ 618 ]<=1;
white[ 619 ]<=1;
white[ 620 ]<=1;
white[ 621 ]<=0;
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white[ 625 ]<=1;
white[ 626 ]<=1;
white[ 627 ]<=1;
white[ 628 ]<=1;
white[ 629 ]<=1;
white[ 630 ]<=1;
white[ 631 ]<=1;
white[ 632 ]<=1;
white[ 633 ]<=1;
white[ 634 ]<=1;
white[ 635 ]<=0;
white[ 636 ]<=0;
white[ 637 ]<=0;
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white[ 667 ]<=0;
white[ 668 ]<=0;
white[ 669 ]<=0;
white[ 670 ]<=0;
white[ 671 ]<=0;
white[ 672 ]<=0;
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```
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white[ 677 ]<=1;
white[ 678 ]<=1;
white[ 679 ]<=1;
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white[ 696 ]<=1;
white[ 697 ]<=1;
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white[ 699 ]<=0;
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white[ 701 ]<=0;
white[ 702 ]<=0;
white[ 703 ]<=0;
white[ 704 ]<=0;
white[ 705 ]<=0;
white[ 706 ]<=0;
white[ 707 ]<=0;
white[ 708 ]<=0;
white[ 709 ]<=1;
white[ 710 ]<=1;
white[ 711 ]<=1;
white[ 712 ]<=1;
white[ 713 ]<=1;
white[ 714 ]<=1;
white[ 715 ]<=1;
white[ 716 ]<=1;
white[ 717 ]<=1;
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white[ 725 ]<=1;
white[ 726 ]<=1;
white[ 727 ]<=1;
white[ 728 ]<=1;
white[ 729 ]<=1;
white[ 730 ]<=0;
```

```
white[ 731 ]<=0;
white[ 732 ]<=0;
white[ 733 ]<=0;
white[ 734 ]<=0;
white[ 735 ]<=0;
white[ 736 ]<=0;
white[ 737 ]<=0;
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white[ 771 ]<=0;
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white[ 775 ]<=1;
white[ 776 ]<=1;
white[ 777 ]<=1;
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white[ 779 ]<=1;
white[ 780 ]<=1;
white[ 781 ]<=1;
white[ 782 ]<=1;
white[ 783 ]<=1;
white[ 784 ]<=1;
white[ 785 ]<=1;
white[ 786 ]<=1;
white[ 787 ]<=1;
white[ 788 ]<=1;
```

```
white[ 789 ]<=1;
white[ 790 ]<=1;
white[ 791 ]<=1;
white[ 792 ]<=1;
white[ 793 ]<=1;
white[ 794 ]<=0;
white[ 795 ]<=0;
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white[ 797 ]<=0;
white[ 798 ]<=0;
white[ 799 ]<=0;
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white[ 813 ]<=1;
white[ 814 ]<=1;
white[ 815 ]<=1;
white[ 816 ]<=1;
white[ 817 ]<=1;
white[ 818 ]<=1;
white[ 819 ]<=1;
white[ 820 ]<=1;
white[ 821 ]<=1;
white[ 822 ]<=1;
white[ 823 ]<=1;
white[ 824 ]<=1;
white[ 825 ]<=0;
white[ 826 ]<=0;
white[ 827 ]<=0;
white[ 828 ]<=0;
white[ 829 ]<=0;
white[ 830 ]<=0;
white[ 831 ]<=0;
white[ 832 ]<=0;
white[ 833 ]<=0;
white[ 834 ]<=0;
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white[ 836 ]<=0;
white[ 837 ]<=0;
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white[ 839 ]<=1;
white[ 840 ]<=1;
white[ 841 ]<=1;
white[ 842 ]<=1;
white[ 843 ]<=1;
white[ 844 ]<=1;
white[ 845 ]<=1;
white[ 846 ]<=1;
```

```
white[ 847 ]<=1;
white[ 848 ]<=1;
white[ 849 ]<=1;
white[ 850 ]<=1;
white[ 851 ]<=1;
white[ 852 ]<=1;
white[ 853 ]<=1;
white[ 854 ]<=1;
white[ 855 ]<=1;
white[ 856 ]<=0;
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white[ 858 ]<=0;
white[ 859 ]<=0;
white[ 860 ]<=0;
white[ 861 ]<=0;
white[ 862 ]<=0;
white[ 863 ]<=0;
white[ 864 ]<=0;
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white[ 868 ]<=0;
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white[ 872 ]<=1;
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white[ 881 ]<=1;
white[ 882 ]<=1;
white[ 883 ]<=1;
white[ 884 ]<=1;
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white[ 887 ]<=1;
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white[ 899 ]<=0;
white[ 900 ]<=0;
white[ 901 ]<=0;
white[ 902 ]<=0;
white[ 903 ]<=1;
white[ 904 ]<=1;
```

```
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white[ 907 ]<=1;
white[ 908 ]<=1;
white[ 909 ]<=1;
white[ 910 ]<=1;
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white[ 958 ]<=0;
white[ 959 ]<=0;
white[ 960 ]<=0;
white[ 961 ]<=0;
white[ 962 ]<=0;
```

```
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white[ 964 ]<=0;
white[ 965 ]<=0;
white[ 966 ]<=1;
white[ 967 ]<=0;
white[ 968 ]<=0;
white[ 969 ]<=0;
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white[ 974 ]<=1;
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white[ 976 ]<=1;
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white[ 978 ]<=1;
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white[ 982 ]<=0;
white[ 983 ]<=0;
white[ 984 ]<=0;
white[ 985 ]<=0;
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white[ 1006 ]<=0;
white[ 1007 ]<=0;
white[ 1008 ]<=0;
white[ 1009 ]<=0;
white[ 1010 ]<=0;
white[ 1011 ]<=0;
white[ 1012 ]<=0;
white[ 1013 ]<=0;
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white[ 1015 ]<=0;
white[ 1016 ]<=0;
white[ 1017 ]<=0;
white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
```

```
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

K:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
white[ 7 ]<=0;
white[ 8 ]<=0;
white[ 9 ]<=0;
white[ 10 ]<=0;
white[ 11 ]<=0;
white[ 12 ]<=0;
white[ 13 ]<=0;
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white[ 38 ]<=0;
white[ 39 ]<=0;
white[ 40 ]<=0;
white[ 41 ]<=0;
white[ 42 ]<=0;
white[ 43 ]<=0;
white[ 44 ]<=0;
white[ 45 ]<=0;
white[ 46 ]<=0;
white[ 47 ]<=0;
white[ 48 ]<=0;
white[ 49 ]<=0;
white[ 50 ]<=0;
white[ 51 ]<=0;
```

```
white[ 52 ]<=0;
white[ 53 ]<=0;
white[ 54 ]<=0;
white[ 55 ]<=0;
white[ 56 ]<=0;
white[ 57 ]<=0;
white[ 58 ]<=0;
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white[ 97 ]<=0;
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white[ 100 ]<=0;
white[ 101 ]<=0;
white[ 102 ]<=0;
white[ 103 ]<=0;
white[ 104 ]<=0;
white[ 105 ]<=0;
white[ 106 ]<=0;
white[ 107 ]<=0;
white[ 108 ]<=0;
white[ 109 ]<=0;
```

```
white[ 110 ]<=0;
white[ 111 ]<=0;
white[ 112 ]<=0;
white[ 113 ]<=0;
white[ 114 ]<=0;
white[ 115 ]<=0;
white[ 116 ]<=0;
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white[ 159 ]<=0;
white[ 160 ]<=0;
white[ 161 ]<=0;
white[ 162 ]<=1;
white[ 163 ]<=0;
white[ 164 ]<=1;
white[ 165 ]<=1;
white[ 166 ]<=1;
white[ 167 ]<=1;
```

```
white[ 168 ]<=1;
white[ 169 ]<=1;
white[ 170 ]<=1;
white[ 171 ]<=1;
white[ 172 ]<=1;
white[ 173 ]<=1;
white[ 174 ]<=0;
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white[ 179 ]<=1;
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white[ 183 ]<=1;
white[ 184 ]<=1;
white[ 185 ]<=1;
white[ 186 ]<=1;
white[ 187 ]<=1;
white[ 188 ]<=1;
white[ 189 ]<=0;
white[ 190 ]<=0;
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white[ 192 ]<=0;
white[ 193 ]<=0;
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white[ 203 ]<=1;
white[ 204 ]<=1;
white[ 205 ]<=1;
white[ 206 ]<=0;
white[ 207 ]<=0;
white[ 208 ]<=0;
white[ 209 ]<=1;
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white[ 213 ]<=1;
white[ 214 ]<=1;
white[ 215 ]<=1;
white[ 216 ]<=1;
white[ 217 ]<=1;
white[ 218 ]<=1;
white[ 219 ]<=1;
white[ 220 ]<=1;
white[ 221 ]<=0;
white[ 222 ]<=0;
white[ 223 ]<=0;
white[ 224 ]<=0;
white[ 225 ]<=0;
```

```
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white[ 231 ]<=1;
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white[ 277 ]<=1;
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white[ 279 ]<=1;
white[ 280 ]<=1;
white[ 281 ]<=1;
white[ 282 ]<=1;
white[ 283 ]<=0;
```

```
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white[ 335 ]<=1;
white[ 336 ]<=1;
white[ 337 ]<=1;
white[ 338 ]<=1;
white[ 339 ]<=1;
white[ 340 ]<=1;
white[ 341 ]<=1;
```

```
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white[ 393 ]<=1;
white[ 394 ]<=1;
white[ 395 ]<=1;
white[ 396 ]<=1;
white[ 397 ]<=1;
white[ 398 ]<=1;
white[ 399 ]<=1;
```

```
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white[ 404 ]<=1;
white[ 405 ]<=1;
white[ 406 ]<=1;
white[ 407 ]<=1;
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white[ 451 ]<=0;
white[ 452 ]<=1;
white[ 453 ]<=1;
white[ 454 ]<=1;
white[ 455 ]<=1;
white[ 456 ]<=1;
white[ 457 ]<=1;
```

```
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white[ 464 ]<=1;
white[ 465 ]<=1;
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white[ 509 ]<=0;
white[ 510 ]<=0;
white[ 511 ]<=0;
white[ 512 ]<=0;
white[ 513 ]<=0;
white[ 514 ]<=0;
white[ 515 ]<=0;
```

```
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white[ 523 ]<=1;
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white[ 567 ]<=1;
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white[ 570 ]<=0;
white[ 571 ]<=0;
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white[ 573 ]<=0;
```

```
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white[ 579 ]<=0;
white[ 580 ]<=1;
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white[ 626 ]<=1;
white[ 627 ]<=1;
white[ 628 ]<=1;
white[ 629 ]<=1;
white[ 630 ]<=1;
white[ 631 ]<=1;
```

```
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white[ 685 ]<=1;
white[ 686 ]<=1;
white[ 687 ]<=1;
white[ 688 ]<=1;
white[ 689 ]<=1;
```

```
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white[ 695 ]<=1;
white[ 696 ]<=1;
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white[ 744 ]<=1;
white[ 745 ]<=1;
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white[ 747 ]<=1;
```

```
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```
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white[ 859 ]<=1;
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white[ 863 ]<=0;
```

```
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white[ 917 ]<=1;
white[ 918 ]<=1;
white[ 919 ]<=1;
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white[ 921 ]<=1;
```

```
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white[ 974 ]<=0;
white[ 975 ]<=0;
white[ 976 ]<=0;
white[ 977 ]<=0;
white[ 978 ]<=0;
white[ 979 ]<=0;
```

```
white[ 980 ]<=0;
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white[ 982 ]<=0;
white[ 983 ]<=0;
white[ 984 ]<=0;
white[ 985 ]<=0;
white[ 986 ]<=0;
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white[ 1009 ]<=0;
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white[ 1012 ]<=0;
white[ 1013 ]<=0;
white[ 1014 ]<=0;
white[ 1015 ]<=0;
white[ 1016 ]<=0;
white[ 1017 ]<=0;
white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

L:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
white[ 7 ]<=0;
white[ 8 ]<=0;
white[ 9 ]<=0;
white[ 10 ]<=0;
```

```
white[ 11 ]<=0;
white[ 12 ]<=0;
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white[ 14 ]<=0;
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white[ 16 ]<=0;
white[ 17 ]<=0;
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white[ 34 ]<=0;
white[ 35 ]<=0;
white[ 36 ]<=0;
white[ 37 ]<=0;
white[ 38 ]<=0;
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white[ 908 ]<=1;
white[ 909 ]<=1;
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```
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white[ 944 ]<=1;
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white[ 993 ]<=0;
white[ 994 ]<=0;
white[ 995 ]<=0;
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```

```
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white[ 1003 ]<=0;
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white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

M:begin
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white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 24 ]<=0;
white[ 25 ]<=0;
white[ 26 ]<=0;
white[ 27 ]<=0;
```

```
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white[ 82 ]<=0;
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white[ 141 ]<=0;
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```

```
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```

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```
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```

```
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white[ 487 ]<=1;
white[ 488 ]<=1;
white[ 489 ]<=1;
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```
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```
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white[ 601 ]<=1;
white[ 602 ]<=1;
white[ 603 ]<=1;
white[ 604 ]<=1;
white[ 605 ]<=1;
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white[ 607 ]<=1;
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```
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white[ 665 ]<=1;
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white[ 778 ]<=1;
white[ 779 ]<=1;
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white[ 781 ]<=1;
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white[ 953 ]<=0;
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```

```
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white[ 961 ]<=0;
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white[ 1009 ]<=0;
white[ 1010 ]<=0;
white[ 1011 ]<=0;
white[ 1012 ]<=0;
white[ 1013 ]<=0;
```

```
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white[ 1015 ]<=0;
white[ 1016 ]<=0;
white[ 1017 ]<=0;
white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

N:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 38 ]<=0;
white[ 39 ]<=0;
white[ 40 ]<=0;
white[ 41 ]<=0;
white[ 42 ]<=0;
white[ 43 ]<=0;
white[ 44 ]<=0;
```

```
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white[ 97 ]<=0;
white[ 98 ]<=0;
white[ 99 ]<=0;
white[ 100 ]<=0;
white[ 101 ]<=0;
white[ 102 ]<=0;
```

```
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white[ 110 ]<=0;
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```

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white[ 214 ]<=1;
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white[ 216 ]<=1;
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```

```
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```

```
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```

```
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white[ 392 ]<=1;
```

```
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white[ 502 ]<=1;
white[ 503 ]<=1;
white[ 504 ]<=1;
white[ 505 ]<=1;
white[ 506 ]<=1;
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white[ 508 ]<=1;
```

```
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white[ 513 ]<=0;
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white[ 515 ]<=0;
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white[ 561 ]<=1;
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```
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white[ 596 ]<=1;
white[ 597 ]<=1;
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white[ 600 ]<=1;
white[ 601 ]<=1;
white[ 602 ]<=1;
white[ 603 ]<=1;
white[ 604 ]<=1;
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white[ 606 ]<=0;
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white[ 608 ]<=0;
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white[ 611 ]<=0;
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white[ 613 ]<=1;
white[ 614 ]<=1;
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white[ 619 ]<=1;
white[ 620 ]<=1;
white[ 621 ]<=1;
white[ 622 ]<=1;
white[ 623 ]<=1;
white[ 624 ]<=1;
```

```
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white[ 626 ]<=1;
white[ 627 ]<=1;
white[ 628 ]<=1;
white[ 629 ]<=1;
white[ 630 ]<=1;
white[ 631 ]<=1;
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white[ 677 ]<=1;
white[ 678 ]<=1;
white[ 679 ]<=1;
white[ 680 ]<=1;
white[ 681 ]<=1;
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white[ 794 ]<=1;
white[ 795 ]<=1;
white[ 796 ]<=1;
white[ 797 ]<=1;
white[ 798 ]<=0;
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white[ 852 ]<=1;
white[ 853 ]<=1;
white[ 854 ]<=1;
white[ 855 ]<=1;
white[ 856 ]<=1;
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```
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white[ 862 ]<=0;
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white[ 909 ]<=0;
white[ 910 ]<=0;
white[ 911 ]<=0;
white[ 912 ]<=0;
white[ 913 ]<=0;
white[ 914 ]<=0;
```

```
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white[ 916 ]<=0;
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white[ 919 ]<=1;
white[ 920 ]<=1;
white[ 921 ]<=1;
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white[ 968 ]<=1;
white[ 969 ]<=1;
white[ 970 ]<=0;
white[ 971 ]<=0;
white[ 972 ]<=0;
```

```
white[ 973 ]<=0;
white[ 974 ]<=0;
white[ 975 ]<=0;
white[ 976 ]<=0;
white[ 977 ]<=0;
white[ 978 ]<=0;
white[ 979 ]<=0;
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white[ 992 ]<=0;
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white[ 994 ]<=0;
white[ 995 ]<=0;
white[ 996 ]<=0;
white[ 997 ]<=0;
white[ 998 ]<=0;
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white[ 1003 ]<=0;
white[ 1004 ]<=0;
white[ 1005 ]<=0;
white[ 1006 ]<=0;
white[ 1007 ]<=0;
white[ 1008 ]<=0;
white[ 1009 ]<=0;
white[ 1010 ]<=0;
white[ 1011 ]<=0;
white[ 1012 ]<=0;
white[ 1013 ]<=0;
white[ 1014 ]<=0;
white[ 1015 ]<=0;
white[ 1016 ]<=0;
white[ 1017 ]<=0;
white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

O:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
```

```
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
white[ 7 ]<=0;
white[ 8 ]<=0;
white[ 9 ]<=0;
white[ 10 ]<=0;
white[ 11 ]<=0;
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white[ 49 ]<=0;
white[ 50 ]<=0;
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white[ 52 ]<=0;
white[ 53 ]<=0;
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white[ 55 ]<=0;
white[ 56 ]<=0;
white[ 57 ]<=0;
white[ 58 ]<=0;
white[ 59 ]<=0;
white[ 60 ]<=0;
white[ 61 ]<=0;
```

```
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white[ 63 ]<=0;
white[ 64 ]<=0;
white[ 65 ]<=0;
white[ 66 ]<=0;
white[ 67 ]<=0;
white[ 68 ]<=0;
white[ 69 ]<=0;
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white[ 113 ]<=1;
white[ 114 ]<=1;
white[ 115 ]<=0;
white[ 116 ]<=0;
white[ 117 ]<=0;
white[ 118 ]<=0;
white[ 119 ]<=0;
```

```
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white[ 123 ]<=0;
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white[ 126 ]<=0;
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white[ 171 ]<=1;
white[ 172 ]<=1;
white[ 173 ]<=1;
white[ 174 ]<=1;
white[ 175 ]<=1;
white[ 176 ]<=1;
white[ 177 ]<=1;
```

```
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white[ 230 ]<=1;
white[ 231 ]<=1;
white[ 232 ]<=1;
white[ 233 ]<=1;
white[ 234 ]<=1;
white[ 235 ]<=1;
```

```
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white[ 241 ]<=1;
white[ 242 ]<=1;
white[ 243 ]<=1;
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white[ 289 ]<=0;
white[ 290 ]<=0;
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```

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white[ 301 ]<=1;
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white[ 347 ]<=1;
white[ 348 ]<=1;
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```

```
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white[ 403 ]<=0;
white[ 404 ]<=1;
white[ 405 ]<=1;
white[ 406 ]<=1;
white[ 407 ]<=1;
white[ 408 ]<=1;
white[ 409 ]<=1;
```

```
white[ 410 ]<=1;
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white[ 415 ]<=0;
white[ 416 ]<=0;
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white[ 422 ]<=1;
white[ 423 ]<=1;
white[ 424 ]<=1;
white[ 425 ]<=1;
white[ 426 ]<=1;
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white[ 438 ]<=1;
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white[ 461 ]<=1;
white[ 462 ]<=0;
white[ 463 ]<=0;
white[ 464 ]<=0;
white[ 465 ]<=0;
white[ 466 ]<=0;
white[ 467 ]<=0;
```

```
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white[ 470 ]<=1;
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white[ 473 ]<=1;
white[ 474 ]<=1;
white[ 475 ]<=1;
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white[ 578 ]<=1;
white[ 579 ]<=1;
white[ 580 ]<=1;
white[ 581 ]<=1;
white[ 582 ]<=1;
white[ 583 ]<=1;
```

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white[ 638 ]<=1;
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white[ 694 ]<=1;
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white[ 810 ]<=1;
white[ 811 ]<=1;
white[ 812 ]<=1;
white[ 813 ]<=1;
white[ 814 ]<=1;
white[ 815 ]<=1;
```

```
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white[ 822 ]<=1;
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white[ 870 ]<=1;
white[ 871 ]<=1;
white[ 872 ]<=1;
white[ 873 ]<=1;
```

```
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white[ 879 ]<=1;
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white[ 927 ]<=0;
white[ 928 ]<=0;
white[ 929 ]<=0;
white[ 930 ]<=0;
white[ 931 ]<=0;
```

```
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white[ 938 ]<=0;
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white[ 985 ]<=0;
white[ 986 ]<=0;
white[ 987 ]<=0;
white[ 988 ]<=0;
white[ 989 ]<=0;
```

```
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white[ 995 ]<=0;
white[ 996 ]<=0;
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white[ 1009 ]<=0;
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white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

P:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 10 ]<=0;
white[ 11 ]<=0;
white[ 12 ]<=0;
white[ 13 ]<=0;
white[ 14 ]<=0;
white[ 15 ]<=0;
white[ 16 ]<=0;
white[ 17 ]<=0;
white[ 18 ]<=0;
white[ 19 ]<=0;
white[ 20 ]<=0;
```

```
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white[ 72 ]<=0;
white[ 73 ]<=0;
white[ 74 ]<=0;
white[ 75 ]<=0;
white[ 76 ]<=0;
white[ 77 ]<=0;
white[ 78 ]<=0;
```

```
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white[ 130 ]<=0;
white[ 131 ]<=1;
white[ 132 ]<=1;
white[ 133 ]<=1;
white[ 134 ]<=1;
white[ 135 ]<=1;
white[ 136 ]<=1;
```

```
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white[ 188 ]<=0;
white[ 189 ]<=0;
white[ 190 ]<=0;
white[ 191 ]<=0;
white[ 192 ]<=0;
white[ 193 ]<=0;
white[ 194 ]<=0;
```

```
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```
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white[ 306 ]<=1;
white[ 307 ]<=1;
white[ 308 ]<=1;
white[ 309 ]<=1;
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white[ 420 ]<=0;
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```

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```

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```
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```

```
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white[ 1001 ]<=0;
white[ 1002 ]<=0;
white[ 1003 ]<=0;
white[ 1004 ]<=0;
white[ 1005 ]<=0;
white[ 1006 ]<=0;
```

```
white[ 1007 ]<=0;
white[ 1008 ]<=0;
white[ 1009 ]<=0;
white[ 1010 ]<=0;
white[ 1011 ]<=0;
white[ 1012 ]<=0;
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white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

Q:begin
white[ 0 ]<=0;
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white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 31 ]<=0;
white[ 32 ]<=0;
white[ 33 ]<=0;
white[ 34 ]<=0;
white[ 35 ]<=0;
white[ 36 ]<=0;
white[ 37 ]<=0;
```

```
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white[ 954 ]<=1;
white[ 955 ]<=1;
white[ 956 ]<=1;
white[ 957 ]<=0;
white[ 958 ]<=0;
white[ 959 ]<=0;
white[ 960 ]<=0;
white[ 961 ]<=0;
white[ 962 ]<=0;
white[ 963 ]<=0;
white[ 964 ]<=0;
white[ 965 ]<=0;
```

```
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white[ 967 ]<=0;
white[ 968 ]<=0;
white[ 969 ]<=0;
white[ 970 ]<=0;
white[ 971 ]<=1;
white[ 972 ]<=0;
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white[ 1019 ]<=1;
white[ 1020 ]<=1;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
```

```
end

R:begin
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white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
white[ 7 ]<=0;
white[ 8 ]<=0;
white[ 9 ]<=0;
white[ 10 ]<=0;
white[ 11 ]<=0;
white[ 12 ]<=0;
white[ 13 ]<=0;
white[ 14 ]<=0;
white[ 15 ]<=0;
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white[ 48 ]<=0;
white[ 49 ]<=0;
white[ 50 ]<=0;
white[ 51 ]<=0;
white[ 52 ]<=0;
white[ 53 ]<=0;
white[ 54 ]<=0;
```

```
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white[ 108 ]<=0;
white[ 109 ]<=0;
white[ 110 ]<=0;
white[ 111 ]<=0;
white[ 112 ]<=0;
```

```
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```
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```

```
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white[ 340 ]<=1;
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white[ 342 ]<=1;
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```

```
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white[ 352 ]<=0;
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white[ 396 ]<=1;
white[ 397 ]<=1;
white[ 398 ]<=0;
white[ 399 ]<=0;
white[ 400 ]<=1;
white[ 401 ]<=1;
white[ 402 ]<=1;
```

```
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white[ 410 ]<=1;
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white[ 454 ]<=1;
white[ 455 ]<=1;
white[ 456 ]<=1;
white[ 457 ]<=1;
white[ 458 ]<=1;
white[ 459 ]<=1;
white[ 460 ]<=1;
```

```
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white[ 512 ]<=0;
white[ 513 ]<=0;
white[ 514 ]<=0;
white[ 515 ]<=1;
white[ 516 ]<=1;
white[ 517 ]<=1;
white[ 518 ]<=1;
```

```
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white[ 523 ]<=1;
white[ 524 ]<=1;
white[ 525 ]<=1;
white[ 526 ]<=1;
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white[ 572 ]<=0;
white[ 573 ]<=0;
white[ 574 ]<=0;
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```

```
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white[ 629 ]<=1;
white[ 630 ]<=1;
white[ 631 ]<=1;
white[ 632 ]<=1;
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white[ 634 ]<=1;
```

```
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white[ 688 ]<=1;
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white[ 692 ]<=1;
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```
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white[ 866 ]<=1;
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white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

S:begin
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white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
white[ 7 ]<=0;
white[ 8 ]<=0;
white[ 9 ]<=0;
white[ 10 ]<=0;
white[ 11 ]<=0;
white[ 12 ]<=0;
white[ 13 ]<=0;
```

```
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white[ 67 ]<=0;
white[ 68 ]<=0;
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```

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```

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```

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```

```
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```

```
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```
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white[ 645 ]<=1;
white[ 646 ]<=1;
white[ 647 ]<=1;
white[ 648 ]<=1;
white[ 649 ]<=1;
white[ 650 ]<=0;
white[ 651 ]<=0;
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white[ 653 ]<=0;
white[ 654 ]<=0;
white[ 655 ]<=0;
white[ 656 ]<=1;
white[ 657 ]<=1;
white[ 658 ]<=1;
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white[ 664 ]<=1;
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white[ 704 ]<=0;
white[ 705 ]<=0;
white[ 706 ]<=0;
white[ 707 ]<=1;
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white[ 709 ]<=1;
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white[ 715 ]<=1;
white[ 716 ]<=1;
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white[ 762 ]<=1;
white[ 763 ]<=1;
white[ 764 ]<=1;
white[ 765 ]<=0;
white[ 766 ]<=0;
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white[ 823 ]<=1;
white[ 824 ]<=1;
white[ 825 ]<=1;
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white[ 879 ]<=1;
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white[ 881 ]<=1;
white[ 882 ]<=1;
white[ 883 ]<=1;
```

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white[ 889 ]<=1;
white[ 890 ]<=0;
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white[ 937 ]<=1;
white[ 938 ]<=0;
white[ 939 ]<=0;
white[ 940 ]<=0;
white[ 941 ]<=0;
```

```
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white[ 947 ]<=1;
white[ 948 ]<=1;
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white[ 993 ]<=0;
white[ 994 ]<=0;
white[ 995 ]<=0;
white[ 996 ]<=0;
white[ 997 ]<=0;
white[ 998 ]<=0;
white[ 999 ]<=0;
```

```
white[ 1000 ]<=0;
white[ 1001 ]<=0;
white[ 1002 ]<=0;
white[ 1003 ]<=0;
white[ 1004 ]<=0;
white[ 1005 ]<=0;
white[ 1006 ]<=0;
white[ 1007 ]<=0;
white[ 1008 ]<=0;
white[ 1009 ]<=0;
white[ 1010 ]<=0;
white[ 1011 ]<=0;
white[ 1012 ]<=0;
white[ 1013 ]<=0;
white[ 1014 ]<=0;
white[ 1015 ]<=0;
white[ 1016 ]<=0;
white[ 1017 ]<=0;
white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

T:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 25 ]<=0;
white[ 26 ]<=0;
white[ 27 ]<=0;
white[ 28 ]<=0;
white[ 29 ]<=0;
white[ 30 ]<=0;
```

```
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white[ 35 ]<=0;
white[ 36 ]<=0;
white[ 37 ]<=0;
white[ 38 ]<=0;
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white[ 82 ]<=0;
white[ 83 ]<=0;
white[ 84 ]<=0;
white[ 85 ]<=0;
white[ 86 ]<=0;
white[ 87 ]<=0;
white[ 88 ]<=0;
```

```
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white[ 94 ]<=0;
white[ 95 ]<=0;
white[ 96 ]<=0;
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white[ 140 ]<=0;
white[ 141 ]<=0;
white[ 142 ]<=0;
white[ 143 ]<=0;
white[ 144 ]<=0;
white[ 145 ]<=0;
white[ 146 ]<=0;
```

```
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white[ 198 ]<=1;
white[ 199 ]<=1;
white[ 200 ]<=1;
white[ 201 ]<=1;
white[ 202 ]<=1;
white[ 203 ]<=1;
white[ 204 ]<=1;
```

```
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white[ 256 ]<=0;
white[ 257 ]<=0;
white[ 258 ]<=0;
white[ 259 ]<=0;
white[ 260 ]<=1;
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white[ 262 ]<=1;
```

```
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white[ 270 ]<=1;
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white[ 320 ]<=0;
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white[ 373 ]<=1;
white[ 374 ]<=1;
white[ 375 ]<=1;
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white[ 378 ]<=1;
```

```
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white[ 434 ]<=1;
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```
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white[ 475 ]<=1;
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white[ 477 ]<=0;
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white[ 479 ]<=0;
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white[ 486 ]<=0;
white[ 487 ]<=0;
white[ 488 ]<=0;
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white[ 490 ]<=1;
white[ 491 ]<=1;
white[ 492 ]<=1;
white[ 493 ]<=1;
white[ 494 ]<=1;
```

```
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white[ 499 ]<=1;
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white[ 607 ]<=0;
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white[ 779 ]<=1;
white[ 780 ]<=1;
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white[ 782 ]<=1;
white[ 783 ]<=1;
white[ 784 ]<=1;
```

```
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white[ 837 ]<=0;
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white[ 839 ]<=0;
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white[ 842 ]<=1;
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```
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white[ 848 ]<=1;
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white[ 895 ]<=0;
white[ 896 ]<=0;
white[ 897 ]<=0;
white[ 898 ]<=0;
white[ 899 ]<=0;
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```

```
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white[ 906 ]<=1;
white[ 907 ]<=1;
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white[ 954 ]<=0;
white[ 955 ]<=0;
white[ 956 ]<=0;
white[ 957 ]<=0;
white[ 958 ]<=0;
```

```
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white[ 962 ]<=0;
white[ 963 ]<=0;
white[ 964 ]<=0;
white[ 965 ]<=0;
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white[ 985 ]<=0;
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white[ 1013 ]<=0;
white[ 1014 ]<=0;
white[ 1015 ]<=0;
white[ 1016 ]<=0;
```

```
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white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

U:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 45 ]<=0;
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white[ 47 ]<=0;
```

```
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white[ 99 ]<=0;
white[ 100 ]<=0;
white[ 101 ]<=0;
white[ 102 ]<=0;
white[ 103 ]<=0;
white[ 104 ]<=0;
white[ 105 ]<=0;
```

```
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white[ 159 ]<=0;
white[ 160 ]<=0;
white[ 161 ]<=0;
white[ 162 ]<=0;
white[ 163 ]<=0;
```

```
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white[ 215 ]<=1;
white[ 216 ]<=1;
white[ 217 ]<=1;
white[ 218 ]<=1;
white[ 219 ]<=1;
white[ 220 ]<=1;
white[ 221 ]<=1;
```

```
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white[ 273 ]<=1;
white[ 274 ]<=1;
white[ 275 ]<=0;
white[ 276 ]<=1;
white[ 277 ]<=1;
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white[ 279 ]<=1;
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```
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white[ 318 ]<=0;
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white[ 320 ]<=0;
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white[ 331 ]<=1;
white[ 332 ]<=1;
white[ 333 ]<=1;
white[ 334 ]<=1;
white[ 335 ]<=1;
white[ 336 ]<=1;
white[ 337 ]<=1;
```

```
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white[ 389 ]<=1;
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white[ 391 ]<=1;
white[ 392 ]<=1;
white[ 393 ]<=1;
white[ 394 ]<=1;
white[ 395 ]<=1;
```

```
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```

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white[ 507 ]<=1;
white[ 508 ]<=1;
white[ 509 ]<=1;
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white[ 511 ]<=0;
```

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```
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white[ 622 ]<=1;
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white[ 626 ]<=1;
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white[ 683 ]<=1;
white[ 684 ]<=1;
white[ 685 ]<=1;
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white[ 741 ]<=0;
white[ 742 ]<=1;
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white[ 799 ]<=0;
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white[ 857 ]<=1;
white[ 858 ]<=1;
white[ 859 ]<=1;
```

```
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white[ 865 ]<=0;
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white[ 913 ]<=1;
white[ 914 ]<=1;
white[ 915 ]<=1;
white[ 916 ]<=1;
white[ 917 ]<=1;
```

```
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white[ 971 ]<=0;
white[ 972 ]<=0;
white[ 973 ]<=0;
white[ 974 ]<=0;
white[ 975 ]<=0;
```

```
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white[ 981 ]<=0;
white[ 982 ]<=0;
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white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

V:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
```

```
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white[ 8 ]<=0;
white[ 9 ]<=0;
white[ 10 ]<=0;
white[ 11 ]<=0;
white[ 12 ]<=0;
white[ 13 ]<=0;
white[ 14 ]<=0;
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white[ 58 ]<=0;
white[ 59 ]<=0;
white[ 60 ]<=0;
white[ 61 ]<=0;
white[ 62 ]<=0;
white[ 63 ]<=0;
white[ 64 ]<=0;
```

```
white[ 65 ]<=0;
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white[ 70 ]<=0;
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white[ 116 ]<=0;
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white[ 118 ]<=0;
white[ 119 ]<=0;
white[ 120 ]<=0;
white[ 121 ]<=0;
white[ 122 ]<=0;
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white[ 1018 ]<=0;
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white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
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W:begin
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white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 19 ]<=0;
white[ 20 ]<=0;
white[ 21 ]<=0;
white[ 22 ]<=0;
white[ 23 ]<=0;
```

```
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white[ 483 ]<=1;
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```
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```
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white[ 887 ]<=1;
white[ 888 ]<=1;
white[ 889 ]<=1;
white[ 890 ]<=1;
white[ 891 ]<=1;
white[ 892 ]<=1;
white[ 893 ]<=0;
```

```
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white[ 895 ]<=0;
white[ 896 ]<=0;
white[ 897 ]<=0;
white[ 898 ]<=0;
white[ 899 ]<=1;
white[ 900 ]<=1;
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white[ 946 ]<=0;
white[ 947 ]<=0;
white[ 948 ]<=0;
white[ 949 ]<=0;
white[ 950 ]<=0;
white[ 951 ]<=0;
```

```
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white[ 957 ]<=0;
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white[ 1005 ]<=0;
white[ 1006 ]<=0;
white[ 1007 ]<=0;
white[ 1008 ]<=0;
white[ 1009 ]<=0;
```

```
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white[ 1011 ]<=0;
white[ 1012 ]<=0;
white[ 1013 ]<=0;
white[ 1014 ]<=0;
white[ 1015 ]<=0;
white[ 1016 ]<=0;
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white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

X:begin
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 35 ]<=0;
white[ 36 ]<=0;
white[ 37 ]<=0;
white[ 38 ]<=0;
white[ 39 ]<=0;
white[ 40 ]<=0;
```

```
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white[ 46 ]<=0;
white[ 47 ]<=0;
white[ 48 ]<=0;
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white[ 92 ]<=0;
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white[ 94 ]<=0;
white[ 95 ]<=0;
white[ 96 ]<=0;
white[ 97 ]<=0;
white[ 98 ]<=0;
```

```
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white[ 103 ]<=0;
white[ 104 ]<=0;
white[ 105 ]<=0;
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white[ 152 ]<=0;
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white[ 154 ]<=0;
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white[ 156 ]<=0;
```

```
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white[ 209 ]<=1;
white[ 210 ]<=1;
white[ 211 ]<=1;
white[ 212 ]<=1;
white[ 213 ]<=1;
white[ 214 ]<=1;
```

```
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white[ 268 ]<=1;
white[ 269 ]<=1;
white[ 270 ]<=1;
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white[ 272 ]<=1;
```

```
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white[ 280 ]<=1;
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white[ 328 ]<=1;
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```

```
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white[ 382 ]<=0;
white[ 383 ]<=0;
white[ 384 ]<=0;
white[ 385 ]<=0;
white[ 386 ]<=0;
white[ 387 ]<=0;
white[ 388 ]<=0;
```

```
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```

```
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white[ 499 ]<=1;
white[ 500 ]<=1;
white[ 501 ]<=1;
white[ 502 ]<=1;
white[ 503 ]<=1;
white[ 504 ]<=1;
```

```
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white[ 508 ]<=0;
white[ 509 ]<=0;
white[ 510 ]<=0;
white[ 511 ]<=0;
white[ 512 ]<=0;
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white[ 557 ]<=1;
white[ 558 ]<=1;
white[ 559 ]<=1;
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white[ 562 ]<=1;
```

```
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white[ 615 ]<=0;
white[ 616 ]<=1;
white[ 617 ]<=1;
white[ 618 ]<=1;
white[ 619 ]<=1;
white[ 620 ]<=1;
```

```
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white[ 627 ]<=1;
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white[ 673 ]<=0;
white[ 674 ]<=0;
white[ 675 ]<=0;
white[ 676 ]<=0;
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white[ 678 ]<=0;
```

```
white[ 679 ]<=1;
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white[ 692 ]<=1;
white[ 693 ]<=1;
white[ 694 ]<=1;
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white[ 697 ]<=1;
white[ 698 ]<=1;
white[ 699 ]<=0;
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white[ 701 ]<=0;
white[ 702 ]<=0;
white[ 703 ]<=0;
white[ 704 ]<=0;
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white[ 706 ]<=0;
white[ 707 ]<=0;
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white[ 731 ]<=1;
white[ 732 ]<=0;
white[ 733 ]<=0;
white[ 734 ]<=0;
white[ 735 ]<=0;
white[ 736 ]<=0;
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white[ 742 ]<=1;
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white[ 789 ]<=1;
white[ 790 ]<=1;
white[ 791 ]<=1;
white[ 792 ]<=1;
white[ 793 ]<=1;
white[ 794 ]<=1;
```

```
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white[ 799 ]<=0;
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white[ 847 ]<=1;
white[ 848 ]<=1;
white[ 849 ]<=1;
white[ 850 ]<=1;
white[ 851 ]<=1;
white[ 852 ]<=1;
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white[ 858 ]<=1;
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white[ 887 ]<=1;
white[ 888 ]<=1;
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white[ 891 ]<=1;
white[ 892 ]<=1;
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white[ 894 ]<=1;
white[ 895 ]<=0;
white[ 896 ]<=0;
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white[ 898 ]<=1;
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white[ 902 ]<=1;
white[ 903 ]<=1;
white[ 904 ]<=1;
white[ 905 ]<=1;
white[ 906 ]<=1;
white[ 907 ]<=1;
white[ 908 ]<=1;
white[ 909 ]<=1;
white[ 910 ]<=1;
```

```
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white[ 914 ]<=1;
white[ 915 ]<=1;
white[ 916 ]<=1;
white[ 917 ]<=1;
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white[ 964 ]<=0;
white[ 965 ]<=0;
white[ 966 ]<=0;
white[ 967 ]<=0;
white[ 968 ]<=0;
```

```
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white[ 970 ]<=0;
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white[ 972 ]<=0;
white[ 973 ]<=0;
white[ 974 ]<=0;
white[ 975 ]<=0;
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white[ 1007 ]<=0;
white[ 1008 ]<=0;
white[ 1009 ]<=0;
white[ 1010 ]<=0;
white[ 1011 ]<=0;
white[ 1012 ]<=0;
white[ 1013 ]<=0;
white[ 1014 ]<=0;
white[ 1015 ]<=0;
white[ 1016 ]<=0;
white[ 1017 ]<=0;
white[ 1018 ]<=0;
white[ 1019 ]<=0;
white[ 1020 ]<=0;
white[ 1021 ]<=0;
white[ 1022 ]<=0;
white[ 1023 ]<=0;
end

Y:begin
```

```
white[ 0 ]<=0;
white[ 1 ]<=0;
white[ 2 ]<=0;
white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
white[ 6 ]<=0;
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white[ 52 ]<=0;
white[ 53 ]<=0;
white[ 54 ]<=0;
white[ 55 ]<=0;
white[ 56 ]<=0;
white[ 57 ]<=0;
```

```
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white[ 65 ]<=0;
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white[ 109 ]<=0;
white[ 110 ]<=0;
white[ 111 ]<=0;
white[ 112 ]<=0;
white[ 113 ]<=0;
white[ 114 ]<=0;
white[ 115 ]<=0;
```

```
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white[ 123 ]<=0;
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white[ 169 ]<=0;
white[ 170 ]<=0;
white[ 171 ]<=0;
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```

```
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white[ 225 ]<=0;
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white[ 227 ]<=1;
white[ 228 ]<=1;
white[ 229 ]<=1;
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```

```
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white[ 239 ]<=0;
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```

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white[ 345 ]<=1;
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```

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white[ 399 ]<=1;
white[ 400 ]<=1;
white[ 401 ]<=1;
white[ 402 ]<=1;
white[ 403 ]<=1;
white[ 404 ]<=1;
white[ 405 ]<=1;
```

```
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white[ 412 ]<=0;
white[ 413 ]<=0;
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white[ 457 ]<=1;
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white[ 459 ]<=1;
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white[ 463 ]<=1;
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```
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white[ 515 ]<=0;
white[ 516 ]<=0;
white[ 517 ]<=0;
white[ 518 ]<=0;
white[ 519 ]<=1;
white[ 520 ]<=1;
white[ 521 ]<=1;
```

```
white[ 522 ]<=1;
white[ 523 ]<=1;
white[ 524 ]<=1;
white[ 525 ]<=1;
white[ 526 ]<=1;
white[ 527 ]<=1;
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Z: begin
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white[ 361 ]<=1;
white[ 362 ]<=1;
white[ 363 ]<=1;
white[ 364 ]<=1;
```

```
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white[ 369 ]<=1;
white[ 370 ]<=1;
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white[ 372 ]<=1;
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white[ 379 ]<=0;
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white[ 382 ]<=0;
white[ 383 ]<=0;
white[ 384 ]<=0;
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white[ 388 ]<=1;
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white[ 396 ]<=1;
white[ 397 ]<=1;
white[ 398 ]<=1;
white[ 399 ]<=1;
white[ 400 ]<=1;
white[ 401 ]<=1;
white[ 402 ]<=1;
white[ 403 ]<=1;
white[ 404 ]<=1;
white[ 405 ]<=1;
white[ 406 ]<=1;
white[ 407 ]<=1;
white[ 408 ]<=0;
white[ 409 ]<=0;
white[ 410 ]<=1;
white[ 411 ]<=0;
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white[ 413 ]<=0;
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white[ 415 ]<=0;
white[ 416 ]<=0;
white[ 417 ]<=0;
white[ 418 ]<=0;
white[ 419 ]<=0;
white[ 420 ]<=1;
white[ 421 ]<=1;
white[ 422 ]<=1;
```

```
white[ 423 ]<=1;
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white[ 429 ]<=1;
white[ 430 ]<=1;
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white[ 434 ]<=1;
white[ 435 ]<=1;
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white[ 437 ]<=1;
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white[ 439 ]<=1;
white[ 440 ]<=0;
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white[ 455 ]<=0;
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white[ 473 ]<=0;
white[ 474 ]<=0;
white[ 475 ]<=0;
white[ 476 ]<=0;
white[ 477 ]<=0;
white[ 478 ]<=0;
white[ 479 ]<=0;
white[ 480 ]<=0;
```

```
white[ 481 ]<=0;
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white[ 483 ]<=0;
white[ 484 ]<=0;
white[ 485 ]<=0;
white[ 486 ]<=0;
white[ 487 ]<=1;
white[ 488 ]<=0;
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white[ 536 ]<=0;
white[ 537 ]<=0;
white[ 538 ]<=0;
```

```
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white[ 578 ]<=0;
white[ 579 ]<=0;
white[ 580 ]<=0;
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white[ 585 ]<=1;
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white[ 589 ]<=1;
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white[ 591 ]<=1;
white[ 592 ]<=1;
white[ 593 ]<=1;
white[ 594 ]<=1;
white[ 595 ]<=1;
white[ 596 ]<=0;
```

```
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white[ 598 ]<=0;
white[ 599 ]<=0;
white[ 600 ]<=0;
white[ 601 ]<=1;
white[ 602 ]<=1;
white[ 603 ]<=0;
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white[ 605 ]<=0;
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white[ 608 ]<=0;
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white[ 635 ]<=1;
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white[ 639 ]<=0;
white[ 640 ]<=0;
white[ 641 ]<=0;
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white[ 651 ]<=1;
white[ 652 ]<=1;
white[ 653 ]<=1;
white[ 654 ]<=1;
```

```
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white[ 696 ]<=1;
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white[ 707 ]<=0;
white[ 708 ]<=0;
white[ 709 ]<=0;
white[ 710 ]<=1;
white[ 711 ]<=1;
white[ 712 ]<=1;
```

```
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white[ 716 ]<=1;
white[ 717 ]<=1;
white[ 718 ]<=1;
white[ 719 ]<=1;
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white[ 723 ]<=1;
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white[ 765 ]<=0;
white[ 766 ]<=0;
white[ 767 ]<=0;
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```

```
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white[ 776 ]<=1;
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white[ 823 ]<=1;
white[ 824 ]<=1;
white[ 825 ]<=1;
white[ 826 ]<=1;
white[ 827 ]<=1;
white[ 828 ]<=0;
```

```
white[ 829 ]<=0;
white[ 830 ]<=0;
white[ 831 ]<=0;
white[ 832 ]<=0;
white[ 833 ]<=0;
white[ 834 ]<=0;
white[ 835 ]<=0;
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white[ 882 ]<=1;
white[ 883 ]<=1;
white[ 884 ]<=1;
white[ 885 ]<=1;
white[ 886 ]<=1;
```

```
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white[ 889 ]<=0;
white[ 890 ]<=0;
white[ 891 ]<=0;
white[ 892 ]<=0;
white[ 893 ]<=0;
white[ 894 ]<=0;
white[ 895 ]<=0;
white[ 896 ]<=0;
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white[ 903 ]<=1;
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white[ 940 ]<=0;
white[ 941 ]<=0;
white[ 942 ]<=0;
white[ 943 ]<=0;
white[ 944 ]<=0;
```

```
white[ 945 ]<=0;
white[ 946 ]<=0;
white[ 947 ]<=0;
white[ 948 ]<=0;
white[ 949 ]<=0;
white[ 950 ]<=0;
white[ 951 ]<=0;
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white[ 992 ]<=0;
white[ 993 ]<=0;
white[ 994 ]<=0;
white[ 995 ]<=0;
white[ 996 ]<=0;
white[ 997 ]<=0;
white[ 998 ]<=0;
white[ 999 ]<=0;
white[ 1000 ]<=0;
white[ 1001 ]<=0;
white[ 1002 ]<=0;
```

```
                white[ 1003 ]<=0;
                white[ 1004 ]<=0;
                white[ 1005 ]<=0;
                white[ 1006 ]<=0;
                white[ 1007 ]<=0;
                white[ 1008 ]<=0;
                white[ 1009 ]<=0;
                white[ 1010 ]<=0;
                white[ 1011 ]<=0;
                white[ 1012 ]<=0;
                white[ 1013 ]<=0;
                white[ 1014 ]<=0;
                white[ 1015 ]<=0;
                white[ 1016 ]<=0;
                white[ 1017 ]<=0;
                white[ 1018 ]<=0;
                white[ 1019 ]<=0;
                white[ 1020 ]<=0;
                white[ 1021 ]<=0;
                white[ 1022 ]<=0;
                white[ 1023 ]<=0;
                end
                endcase
        end
end

always@(posedge iclk or negedge ireset_n)
begin
    if(!ireset_n)
        begin
            address <= 18'bZ;
        end
    else
        case(iletter)
        A: address <= A_base;
        B: address <= B_base;
        C: address <= C_base;
        D: address <= D_base;
        E: address <= E_base;
        F: address <= F_base;
        G: address <= G_base;
        H: address <= H_base;
        I: address <= I_base;
        J: address <= J_base;
        K: address <= K_base;
        L: address <= L_base;
        M: address <= M_base;
        N: address <= N_base;
        O: address <= O_base;
        P: address <= P_base;
        Q: address <= Q_base;
        R: address <= R_base;
        S: address <= S_base;
        T: address <= T_base;
        U: address <= U_base;
        V: address <= V_base;
        W: address <= W_base;
        X: address <= X_base;
```

```
            Y: address <= Y_base;
            Z: address <= Z_base;
        endcase
end

always@(posedge iclk or negedge ireset_n)
begin
        if(!ireset_n)
        begin
            oOVERRIDE<= 0;
            oADDR <= 18'bZ;
            counter <= 5'd31;
        end
        else if(display_area)
        begin
            if(counter == 0)
                counter <= 5'd31;
            else
                counter <= counter-1;
            oOVERRIDE <= white[counter + 32*(iy_cnt-iletter_pos_y)];
            oADDR <= address + counter + 32*(iy_cnt-iletter_pos_y);
        end
        else
        begin
            oOVERRIDE <= 0;
            oADDR <= 18'bZ;
        end
end

endmodule
```

life.v

```
module Life(
                clk_ltm,
                reset_n,
                x_cnt,
                y_cnt,
                life,
                oOVERRIDE,
                oADDR
                );

input clk_ltm;
input reset_n;
input [10:0] x_cnt;
input [9:0] y_cnt;
input [3:0]life;
output oOVERRIDE;
output [17:0] oADDR;
//PARAMETER
parameter BASE_ADDR = 89025;
parameter INIT = 2'b00;
parameter START = 2'b01;
parameter PAUSE = 2'b10;
parameter H_LINE = 1056;
```

```
parameter V_LINE = 525;
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
parameter Vertical_Front_Porch = 10;
parameter heart_base = 18'd92639;
//WIRE & REG
wire [17:0] address;
wire [1:0] OVERRIDE;
symbol heart(
                        .iclk(clk_ltm),
                        .ireset_n(reset_n),
                        .ix_cnt(x_cnt),
                        .iy_cnt(y_cnt),
                        .isymbol_pos_x(Hsync_Blank-1+730),
                        .isymbol_pos_y(Vertical_Back_Porch+90),
                        .iBASE_ADDR(heart_base),
                        .oOVERRIDE(OVERRIDE[1]),
                        .oADDR(address)
);

number life1(
                        .iclk(clk_ltm),
                        .iReset_n(reset_n),
                        .ixcount(x_cnt),
                        .iycount(y_cnt),
                        .iled_pos_x(Hsync_Blank-1+600),
                        .iled_pos_y(Vertical_Back_Porch+80),
                        .inumber(life),
                        .oOVERRIDE(OVERRIDE[0])
);

////OUTPUT
assign oOVERRIDE = OVERRIDE[0] || OVERRIDE[1];
assign oADDR = OVERRIDE[0] ? BASE_ADDR :
                            OVERRIDE[1] ? address : 18'bZ;

endmodule
```

lose.v

```
module lose(
                        iclk,
                        ireset_n,
                        ix_cnt,
                        iy_cnt,
                        oADDR);

//=============================================
//Parameter=============================
//=============================================
parameter A = 5'd1;
parameter B = 5'd2;
parameter C = 5'd3;
parameter D = 5'd4;
```

```
parameter E = 5'd5;
parameter F = 5'd6;
parameter G = 5'd7;
parameter H = 5'd8;
parameter I = 5'd9;
parameter J = 5'd10;
parameter K = 5'd11;
parameter L = 5'd12;
parameter M = 5'd13;
parameter N = 5'd14;
parameter O = 5'd15;
parameter P = 5'd16;
parameter Q = 5'd17;
parameter R = 5'd18;
parameter S = 5'd19;
parameter T = 5'd20;
parameter U = 5'd21;
parameter V = 5'd22;
parameter W = 5'd23;
parameter X = 5'd24;
parameter Y = 5'd25;
parameter Z = 5'd26;

parameter H_LINE = 1056;
parameter V_LINE = 525;
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
parameter Vertical_Front_Porch = 10;
//=============================================
//I/O DECALARATION=============================
//=============================================
input iclk;
input ireset_n;
input [10:0] ix_cnt;
input [9:0] iy_cnt;
output [17:0] oADDR;

//=============================================
//WIRE & REG===================================
//=============================================
wire [4:0] letter[0:20];
wire [10:0] letter_pos_x[0:20];
wire [9:0] letter_pos_y[0:20];
wire [20:0] override;
wire [17:0] address[0:20];
reg [17:0] oADDR;
//=============================================
//Structured logic=============================
//=============================================
//Assign Letters
assign letter[0] = Y;
assign letter[1] = O;
assign letter[2] = U;
assign letter[3] = L;
assign letter[4] = O;
assign letter[5] = S;
assign letter[6] = E;
```

```
assign letter[7] = P;
assign letter[8] = L;
assign letter[9] = E;
assign letter[10] = A;
assign letter[11] = S;
assign letter[12] = E;
assign letter[13] = T;
assign letter[14] = R;
assign letter[15] = Y;
assign letter[16] = A;
assign letter[17] = G;
assign letter[18] = A;
assign letter[19] = I;
assign letter[20] = N;


//assign letter position
assign letter_pos_x[0] = Hsync_Blank-2+496;
assign letter_pos_x[1] = Hsync_Blank-2+464;
assign letter_pos_x[2] = Hsync_Blank-2+432;
assign letter_pos_x[3] = Hsync_Blank-2+368;
assign letter_pos_x[4] = Hsync_Blank-2+336;
assign letter_pos_x[5] = Hsync_Blank-2+304;
assign letter_pos_x[6] = Hsync_Blank-2+272;

assign letter_pos_x[7] = Hsync_Blank-2+624;
assign letter_pos_x[8] = Hsync_Blank-2+592;
assign letter_pos_x[9] = Hsync_Blank-2+560;
assign letter_pos_x[10] = Hsync_Blank-2+528;
assign letter_pos_x[11] = Hsync_Blank-2+496;
assign letter_pos_x[12] = Hsync_Blank-2+464;

assign letter_pos_x[13] = Hsync_Blank-2+400;
assign letter_pos_x[14] = Hsync_Blank-2+368;
assign letter_pos_x[15] = Hsync_Blank-2+336;

assign letter_pos_x[16] = Hsync_Blank-2+272;
assign letter_pos_x[17] = Hsync_Blank-2+240;
assign letter_pos_x[18] = Hsync_Blank-2+208;
assign letter_pos_x[19] = Hsync_Blank-2+176;
assign letter_pos_x[20] = Hsync_Blank-2+144;


assign letter_pos_y[0] = Vertical_Back_Porch-1+160;
assign letter_pos_y[1] = Vertical_Back_Porch-1+160;
assign letter_pos_y[2] = Vertical_Back_Porch-1+160;
assign letter_pos_y[3] = Vertical_Back_Porch-1+160;
assign letter_pos_y[4] = Vertical_Back_Porch-1+160;
assign letter_pos_y[5] = Vertical_Back_Porch-1+160;
assign letter_pos_y[6] = Vertical_Back_Porch-1+160;

assign letter_pos_y[7] = Vertical_Back_Porch-1+240;
assign letter_pos_y[8] = Vertical_Back_Porch-1+240;
assign letter_pos_y[9] = Vertical_Back_Porch-1+240;
assign letter_pos_y[10] = Vertical_Back_Porch-1+240;
assign letter_pos_y[11] = Vertical_Back_Porch-1+240;
assign letter_pos_y[12] = Vertical_Back_Porch-1+240;
assign letter_pos_y[13] = Vertical_Back_Porch-1+240;
```

```
assign letter_pos_y[14] = Vertical_Back_Porch-1+240;
assign letter_pos_y[15] = Vertical_Back_Porch-1+240;
assign letter_pos_y[16] = Vertical_Back_Porch-1+240;
assign letter_pos_y[17] = Vertical_Back_Porch-1+240;
assign letter_pos_y[18] = Vertical_Back_Porch-1+240;
assign letter_pos_y[19] = Vertical_Back_Porch-1+240;
assign letter_pos_y[20] = Vertical_Back_Porch-1+240;


letter letter0(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[0]),
                        .iletter_pos_y(letter_pos_y[0]),
                        .iletter(letter[0]),
                        .oOVERRIDE(override[0]),
                        .oADDR(address[0])
                        );

letter letter1(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[1]),
                        .iletter_pos_y(letter_pos_y[1]),
                        .iletter(letter[1]),
                        .oOVERRIDE(override[1]),
                        .oADDR(address[1])
                        );

letter letter2(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[2]),
                        .iletter_pos_y(letter_pos_y[2]),
                        .iletter(letter[2]),
                        .oOVERRIDE(override[2]),
                        .oADDR(address[2])
                        );

letter letter3(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[3]),
                        .iletter_pos_y(letter_pos_y[3]),
                        .iletter(letter[3]),
                        .oOVERRIDE(override[3]),
                        .oADDR(address[3])
                        );

letter letter4(
```

```
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[4]),
                .iletter_pos_y(letter_pos_y[4]),
                .iletter(letter[4]),
                .oOVERRIDE(override[4]),
                .oADDR(address[4])
                );

letter letter5(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[5]),
                .iletter_pos_y(letter_pos_y[5]),
                .iletter(letter[5]),
                .oOVERRIDE(override[5]),
                .oADDR(address[5])
                );

letter letter6(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[6]),
                .iletter_pos_y(letter_pos_y[6]),
                .iletter(letter[6]),
                .oOVERRIDE(override[6]),
                .oADDR(address[6])
                );

letter letter7(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[7]),
                .iletter_pos_y(letter_pos_y[7]),
                .iletter(letter[7]),
                .oOVERRIDE(override[7]),
                .oADDR(address[7])
                );

letter letter8(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[8]),
                .iletter_pos_y(letter_pos_y[8]),
                .iletter(letter[8]),
                .oOVERRIDE(override[8]),
                .oADDR(address[8])
                );
```

```
letter letter9(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[9]),
                        .iletter_pos_y(letter_pos_y[9]),
                        .iletter(letter[9]),
                        .oOVERRIDE(override[9]),
                        .oADDR(address[9])
                        );

letter letter10(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[10]),
                        .iletter_pos_y(letter_pos_y[10]),
                        .iletter(letter[10]),
                        .oOVERRIDE(override[10]),
                        .oADDR(address[10])
                        );

letter letter11(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[11]),
                        .iletter_pos_y(letter_pos_y[11]),
                        .iletter(letter[11]),
                        .oOVERRIDE(override[11]),
                        .oADDR(address[11])
                        );

letter letter12(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[12]),
                        .iletter_pos_y(letter_pos_y[12]),
                        .iletter(letter[12]),
                        .oOVERRIDE(override[12]),
                        .oADDR(address[12])
                        );

letter letter13(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[13]),
                        .iletter_pos_y(letter_pos_y[13]),
                        .iletter(letter[13]),
                        .oOVERRIDE(override[13]),
```

```
                .oADDR(address[13])
                );

letter letter14(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[14]),
                .iletter_pos_y(letter_pos_y[14]),
                .iletter(letter[14]),
                .oOVERRIDE(override[14]),
                .oADDR(address[14])
                );

letter letter15(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[15]),
                .iletter_pos_y(letter_pos_y[15]),
                .iletter(letter[15]),
                .oOVERRIDE(override[15]),
                .oADDR(address[15])
                );

letter letter16(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[16]),
                .iletter_pos_y(letter_pos_y[16]),
                .iletter(letter[16]),
                .oOVERRIDE(override[16]),
                .oADDR(address[16])
                );

letter letter17(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[17]),
                .iletter_pos_y(letter_pos_y[17]),
                .iletter(letter[17]),
                .oOVERRIDE(override[17]),
                .oADDR(address[17])
                );

letter letter18(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[18]),
                .iletter_pos_y(letter_pos_y[18]),
```

```
                        .iletter(letter[18]),
                        .oOVERRIDE(override[18]),
                        .oADDR(address[18])
                        );

letter letter19(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[19]),
                        .iletter_pos_y(letter_pos_y[19]),
                        .iletter(letter[19]),
                        .oOVERRIDE(override[19]),
                        .oADDR(address[19])
                        );

letter letter20(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[20]),
                        .iletter_pos_y(letter_pos_y[20]),
                        .iletter(letter[20]),
                        .oOVERRIDE(override[20]),
                        .oADDR(address[20])
                        );


always@(posedge iclk or negedge ireset_n)
begin
      if(!ireset_n)
            oADDR <= 18'bZ;
      else
            case(override)
            21'b000000000000000000001 : oADDR <= address[0];
            21'b000000000000000000010 : oADDR <= address[1];
            21'b000000000000000000100 : oADDR <= address[2];
            21'b000000000000000001000 : oADDR <= address[3];
            21'b000000000000000010000 : oADDR <= address[4];
            21'b000000000000000100000 : oADDR <= address[5];
            21'b000000000000001000000 : oADDR <= address[6];
            21'b000000000000010000000 : oADDR <= address[7];
            21'b000000000000100000000 : oADDR <= address[8];
            21'b000000000001000000000 : oADDR <= address[9];
            21'b000000000010000000000 : oADDR <= address[10];
            21'b000000000100000000000 : oADDR <= address[11];
            21'b000000001000000000000 : oADDR <= address[12];
            21'b000000010000000000000 : oADDR <= address[13];
            21'b000000100000000000000 : oADDR <= address[14];
            21'b000001000000000000000 : oADDR <= address[15];
            21'b000010000000000000000 : oADDR <= address[16];
            21'b000100000000000000000 : oADDR <= address[17];
            21'b001000000000000000000 : oADDR <= address[18];
            21'b010000000000000000000 : oADDR <= address[19];
            21'b100000000000000000000 : oADDR <= address[20];
            default: oADDR <= 18'd89025;
```

```
            endcase;
end

endmodule
```

mole_controller.v

```
module mole_ctrl        (
                        iCLK,                   // LCD display clock
                        iRST_n,             // systen reset
                       x_cnt,
                y_cnt,
                        moleControl,
                        moleExist,
                        mole_address,
                        );
//////=================================================
// for every mole control
//    001 mole up, 000 mole down due to time out
//    101 bottle up, 100 bottle down
//    011 evil up, 010 evil down
//    110 mole hit!!!!
//////=================================================

//=============================================================================
// PARAMETER declarations
//=============================================================================
parameter H_LINE = 1056;
parameter V_LINE = 525;
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
parameter Vertical_Front_Porch = 10;
parameter moleBase = 48000;

parameter bottleOffset = 103439-48000;
parameter evilOffset = 117839-48000;
//=============================================================================
// PORT declarations
//=============================================================================
input                   iCLK;
input                   iRST_n;
input [10:0] x_cnt;
input [9:0] y_cnt;
input [31:0]        moleControl;
output          moleExist;
output[17:0] mole_address;

//=============================================================================
// REG/WIRE declarations
//=============================================================================
wire [15:0] area;
wire [1:0] mole0;
wire [1:0] mole1;
wire [1:0] mole2;
```

```
wire [1:0] mole3;
wire [1:0] mole4;
wire [1:0] mole5;
wire [1:0] mole6;
wire [1:0] mole7;
wire [1:0] mole8;
wire updn0;
wire updn1;
wire updn2;
wire updn3;
wire updn4;
wire updn5;
wire updn6;
wire updn7;
wire updn8;

reg [9:0]x_offset;
reg [9:0]y_offset;
reg [9:0]abs_x;
reg [9:0]abs_y;
reg [9:0]bound_x;
reg [6:0]hole [0:14];
reg [6:0]moleLeftBound [0:119];
reg [6:0]moleRightBound [0:119];

reg [6:0]bottleLeftBound [0:119];
reg [6:0]bottleRightBound [0:119];

reg [6:0]evilLeftBound [0:119];
reg [6:0]evilRightBound [0:119];

reg [6:0]moleHeight[0:8];
reg [33:0]counter00;
reg [33:0]counter11;
reg [33:0]counter22;
reg [33:0]counter33;
reg [33:0]counter44;
reg [33:0]counter55;
reg [33:0]counter66;
reg [33:0]counter77;
reg [33:0]counter88;

reg [33:0]counter2;
reg [17:0] mole_address;//32000+1
reg [1:0] moleExist ;

//=============================================================================
// Structural coding
//=============================================================================



//generate the bound of the holes
always@(posedge iCLK    or negedge iRST_n)
      begin
            if (!iRST_n)
                  begin
                      hole[0] <= 0;
```

```
                    hole[1] <= 0;
                    hole[2] <= 0;
                    hole[3] <= 0;
                    hole[4] <= 0;
                    hole[5] <= 0;
                    hole[6] <= 0;
                    hole[7] <= 0;
                    hole[8] <= 0;
                    hole[9] <= 0;
                    hole[10] <= 0;
                    hole[11] <= 0;
                    hole[12] <= 0;
                    hole[13] <= 0;
                    hole[14] <= 0;
                end
        else
            begin
                hole[0] <= 80;
                    hole[1] <= 80;
                    hole[2] <= 80;
                    hole[3] <= 75;
                    hole[4] <= 75;
                    hole[5] <= 75;
                    hole[6] <= 75;
                    hole[7] <= 75;
                    hole[8] <= 75;
                    hole[9] <= 75;
                    hole[10] <= 70;
                    hole[11] <= 70;
                    hole[12] <= 70;
                    hole[13] <= 65;
                    hole[14] <= 65;
            end
    end



//generate the boundmoleHeight of the mole
always@(posedge iCLK or negedge iRST_n)
    begin
        if (!iRST_n)
                begin
                    moleLeftBound[      0     ] <=        0     ;
                      moleLeftBound[    1     ] <=        0     ;
                      moleLeftBound[    2     ] <=        0     ;
                      moleLeftBound[    3     ] <=        0     ;
                      moleLeftBound[    4     ] <=        0     ;
                      moleLeftBound[    5     ] <=        0     ;
                      moleLeftBound[    6     ] <=        0     ;
                      moleLeftBound[    7     ] <=        0     ;
                      moleLeftBound[    8     ] <=        0     ;
                      moleLeftBound[    9     ] <=        0     ;
                      moleLeftBound[    10    ] <=        0     ;
                      moleLeftBound[    11    ] <=        0     ;
                      moleLeftBound[    12    ] <=        0     ;
                      moleLeftBound[    13    ] <=        0     ;
                      moleLeftBound[    14    ] <=        0     ;
                      moleLeftBound[    15    ] <=        0     ;
```

```
moleLeftBound[  16  ] <=  0  ;
moleLeftBound[  17  ] <=  0  ;
moleLeftBound[  18  ] <=  0  ;
moleLeftBound[  19  ] <=  0  ;
moleLeftBound[  20  ] <=  0  ;
moleLeftBound[  21  ] <=  0  ;
moleLeftBound[  22  ] <=  0  ;
moleLeftBound[  23  ] <=  0  ;
moleLeftBound[  24  ] <=  0  ;
moleLeftBound[  25  ] <=  0  ;
moleLeftBound[  26  ] <=  0  ;
moleLeftBound[  27  ] <=  0  ;
moleLeftBound[  28  ] <=  0  ;
moleLeftBound[  29  ] <=  0  ;
moleLeftBound[  30  ] <=  0  ;
moleLeftBound[  31  ] <=  0  ;
moleLeftBound[  32  ] <=  0  ;
moleLeftBound[  33  ] <=  0  ;
moleLeftBound[  34  ] <=  0  ;
moleLeftBound[  35  ] <=  0  ;
moleLeftBound[  36  ] <=  0  ;
moleLeftBound[  37  ] <=  0  ;
moleLeftBound[  38  ] <=  0  ;
moleLeftBound[  39  ] <=  0  ;
moleLeftBound[  40  ] <=  0  ;
moleLeftBound[  41  ] <=  0  ;
moleLeftBound[  42  ] <=  0  ;
moleLeftBound[  43  ] <=  0  ;
moleLeftBound[  44  ] <=  0  ;
moleLeftBound[  45  ] <=  0  ;
moleLeftBound[  46  ] <=  0  ;
moleLeftBound[  47  ] <=  0  ;
moleLeftBound[  48  ] <=  0  ;
moleLeftBound[  49  ] <=  0  ;
moleLeftBound[  50  ] <=  0  ;
moleLeftBound[  51  ] <=  0  ;
moleLeftBound[  52  ] <=  0  ;
moleLeftBound[  53  ] <=  0  ;
moleLeftBound[  54  ] <=  0  ;
moleLeftBound[  55  ] <=  0  ;
moleLeftBound[  56  ] <=  0  ;
moleLeftBound[  57  ] <=  0  ;
moleLeftBound[  58  ] <=  0  ;
moleLeftBound[  59  ] <=  0  ;
moleLeftBound[  60  ] <=  0  ;
moleLeftBound[  61  ] <=  0  ;
moleLeftBound[  62  ] <=  0  ;
moleLeftBound[  63  ] <=  0  ;
moleLeftBound[  64  ] <=  0  ;
moleLeftBound[  65  ] <=  0  ;
moleLeftBound[  66  ] <=  0  ;
moleLeftBound[  67  ] <=  0  ;
moleLeftBound[  68  ] <=  0  ;
moleLeftBound[  69  ] <=  0  ;
moleLeftBound[  70  ] <=  0  ;
moleLeftBound[  71  ] <=  0  ;
moleLeftBound[  72  ] <=  0  ;
moleLeftBound[  73  ] <=  0  ;
```

```
moleLeftBound[   74  ] <=      0   ;
moleLeftBound[   75  ] <=      0   ;
moleLeftBound[   76  ] <=      0   ;
moleLeftBound[   77  ] <=      0   ;
moleLeftBound[   78  ] <=      0   ;
moleLeftBound[   79  ] <=      0   ;
moleLeftBound[   80  ] <=      0   ;
moleLeftBound[   81  ] <=      0   ;
moleLeftBound[   82  ] <=      0   ;
moleLeftBound[   83  ] <=      0   ;
moleLeftBound[   84  ] <=      0   ;
moleLeftBound[   85  ] <=      0   ;
moleLeftBound[   86  ] <=      0   ;
moleLeftBound[   87  ] <=      0   ;
moleLeftBound[   88  ] <=      0   ;
moleLeftBound[   89  ] <=      0   ;
moleLeftBound[   90  ] <=      0   ;
moleLeftBound[   91  ] <=      0   ;
moleLeftBound[   92  ] <=      0   ;
moleLeftBound[   93  ] <=      0   ;
moleLeftBound[   94  ] <=      0   ;
moleLeftBound[   95  ] <=      0   ;
moleLeftBound[   96  ] <=      0   ;
moleLeftBound[   97  ] <=      0   ;
moleLeftBound[   98  ] <=      0   ;
moleLeftBound[   99  ] <=      0   ;
moleLeftBound[   100 ] <=      0   ;
moleLeftBound[   101 ] <=      0   ;
moleLeftBound[   102 ] <=      0   ;
moleLeftBound[   103 ] <=      0   ;
moleLeftBound[   104 ] <=      0   ;
moleLeftBound[   105 ] <=      0   ;
moleLeftBound[   106 ] <=      0   ;
moleLeftBound[   107 ] <=      0   ;
moleLeftBound[   108 ] <=      0   ;
moleLeftBound[   109 ] <=      0   ;
moleLeftBound[   110 ] <=      0   ;
moleLeftBound[   111 ] <=      0   ;
moleLeftBound[   112 ] <=      0   ;
moleLeftBound[   113 ] <=      0   ;
moleLeftBound[   114 ] <=      0   ;
moleLeftBound[   115 ] <=      0   ;
moleLeftBound[   116 ] <=      0   ;
moleLeftBound[   117 ] <=      0   ;
moleLeftBound[   118 ] <=      0   ;
moleLeftBound[   119 ] <=      0   ;

moleRightBound[  0   ] <=      0   ;
moleRightBound[  1   ] <=      0   ;
moleRightBound[  2   ] <=      0   ;
moleRightBound[  3   ] <=      0   ;
moleRightBound[  4   ] <=      0   ;
moleRightBound[  5   ] <=      0   ;
moleRightBound[  6   ] <=      0   ;
moleRightBound[  7   ] <=      0   ;
moleRightBound[  8   ] <=      0   ;
moleRightBound[  9   ] <=      0   ;
moleRightBound[  10  ] <=      0   ;
```

```
moleRightBound[  11  ] <=      0    ;
moleRightBound[  12  ] <=      0    ;
moleRightBound[  13  ] <=      0    ;
moleRightBound[  14  ] <=      0    ;
moleRightBound[  15  ] <=      0    ;
moleRightBound[  16  ] <=      0    ;
moleRightBound[  17  ] <=      0    ;
moleRightBound[  18  ] <=      0    ;
moleRightBound[  19  ] <=      0    ;
moleRightBound[  20  ] <=      0    ;
moleRightBound[  21  ] <=      0    ;
moleRightBound[  22  ] <=      0    ;
moleRightBound[  23  ] <=      0    ;
moleRightBound[  24  ] <=      0    ;
moleRightBound[  25  ] <=      0    ;
moleRightBound[  26  ] <=      0    ;
moleRightBound[  27  ] <=      0    ;
moleRightBound[  28  ] <=      0    ;
moleRightBound[  29  ] <=      0    ;
moleRightBound[  30  ] <=      0    ;
moleRightBound[  31  ] <=      0    ;
moleRightBound[  32  ] <=      0    ;
moleRightBound[  33  ] <=      0    ;
moleRightBound[  34  ] <=      0    ;
moleRightBound[  35  ] <=      0    ;
moleRightBound[  36  ] <=      0    ;
moleRightBound[  37  ] <=      0    ;
moleRightBound[  38  ] <=      0    ;
moleRightBound[  39  ] <=      0    ;
moleRightBound[  40  ] <=      0    ;
moleRightBound[  41  ] <=      0    ;
moleRightBound[  42  ] <=      0    ;
moleRightBound[  43  ] <=      0    ;
moleRightBound[  44  ] <=      0    ;
moleRightBound[  45  ] <=      0    ;
moleRightBound[  46  ] <=      0    ;
moleRightBound[  47  ] <=      0    ;
moleRightBound[  48  ] <=      0    ;
moleRightBound[  49  ] <=      0    ;
moleRightBound[  50  ] <=      0    ;
moleRightBound[  51  ] <=      0    ;
moleRightBound[  52  ] <=      0    ;
moleRightBound[  53  ] <=      0    ;
moleRightBound[  54  ] <=      0    ;
moleRightBound[  55  ] <=      0    ;
moleRightBound[  56  ] <=      0    ;
moleRightBound[  57  ] <=      0    ;
moleRightBound[  58  ] <=      0    ;
moleRightBound[  59  ] <=      0    ;
moleRightBound[  60  ] <=      0    ;
moleRightBound[  61  ] <=      0    ;
moleRightBound[  62  ] <=      0    ;
moleRightBound[  63  ] <=      0    ;
moleRightBound[  64  ] <=      0    ;
moleRightBound[  65  ] <=      0    ;
moleRightBound[  66  ] <=      0    ;
moleRightBound[  67  ] <=      0    ;
moleRightBound[  68  ] <=      0    ;
```

```
                moleRightBound[  69  ] <=      0   ;
                moleRightBound[  70  ] <=      0   ;
                moleRightBound[  71  ] <=      0   ;
                moleRightBound[  72  ] <=      0   ;
                moleRightBound[  73  ] <=      0   ;
                moleRightBound[  74  ] <=      0   ;
                moleRightBound[  75  ] <=      0   ;
                moleRightBound[  76  ] <=      0   ;
                moleRightBound[  77  ] <=      0   ;
                moleRightBound[  78  ] <=      0   ;
                moleRightBound[  79  ] <=      0   ;
                moleRightBound[  80  ] <=      0   ;
                moleRightBound[  81  ] <=      0   ;
                moleRightBound[  82  ] <=      0   ;
                moleRightBound[  83  ] <=      0   ;
                moleRightBound[  84  ] <=      0   ;
                moleRightBound[  85  ] <=      0   ;
                moleRightBound[  86  ] <=      0   ;
                moleRightBound[  87  ] <=      0   ;
                moleRightBound[  88  ] <=      0   ;
                moleRightBound[  89  ] <=      0   ;
                moleRightBound[  90  ] <=      0   ;
                moleRightBound[  91  ] <=      0   ;
                moleRightBound[  92  ] <=      0   ;
                moleRightBound[  93  ] <=      0   ;
                moleRightBound[  94  ] <=      0   ;
                moleRightBound[  95  ] <=      0   ;
                moleRightBound[  96  ] <=      0   ;
                moleRightBound[  97  ] <=      0   ;
                moleRightBound[  98  ] <=      0   ;
                moleRightBound[  99  ] <=      0   ;
                moleRightBound[  100 ] <=      0   ;
                moleRightBound[  101 ] <=      0   ;
                moleRightBound[  102 ] <=      0   ;
                moleRightBound[  103 ] <=      0   ;
                moleRightBound[  104 ] <=      0   ;
                moleRightBound[  105 ] <=      0   ;
                moleRightBound[  106 ] <=      0   ;
                moleRightBound[  107 ] <=      0   ;
                moleRightBound[  108 ] <=      0   ;
                moleRightBound[  109 ] <=      0   ;
                moleRightBound[  110 ] <=      0   ;
                moleRightBound[  111 ] <=      0   ;
                moleRightBound[  112 ] <=      0   ;
                moleRightBound[  113 ] <=      0   ;
                moleRightBound[  114 ] <=      0   ;
                moleRightBound[  115 ] <=      0   ;
                moleRightBound[  116 ] <=      0   ;
                moleRightBound[  117 ] <=      0   ;
                moleRightBound[  118 ] <=      0   ;
                moleRightBound[  119 ] <=      0   ;

            end
    else
        begin
             moleLeftBound[   0    ] <=      119 ;
                moleLeftBound[    1    ] <=      119 ;
                moleLeftBound[    2    ] <=      54  ;
```

```
moleLeftBound[  3  ] <=  50  ;
moleLeftBound[  4  ] <=  47  ;
moleLeftBound[  5  ] <=  45  ;
moleLeftBound[  6  ] <=  43  ;
moleLeftBound[  7  ] <=  41  ;
moleLeftBound[  8  ] <=  40  ;
moleLeftBound[  9  ] <=  38  ;
moleLeftBound[  10 ] <=  37  ;
moleLeftBound[  11 ] <=  36  ;
moleLeftBound[  12 ] <=  35  ;
moleLeftBound[  13 ] <=  34  ;
moleLeftBound[  14 ] <=  33  ;
moleLeftBound[  15 ] <=  32  ;
moleLeftBound[  16 ] <=  32  ;
moleLeftBound[  17 ] <=  31  ;
moleLeftBound[  18 ] <=  30  ;
moleLeftBound[  19 ] <=  30  ;
moleLeftBound[  20 ] <=  29  ;
moleLeftBound[  21 ] <=  28  ;
moleLeftBound[  22 ] <=  28  ;
moleLeftBound[  23 ] <=  28  ;
moleLeftBound[  24 ] <=  27  ;
moleLeftBound[  25 ] <=  27  ;
moleLeftBound[  26 ] <=  26  ;
moleLeftBound[  27 ] <=  26  ;
moleLeftBound[  28 ] <=  26  ;
moleLeftBound[  29 ] <=  25  ;
moleLeftBound[  30 ] <=  25  ;
moleLeftBound[  31 ] <=  25  ;
moleLeftBound[  32 ] <=  25  ;
moleLeftBound[  33 ] <=  24  ;
moleLeftBound[  34 ] <=  23  ;
moleLeftBound[  35 ] <=  22  ;
moleLeftBound[  36 ] <=  21  ;
moleLeftBound[  37 ] <=  21  ;
moleLeftBound[  38 ] <=  20  ;
moleLeftBound[  39 ] <=  20  ;
moleLeftBound[  40 ] <=  18  ;
moleLeftBound[  41 ] <=  16  ;
moleLeftBound[  42 ] <=  14  ;
moleLeftBound[  43 ] <=  13  ;
moleLeftBound[  44 ] <=  12  ;
moleLeftBound[  45 ] <=  11  ;
moleLeftBound[  46 ] <=  10  ;
moleLeftBound[  47 ] <=  10  ;
moleLeftBound[  48 ] <=  10  ;
moleLeftBound[  49 ] <=  10  ;
moleLeftBound[  50 ] <=  9   ;
moleLeftBound[  51 ] <=  9   ;
moleLeftBound[  52 ] <=  10  ;
moleLeftBound[  53 ] <=  10  ;
moleLeftBound[  54 ] <=  10  ;
moleLeftBound[  55 ] <=  11  ;
moleLeftBound[  56 ] <=  11  ;
moleLeftBound[  57 ] <=  13  ;
moleLeftBound[  58 ] <=  15  ;
moleLeftBound[  59 ] <=  18  ;
moleLeftBound[  60 ] <=  18  ;
```

```
moleLeftBound[  61 ] <=  18 ;
moleLeftBound[  62 ] <=  18 ;
moleLeftBound[  63 ] <=  17 ;
moleLeftBound[  64 ] <=  17 ;
moleLeftBound[  65 ] <=  17 ;
moleLeftBound[  66 ] <=  17 ;
moleLeftBound[  67 ] <=  17 ;
moleLeftBound[  68 ] <=  17 ;
moleLeftBound[  69 ] <=  16 ;
moleLeftBound[  70 ] <=  16 ;
moleLeftBound[  71 ] <=  16 ;
moleLeftBound[  72 ] <=  16 ;
moleLeftBound[  73 ] <=  16 ;
moleLeftBound[  74 ] <=  16 ;
moleLeftBound[  75 ] <=  16 ;
moleLeftBound[  76 ] <=  15 ;
moleLeftBound[  77 ] <=  15 ;
moleLeftBound[  78 ] <=  15 ;
moleLeftBound[  79 ] <=  15 ;
moleLeftBound[  80 ] <=  15 ;
moleLeftBound[  81 ] <=  15 ;
moleLeftBound[  82 ] <=  15 ;
moleLeftBound[  83 ] <=  15 ;
moleLeftBound[  84 ] <=  15 ;
moleLeftBound[  85 ] <=  14 ;
moleLeftBound[  86 ] <=  14 ;
moleLeftBound[  87 ] <=  14 ;
moleLeftBound[  88 ] <=  14 ;
moleLeftBound[  89 ] <=  14 ;
moleLeftBound[  90 ] <=  14 ;
moleLeftBound[  91 ] <=  14 ;
moleLeftBound[  92 ] <=  14 ;
moleLeftBound[  93 ] <=  14 ;
moleLeftBound[  94 ] <=  14 ;
moleLeftBound[  95 ] <=  14 ;
moleLeftBound[  96 ] <=  14 ;
moleLeftBound[  97 ] <=  14 ;
moleLeftBound[  98 ] <=  14 ;
moleLeftBound[  99 ] <=  14 ;
moleLeftBound[ 100 ] <=  14 ;
moleLeftBound[ 101 ] <=  14 ;
moleLeftBound[ 102 ] <=  14 ;
moleLeftBound[ 103 ] <=  14 ;
moleLeftBound[ 104 ] <=  14 ;
moleLeftBound[ 105 ] <=  14 ;
moleLeftBound[ 106 ] <=  14 ;
moleLeftBound[ 107 ] <=  14 ;
moleLeftBound[ 108 ] <=  14 ;
moleLeftBound[ 109 ] <=  14 ;
moleLeftBound[ 110 ] <=  14 ;
moleLeftBound[ 111 ] <=  14 ;
moleLeftBound[ 112 ] <=  14 ;
moleLeftBound[ 113 ] <=  14 ;
moleLeftBound[ 114 ] <=  14 ;
moleLeftBound[ 115 ] <=  14 ;
moleLeftBound[ 116 ] <=  14 ;
moleLeftBound[ 117 ] <=  15 ;
moleLeftBound[ 118 ] <=  15 ;
```

```
moleLeftBound[   119 ] <=      10  ;

moleRightBound[  0   ] <=      119 ;
moleRightBound[  1   ] <=      119 ;
moleRightBound[  2   ] <=      67  ;
moleRightBound[  3   ] <=      71  ;
moleRightBound[  4   ] <=      74  ;
moleRightBound[  5   ] <=      76  ;
moleRightBound[  6   ] <=      78  ;
moleRightBound[  7   ] <=      80  ;
moleRightBound[  8   ] <=      81  ;
moleRightBound[  9   ] <=      82  ;
moleRightBound[  10  ] <=      83  ;
moleRightBound[  11  ] <=      85  ;
moleRightBound[  12  ] <=      86  ;
moleRightBound[  13  ] <=      87  ;
moleRightBound[  14  ] <=      88  ;
moleRightBound[  15  ] <=      89  ;
moleRightBound[  16  ] <=      90  ;
moleRightBound[  17  ] <=      90  ;
moleRightBound[  18  ] <=      91  ;
moleRightBound[  19  ] <=      92  ;
moleRightBound[  20  ] <=      92  ;
moleRightBound[  21  ] <=      93  ;
moleRightBound[  22  ] <=      93  ;
moleRightBound[  23  ] <=      94  ;
moleRightBound[  24  ] <=      94  ;
moleRightBound[  25  ] <=      95  ;
moleRightBound[  26  ] <=      95  ;
moleRightBound[  27  ] <=      95  ;
moleRightBound[  28  ] <=      96  ;
moleRightBound[  29  ] <=      96  ;
moleRightBound[  30  ] <=      96  ;
moleRightBound[  31  ] <=      96  ;
moleRightBound[  32  ] <=      96  ;
moleRightBound[  33  ] <=      97  ;
moleRightBound[  34  ] <=      98  ;
moleRightBound[  35  ] <=      99  ;
moleRightBound[  36  ] <=      100 ;
moleRightBound[  37  ] <=      101 ;
moleRightBound[  38  ] <=      101 ;
moleRightBound[  39  ] <=      101 ;
moleRightBound[  40  ] <=      103 ;
moleRightBound[  41  ] <=      105 ;
moleRightBound[  42  ] <=      107 ;
moleRightBound[  43  ] <=      108 ;
moleRightBound[  44  ] <=      109 ;
moleRightBound[  45  ] <=      110 ;
moleRightBound[  46  ] <=      111 ;
moleRightBound[  47  ] <=      111 ;
moleRightBound[  48  ] <=      111 ;
moleRightBound[  49  ] <=      111 ;
moleRightBound[  50  ] <=      112 ;
moleRightBound[  51  ] <=      112 ;
moleRightBound[  52  ] <=      111 ;
moleRightBound[  53  ] <=      111 ;
moleRightBound[  54  ] <=      111 ;
moleRightBound[  55  ] <=      110 ;
```

```
moleRightBound[  56  ] <=      110 ;
moleRightBound[  57  ] <=      108 ;
moleRightBound[  58  ] <=      106 ;
moleRightBound[  59  ] <=      104 ;
moleRightBound[  60  ] <=      104 ;
moleRightBound[  61  ] <=      104 ;
moleRightBound[  62  ] <=      104 ;
moleRightBound[  63  ] <=      105 ;
moleRightBound[  64  ] <=      105 ;
moleRightBound[  65  ] <=      105 ;
moleRightBound[  66  ] <=      105 ;
moleRightBound[  67  ] <=      105 ;
moleRightBound[  68  ] <=      105 ;
moleRightBound[  69  ] <=      106 ;
moleRightBound[  70  ] <=      106 ;
moleRightBound[  71  ] <=      106 ;
moleRightBound[  72  ] <=      106 ;
moleRightBound[  73  ] <=      106 ;
moleRightBound[  74  ] <=      106 ;
moleRightBound[  75  ] <=      106 ;
moleRightBound[  76  ] <=      107 ;
moleRightBound[  77  ] <=      107 ;
moleRightBound[  78  ] <=      107 ;
moleRightBound[  79  ] <=      107 ;
moleRightBound[  80  ] <=      107 ;
moleRightBound[  81  ] <=      107 ;
moleRightBound[  82  ] <=      107 ;
moleRightBound[  83  ] <=      107 ;
moleRightBound[  84  ] <=      108 ;
moleRightBound[  85  ] <=      108 ;
moleRightBound[  86  ] <=      108 ;
moleRightBound[  87  ] <=      108 ;
moleRightBound[  88  ] <=      108 ;
moleRightBound[  89  ] <=      108 ;
moleRightBound[  90  ] <=      108 ;
moleRightBound[  91  ] <=      108 ;
moleRightBound[  92  ] <=      108 ;
moleRightBound[  93  ] <=      108 ;
moleRightBound[  94  ] <=      108 ;
moleRightBound[  95  ] <=      108 ;
moleRightBound[  96  ] <=      108 ;
moleRightBound[  97  ] <=      108 ;
moleRightBound[  98  ] <=      108 ;
moleRightBound[  99  ] <=      108 ;
moleRightBound[  100 ] <=      108 ;
moleRightBound[  101 ] <=      108 ;
moleRightBound[  102 ] <=      108 ;
moleRightBound[  103 ] <=      108 ;
moleRightBound[  104 ] <=      108 ;
moleRightBound[  105 ] <=      108 ;
moleRightBound[  106 ] <=      108 ;
moleRightBound[  107 ] <=      108 ;
moleRightBound[  108 ] <=      108 ;
moleRightBound[  109 ] <=      108 ;
moleRightBound[  110 ] <=      108 ;
moleRightBound[  111 ] <=      108 ;
moleRightBound[  112 ] <=      108 ;
moleRightBound[  113 ] <=      108 ;
```

```
                moleRightBound[  114 ] <=      108 ;
                moleRightBound[  115 ] <=      108 ;
                moleRightBound[  116 ] <=      108 ;
                moleRightBound[  117 ] <=      108 ;
                moleRightBound[  118 ] <=      108 ;
                moleRightBound[  119 ] <=      108 ;
        end
    end


//generate the boundbottleHeight of the bottle
always@(posedge iCLK or negedge iRST_n)
    begin
        if (!iRST_n)
            begin
                bottleLeftBound[    0    ] <=      0    ;
                bottleLeftBound[    1    ] <=      0    ;
                bottleLeftBound[    2    ] <=      0    ;
                bottleLeftBound[    3    ] <=      0    ;
                bottleLeftBound[    4    ] <=      0    ;
                bottleLeftBound[    5    ] <=      0    ;
                bottleLeftBound[    6    ] <=      0    ;
                bottleLeftBound[    7    ] <=      0    ;
                bottleLeftBound[    8    ] <=      0    ;
                bottleLeftBound[    9    ] <=      0    ;
                bottleLeftBound[    10   ] <=      0    ;
                bottleLeftBound[    11   ] <=      0    ;
                bottleLeftBound[    12   ] <=      0    ;
                bottleLeftBound[    13   ] <=      0    ;
                bottleLeftBound[    14   ] <=      0    ;
                bottleLeftBound[    15   ] <=      0    ;
                bottleLeftBound[    16   ] <=      0    ;
                bottleLeftBound[    17   ] <=      0    ;
                bottleLeftBound[    18   ] <=      0    ;
                bottleLeftBound[    19   ] <=      0    ;
                bottleLeftBound[    20   ] <=      0    ;
                bottleLeftBound[    21   ] <=      0    ;
                bottleLeftBound[    22   ] <=      0    ;
                bottleLeftBound[    23   ] <=      0    ;
                bottleLeftBound[    24   ] <=      0    ;
                bottleLeftBound[    25   ] <=      0    ;
                bottleLeftBound[    26   ] <=      0    ;
                bottleLeftBound[    27   ] <=      0    ;
                bottleLeftBound[    28   ] <=      0    ;
                bottleLeftBound[    29   ] <=      0    ;
                bottleLeftBound[    30   ] <=      0    ;
                bottleLeftBound[    31   ] <=      0    ;
                bottleLeftBound[    32   ] <=      0    ;
                bottleLeftBound[    33   ] <=      0    ;
                bottleLeftBound[    34   ] <=      0    ;
                bottleLeftBound[    35   ] <=      0    ;
                bottleLeftBound[    36   ] <=      0    ;
                bottleLeftBound[    37   ] <=      0    ;
                bottleLeftBound[    38   ] <=      0    ;
                bottleLeftBound[    39   ] <=      0    ;
                bottleLeftBound[    40   ] <=      0    ;
                bottleLeftBound[    41   ] <=      0    ;
                bottleLeftBound[    42   ] <=      0    ;
```

```
bottleLeftBound[  43  ] <=      0   ;
bottleLeftBound[  44  ] <=      0   ;
bottleLeftBound[  45  ] <=      0   ;
bottleLeftBound[  46  ] <=      0   ;
bottleLeftBound[  47  ] <=      0   ;
bottleLeftBound[  48  ] <=      0   ;
bottleLeftBound[  49  ] <=      0   ;
bottleLeftBound[  50  ] <=      0   ;
bottleLeftBound[  51  ] <=      0   ;
bottleLeftBound[  52  ] <=      0   ;
bottleLeftBound[  53  ] <=      0   ;
bottleLeftBound[  54  ] <=      0   ;
bottleLeftBound[  55  ] <=      0   ;
bottleLeftBound[  56  ] <=      0   ;
bottleLeftBound[  57  ] <=      0   ;
bottleLeftBound[  58  ] <=      0   ;
bottleLeftBound[  59  ] <=      0   ;
bottleLeftBound[  60  ] <=      0   ;
bottleLeftBound[  61  ] <=      0   ;
bottleLeftBound[  62  ] <=      0   ;
bottleLeftBound[  63  ] <=      0   ;
bottleLeftBound[  64  ] <=      0   ;
bottleLeftBound[  65  ] <=      0   ;
bottleLeftBound[  66  ] <=      0   ;
bottleLeftBound[  67  ] <=      0   ;
bottleLeftBound[  68  ] <=      0   ;
bottleLeftBound[  69  ] <=      0   ;
bottleLeftBound[  70  ] <=      0   ;
bottleLeftBound[  71  ] <=      0   ;
bottleLeftBound[  72  ] <=      0   ;
bottleLeftBound[  73  ] <=      0   ;
bottleLeftBound[  74  ] <=      0   ;
bottleLeftBound[  75  ] <=      0   ;
bottleLeftBound[  76  ] <=      0   ;
bottleLeftBound[  77  ] <=      0   ;
bottleLeftBound[  78  ] <=      0   ;
bottleLeftBound[  79  ] <=      0   ;
bottleLeftBound[  80  ] <=      0   ;
bottleLeftBound[  81  ] <=      0   ;
bottleLeftBound[  82  ] <=      0   ;
bottleLeftBound[  83  ] <=      0   ;
bottleLeftBound[  84  ] <=      0   ;
bottleLeftBound[  85  ] <=      0   ;
bottleLeftBound[  86  ] <=      0   ;
bottleLeftBound[  87  ] <=      0   ;
bottleLeftBound[  88  ] <=      0   ;
bottleLeftBound[  89  ] <=      0   ;
bottleLeftBound[  90  ] <=      0   ;
bottleLeftBound[  91  ] <=      0   ;
bottleLeftBound[  92  ] <=      0   ;
bottleLeftBound[  93  ] <=      0   ;
bottleLeftBound[  94  ] <=      0   ;
bottleLeftBound[  95  ] <=      0   ;
bottleLeftBound[  96  ] <=      0   ;
bottleLeftBound[  97  ] <=      0   ;
bottleLeftBound[  98  ] <=      0   ;
bottleLeftBound[  99  ] <=      0   ;
bottleLeftBound[  100 ] <=      0   ;
```

```
bottleLeftBound[   101  ] <=       0    ;
bottleLeftBound[   102  ] <=       0    ;
bottleLeftBound[   103  ] <=       0    ;
bottleLeftBound[   104  ] <=       0    ;
bottleLeftBound[   105  ] <=       0    ;
bottleLeftBound[   106  ] <=       0    ;
bottleLeftBound[   107  ] <=       0    ;
bottleLeftBound[   108  ] <=       0    ;
bottleLeftBound[   109  ] <=       0    ;
bottleLeftBound[   110  ] <=       0    ;
bottleLeftBound[   111  ] <=       0    ;
bottleLeftBound[   112  ] <=       0    ;
bottleLeftBound[   113  ] <=       0    ;
bottleLeftBound[   114  ] <=       0    ;
bottleLeftBound[   115  ] <=       0    ;
bottleLeftBound[   116  ] <=       0    ;
bottleLeftBound[   117  ] <=       0    ;
bottleLeftBound[   118  ] <=       0    ;
bottleLeftBound[   119  ] <=       0    ;

bottleRightBound[  0    ] <=       0    ;
bottleRightBound[  1    ] <=       0    ;
bottleRightBound[  2    ] <=       0    ;
bottleRightBound[  3    ] <=       0    ;
bottleRightBound[  4    ] <=       0    ;
bottleRightBound[  5    ] <=       0    ;
bottleRightBound[  6    ] <=       0    ;
bottleRightBound[  7    ] <=       0    ;
bottleRightBound[  8    ] <=       0    ;
bottleRightBound[  9    ] <=       0    ;
bottleRightBound[  10   ] <=       0    ;
bottleRightBound[  11   ] <=       0    ;
bottleRightBound[  12   ] <=       0    ;
bottleRightBound[  13   ] <=       0    ;
bottleRightBound[  14   ] <=       0    ;
bottleRightBound[  15   ] <=       0    ;
bottleRightBound[  16   ] <=       0    ;
bottleRightBound[  17   ] <=       0    ;
bottleRightBound[  18   ] <=       0    ;
bottleRightBound[  19   ] <=       0    ;
bottleRightBound[  20   ] <=       0    ;
bottleRightBound[  21   ] <=       0    ;
bottleRightBound[  22   ] <=       0    ;
bottleRightBound[  23   ] <=       0    ;
bottleRightBound[  24   ] <=       0    ;
bottleRightBound[  25   ] <=       0    ;
bottleRightBound[  26   ] <=       0    ;
bottleRightBound[  27   ] <=       0    ;
bottleRightBound[  28   ] <=       0    ;
bottleRightBound[  29   ] <=       0    ;
bottleRightBound[  30   ] <=       0    ;
bottleRightBound[  31   ] <=       0    ;
bottleRightBound[  32   ] <=       0    ;
bottleRightBound[  33   ] <=       0    ;
bottleRightBound[  34   ] <=       0    ;
bottleRightBound[  35   ] <=       0    ;
bottleRightBound[  36   ] <=       0    ;
bottleRightBound[  37   ] <=       0    ;
```

```
bottleRightBound[ 38 ] <= 0 ;
bottleRightBound[ 39 ] <= 0 ;
bottleRightBound[ 40 ] <= 0 ;
bottleRightBound[ 41 ] <= 0 ;
bottleRightBound[ 42 ] <= 0 ;
bottleRightBound[ 43 ] <= 0 ;
bottleRightBound[ 44 ] <= 0 ;
bottleRightBound[ 45 ] <= 0 ;
bottleRightBound[ 46 ] <= 0 ;
bottleRightBound[ 47 ] <= 0 ;
bottleRightBound[ 48 ] <= 0 ;
bottleRightBound[ 49 ] <= 0 ;
bottleRightBound[ 50 ] <= 0 ;
bottleRightBound[ 51 ] <= 0 ;
bottleRightBound[ 52 ] <= 0 ;
bottleRightBound[ 53 ] <= 0 ;
bottleRightBound[ 54 ] <= 0 ;
bottleRightBound[ 55 ] <= 0 ;
bottleRightBound[ 56 ] <= 0 ;
bottleRightBound[ 57 ] <= 0 ;
bottleRightBound[ 58 ] <= 0 ;
bottleRightBound[ 59 ] <= 0 ;
bottleRightBound[ 60 ] <= 0 ;
bottleRightBound[ 61 ] <= 0 ;
bottleRightBound[ 62 ] <= 0 ;
bottleRightBound[ 63 ] <= 0 ;
bottleRightBound[ 64 ] <= 0 ;
bottleRightBound[ 65 ] <= 0 ;
bottleRightBound[ 66 ] <= 0 ;
bottleRightBound[ 67 ] <= 0 ;
bottleRightBound[ 68 ] <= 0 ;
bottleRightBound[ 69 ] <= 0 ;
bottleRightBound[ 70 ] <= 0 ;
bottleRightBound[ 71 ] <= 0 ;
bottleRightBound[ 72 ] <= 0 ;
bottleRightBound[ 73 ] <= 0 ;
bottleRightBound[ 74 ] <= 0 ;
bottleRightBound[ 75 ] <= 0 ;
bottleRightBound[ 76 ] <= 0 ;
bottleRightBound[ 77 ] <= 0 ;
bottleRightBound[ 78 ] <= 0 ;
bottleRightBound[ 79 ] <= 0 ;
bottleRightBound[ 80 ] <= 0 ;
bottleRightBound[ 81 ] <= 0 ;
bottleRightBound[ 82 ] <= 0 ;
bottleRightBound[ 83 ] <= 0 ;
bottleRightBound[ 84 ] <= 0 ;
bottleRightBound[ 85 ] <= 0 ;
bottleRightBound[ 86 ] <= 0 ;
bottleRightBound[ 87 ] <= 0 ;
bottleRightBound[ 88 ] <= 0 ;
bottleRightBound[ 89 ] <= 0 ;
bottleRightBound[ 90 ] <= 0 ;
bottleRightBound[ 91 ] <= 0 ;
bottleRightBound[ 92 ] <= 0 ;
bottleRightBound[ 93 ] <= 0 ;
bottleRightBound[ 94 ] <= 0 ;
bottleRightBound[ 95 ] <= 0 ;
```

```
                    bottleRightBound[  96   ] <=      0    ;
                    bottleRightBound[  97   ] <=      0    ;
                    bottleRightBound[  98   ] <=      0    ;
                    bottleRightBound[  99   ] <=      0    ;
                    bottleRightBound[  100  ] <=      0    ;
                    bottleRightBound[  101  ] <=      0    ;
                    bottleRightBound[  102  ] <=      0    ;
                    bottleRightBound[  103  ] <=      0    ;
                    bottleRightBound[  104  ] <=      0    ;
                    bottleRightBound[  105  ] <=      0    ;
                    bottleRightBound[  106  ] <=      0    ;
                    bottleRightBound[  107  ] <=      0    ;
                    bottleRightBound[  108  ] <=      0    ;
                    bottleRightBound[  109  ] <=      0    ;
                    bottleRightBound[  110  ] <=      0    ;
                    bottleRightBound[  111  ] <=      0    ;
                    bottleRightBound[  112  ] <=      0    ;
                    bottleRightBound[  113  ] <=      0    ;
                    bottleRightBound[  114  ] <=      0    ;
                    bottleRightBound[  115  ] <=      0    ;
                    bottleRightBound[  116  ] <=      0    ;
                    bottleRightBound[  117  ] <=      0    ;
                    bottleRightBound[  118  ] <=      0    ;
                    bottleRightBound[  119  ] <=      0    ;

                end
        else
            begin
                                                    bottleLeftBound[       0  ]                <=
    52          ;
                                                                    bottleLeftBound[       1
    ] <=       50   ;
                                                                    bottleLeftBound[       2
    ] <=       46   ;
                                                                    bottleLeftBound[       3
    ] <=       46   ;
                                                                    bottleLeftBound[       4
    ] <=       44   ;
                                                                    bottleLeftBound[       5
    ] <=       43   ;
                                                                    bottleLeftBound[       6
    ] <=       42   ;
                                                                    bottleLeftBound[       7
    ] <=       41   ;
                                                                    bottleLeftBound[       8
    ] <=       41   ;
                                                                    bottleLeftBound[       9
    ] <=       40   ;
                                                                    bottleLeftBound[
10  ] <=       40   ;
                                                                    bottleLeftBound[
11  ] <=       40   ;
                                                                    bottleLeftBound[
12  ] <=       40   ;
                                                                    bottleLeftBound[
13  ] <=       39   ;
                                                                    bottleLeftBound[
14  ] <=       38   ;
```

```
bottleLeftBound[ 15 ] <= 37 ;
bottleLeftBound[ 16 ] <= 36 ;
bottleLeftBound[ 17 ] <= 34 ;
bottleLeftBound[ 18 ] <= 33 ;
bottleLeftBound[ 19 ] <= 33 ;
bottleLeftBound[ 20 ] <= 30 ;
bottleLeftBound[ 21 ] <= 31 ;
bottleLeftBound[ 22 ] <= 30 ;
bottleLeftBound[ 23 ] <= 29 ;
bottleLeftBound[ 24 ] <= 28 ;
bottleLeftBound[ 25 ] <= 28 ;
bottleLeftBound[ 26 ] <= 28 ;
bottleLeftBound[ 27 ] <= 28 ;
bottleLeftBound[ 28 ] <= 28 ;
bottleLeftBound[ 29 ] <= 27 ;
bottleLeftBound[ 30 ] <= 27 ;
bottleLeftBound[ 31 ] <= 25 ;
bottleLeftBound[ 32 ] <= 23 ;
bottleLeftBound[ 33 ] <= 22 ;
bottleLeftBound[ 34 ] <= 21 ;
bottleLeftBound[ 35 ] <= 21 ;
bottleLeftBound[ 36 ] <= 20 ;
bottleLeftBound[ 37 ] <= 20 ;
bottleLeftBound[ 38 ] <= 20 ;
bottleLeftBound[ 39 ] <= 20 ;
bottleLeftBound[ 40 ] <= 20 ;
bottleLeftBound[ 41 ] <= 20 ;
bottleLeftBound[ 42 ] <= 20 ;
bottleLeftBound[ 43 ] <= 20 ;
```

```
                                                                bottleLeftBound[
44  ] <=        18  ;
                                                                bottleLeftBound[
45  ] <=        16  ;
                                                                bottleLeftBound[
46  ] <=        15  ;
                                                                bottleLeftBound[
47  ] <=        14  ;
                                                                bottleLeftBound[
48  ] <=        13  ;
                                                                bottleLeftBound[
49  ] <=        13  ;
                                                                bottleLeftBound[
50  ] <=        13  ;
                                                                bottleLeftBound[
51  ] <=        13  ;
                                                                bottleLeftBound[
52  ] <=        13  ;
                                                                bottleLeftBound[
53  ] <=        13  ;
                                                                bottleLeftBound[
54  ] <=        13  ;
                                                                bottleLeftBound[
55  ] <=        13  ;
                                                                bottleLeftBound[
56  ] <=        13  ;
                                                                bottleLeftBound[
57  ] <=        13  ;
                                                                bottleLeftBound[
58  ] <=        13  ;
                                                                bottleLeftBound[
59  ] <=        13  ;
                                                                bottleLeftBound[
60  ] <=        13  ;
                                                                bottleLeftBound[
61  ] <=        13  ;
                                                                bottleLeftBound[
62  ] <=        13  ;
                                                                bottleLeftBound[
63  ] <=        13  ;
                                                                bottleLeftBound[
64  ] <=        13  ;
                                                                bottleLeftBound[
65  ] <=        13  ;
                                                                bottleLeftBound[
66  ] <=        13  ;
                                                                bottleLeftBound[
67  ] <=        13  ;
                                                                bottleLeftBound[
68  ] <=        13  ;
                                                                bottleLeftBound[
69  ] <=        13  ;
                                                                bottleLeftBound[
70  ] <=        13  ;
                                                                bottleLeftBound[
71  ] <=        13  ;
                                                                bottleLeftBound[
72  ] <=        13  ;
```

```
                                                                bottleLeftBound[
73   ] <=      13   ;
                                                                bottleLeftBound[
74   ] <=      13   ;
                                                                bottleLeftBound[
75   ] <=      13   ;
                                                                bottleLeftBound[
76   ] <=      13   ;
                                                                bottleLeftBound[
77   ] <=      13   ;
                                                                bottleLeftBound[
78   ] <=      13   ;
                                                                bottleLeftBound[
79   ] <=      13   ;
                                                                bottleLeftBound[
80   ] <=      13   ;
                                                                bottleLeftBound[
81   ] <=      13   ;
                                                                bottleLeftBound[
82   ] <=      13   ;
                                                                bottleLeftBound[
83   ] <=      13   ;
                                                                bottleLeftBound[
84   ] <=      13   ;
                                                                bottleLeftBound[
85   ] <=      13   ;
                                                                bottleLeftBound[
86   ] <=      13   ;
                                                                bottleLeftBound[
87   ] <=      13   ;
                                                                bottleLeftBound[
88   ] <=      13   ;
                                                                bottleLeftBound[
89   ] <=      13   ;
                                                                bottleLeftBound[
90   ] <=      13   ;
                                                                bottleLeftBound[
91   ] <=      13   ;
                                                                bottleLeftBound[
92   ] <=      13   ;
                                                                bottleLeftBound[
93   ] <=      13   ;
                                                                bottleLeftBound[
94   ] <=      13   ;
                                                                bottleLeftBound[
95   ] <=      13   ;
                                                                bottleLeftBound[
96   ] <=      13   ;
                                                                bottleLeftBound[
97   ] <=      13   ;
                                                                bottleLeftBound[
98   ] <=      13   ;
                                                                bottleLeftBound[
99   ] <=      13   ;
                                                                bottleLeftBound[
100  ] <=      13   ;
                                                                bottleLeftBound[
101  ] <=      13   ;
```

```
                                                    bottleLeftBound[
102 ] <=      13  ;
                                                    bottleLeftBound[
103 ] <=      13  ;
                                                    bottleLeftBound[
104 ] <=      13  ;
                                                    bottleLeftBound[
105 ] <=      13  ;
                                                    bottleLeftBound[
106 ] <=      13  ;
                                                    bottleLeftBound[
107 ] <=      13  ;
                                                    bottleLeftBound[
108 ] <=      13  ;
                                                    bottleLeftBound[
109 ] <=      13  ;
                                                    bottleLeftBound[
110 ] <=      13  ;
                                                    bottleLeftBound[
111 ] <=      13  ;
                                                    bottleLeftBound[
112 ] <=      13  ;
                                                    bottleLeftBound[
113 ] <=      13  ;
                                                    bottleLeftBound[
114 ] <=      14  ;
                                                    bottleLeftBound[
115 ] <=      14  ;
                                                    bottleLeftBound[
116 ] <=      15  ;
                                                    bottleLeftBound[
117 ] <=      17  ;
                                                    bottleLeftBound[
118 ] <=      18  ;
                                                    bottleLeftBound[
119 ] <=      23  ;

                                                     bottleRightBound[   0
    ] <=      68  ;
                                                     bottleRightBound[   1
    ] <=      72  ;
                                                     bottleRightBound[   2
    ] <=      75  ;
                                                     bottleRightBound[   3
    ] <=      76  ;
                                                     bottleRightBound[   4
    ] <=      77  ;
                                                     bottleRightBound[   5
    ] <=      78  ;
                                                     bottleRightBound[   6
    ] <=      79  ;
                                                     bottleRightBound[   7
    ] <=      80  ;
                                                     bottleRightBound[   8
    ] <=      81  ;
                                                     bottleRightBound[   9
    ] <=      81  ;
                                                     bottleRightBound[
```

```
10  ] <=    82  ;
                                                    bottleRightBound[
11  ] <=    82  ;
                                                    bottleRightBound[
12  ] <=    82  ;
                                                    bottleRightBound[
13  ] <=    83  ;
                                                    bottleRightBound[
14  ] <=    84  ;
                                                    bottleRightBound[
15  ] <=    86  ;
                                                    bottleRightBound[
16  ] <=    87  ;
                                                    bottleRightBound[
17  ] <=    88  ;
                                                    bottleRightBound[
18  ] <=    90  ;
                                                    bottleRightBound[
19  ] <=    90  ;
                                                    bottleRightBound[
20  ] <=    92  ;
                                                    bottleRightBound[
21  ] <=    93  ;
                                                    bottleRightBound[
22  ] <=    93  ;
                                                    bottleRightBound[
23  ] <=    94  ;
                                                    bottleRightBound[
24  ] <=    94  ;
                                                    bottleRightBound[
25  ] <=    94  ;
                                                    bottleRightBound[
26  ] <=    95  ;
                                                    bottleRightBound[
27  ] <=    95  ;
                                                    bottleRightBound[
28  ] <=    95  ;
                                                    bottleRightBound[
29  ] <=    95  ;
                                                    bottleRightBound[
30  ] <=    95  ;
                                                    bottleRightBound[
31  ] <=    98  ;
                                                    bottleRightBound[
32  ] <=    100 ;
                                                    bottleRightBound[
33  ] <=    101 ;
                                                    bottleRightBound[
34  ] <=    102 ;
                                                    bottleRightBound[
35  ] <=    102 ;
                                                    bottleRightBound[
36  ] <=    103 ;
                                                    bottleRightBound[
37  ] <=    103 ;
                                                    bottleRightBound[
38  ] <=    103 ;
                                                    bottleRightBound[
```

```
39  ] <=      103 ;  bottleRightBound[
40  ] <=      103 ;  bottleRightBound[
41  ] <=      103 ;  bottleRightBound[
42  ] <=      103 ;  bottleRightBound[
43  ] <=      102 ;  bottleRightBound[
44  ] <=      103 ;  bottleRightBound[
45  ] <=      106 ;  bottleRightBound[
46  ] <=      106 ;  bottleRightBound[
47  ] <=      105 ;  bottleRightBound[
48  ] <=      107 ;  bottleRightBound[
49  ] <=      107 ;  bottleRightBound[
50  ] <=      107 ;  bottleRightBound[
51  ] <=      107 ;  bottleRightBound[
52  ] <=      107 ;  bottleRightBound[
53  ] <=      107 ;  bottleRightBound[
54  ] <=      107 ;  bottleRightBound[
55  ] <=      107 ;  bottleRightBound[
56  ] <=      107 ;  bottleRightBound[
57  ] <=      107 ;  bottleRightBound[
58  ] <=      107 ;  bottleRightBound[
59  ] <=      107 ;  bottleRightBound[
60  ] <=      107 ;  bottleRightBound[
61  ] <=      107 ;  bottleRightBound[
62  ] <=      107 ;  bottleRightBound[
63  ] <=      107 ;  bottleRightBound[
64  ] <=      107 ;  bottleRightBound[
65  ] <=      107 ;  bottleRightBound[
66  ] <=      107 ;  bottleRightBound[
67  ] <=      107 ;  bottleRightBound[
```

```
68  ] <=    107 ;
                                                    bottleRightBound[
69  ] <=    107 ;
                                                    bottleRightBound[
70  ] <=    107 ;
                                                    bottleRightBound[
71  ] <=    107 ;
                                                    bottleRightBound[
72  ] <=    107 ;
                                                    bottleRightBound[
73  ] <=    107 ;
                                                    bottleRightBound[
74  ] <=    107 ;
                                                    bottleRightBound[
75  ] <=    107 ;
                                                    bottleRightBound[
76  ] <=    107 ;
                                                    bottleRightBound[
77  ] <=    107 ;
                                                    bottleRightBound[
78  ] <=    107 ;
                                                    bottleRightBound[
79  ] <=    107 ;
                                                    bottleRightBound[
80  ] <=    107 ;
                                                    bottleRightBound[
81  ] <=    107 ;
                                                    bottleRightBound[
82  ] <=    107 ;
                                                    bottleRightBound[
83  ] <=    107 ;
                                                    bottleRightBound[
84  ] <=    107 ;
                                                    bottleRightBound[
85  ] <=    107 ;
                                                    bottleRightBound[
86  ] <=    107 ;
                                                    bottleRightBound[
87  ] <=    107 ;
                                                    bottleRightBound[
88  ] <=    107 ;
                                                    bottleRightBound[
89  ] <=    107 ;
                                                    bottleRightBound[
90  ] <=    107 ;
                                                    bottleRightBound[
91  ] <=    107 ;
                                                    bottleRightBound[
92  ] <=    107 ;
                                                    bottleRightBound[
93  ] <=    107 ;
                                                    bottleRightBound[
94  ] <=    107 ;
                                                    bottleRightBound[
95  ] <=    107 ;
                                                    bottleRightBound[
96  ] <=    107 ;
                                                    bottleRightBound[
```

```
97   ] <=       107 ;
                                                                bottleRightBound[
98   ] <=       107 ;
                                                                bottleRightBound[
99   ] <=       107 ;
                                                                bottleRightBound[
100  ] <=       107 ;
                                                                bottleRightBound[
101  ] <=       107 ;
                                                                bottleRightBound[
102  ] <=       107 ;
                                                                bottleRightBound[
103  ] <=       107 ;
                                                                bottleRightBound[
104  ] <=       107 ;
                                                                bottleRightBound[
105  ] <=       107 ;
                                                                bottleRightBound[
106  ] <=       107 ;
                                                                bottleRightBound[
107  ] <=       107 ;
                                                                bottleRightBound[
108  ] <=       107 ;
                                                                bottleRightBound[
109  ] <=       107 ;
                                                                bottleRightBound[
110  ] <=       107 ;
                                                                bottleRightBound[
111  ] <=       107 ;
                                                                bottleRightBound[
112  ] <=       107 ;
                                                                bottleRightBound[
113  ] <=       107 ;
                                                                bottleRightBound[
114  ] <=       106 ;
                                                                bottleRightBound[
115  ] <=       106 ;
                                                                bottleRightBound[
116  ] <=       105 ;
                                                                bottleRightBound[
117  ] <=       104 ;
                                                                bottleRightBound[
118  ] <=       103 ;
                                                                bottleRightBound[
119  ] <=       98   ;
            end
      end


//generate the boundevilHeight of the evil
always@(posedge iCLK or negedge iRST_n)
      begin
            if (!iRST_n)
                  begin
                        evilLeftBound[  0     ] <=       0     ;
                          evilLeftBound[ 1     ] <=       0     ;
                          evilLeftBound[ 2     ] <=       0     ;
                          evilLeftBound[ 3     ] <=       0     ;
```

```
evilLeftBound[4  ] <=  0  ;
evilLeftBound[5  ] <=  0  ;
evilLeftBound[6  ] <=  0  ;
evilLeftBound[7  ] <=  0  ;
evilLeftBound[8  ] <=  0  ;
evilLeftBound[9  ] <=  0  ;
evilLeftBound[10 ] <=  0  ;
evilLeftBound[11 ] <=  0  ;
evilLeftBound[12 ] <=  0  ;
evilLeftBound[13 ] <=  0  ;
evilLeftBound[14 ] <=  0  ;
evilLeftBound[15 ] <=  0  ;
evilLeftBound[16 ] <=  0  ;
evilLeftBound[17 ] <=  0  ;
evilLeftBound[18 ] <=  0  ;
evilLeftBound[19 ] <=  0  ;
evilLeftBound[20 ] <=  0  ;
evilLeftBound[21 ] <=  0  ;
evilLeftBound[22 ] <=  0  ;
evilLeftBound[23 ] <=  0  ;
evilLeftBound[24 ] <=  0  ;
evilLeftBound[25 ] <=  0  ;
evilLeftBound[26 ] <=  0  ;
evilLeftBound[27 ] <=  0  ;
evilLeftBound[28 ] <=  0  ;
evilLeftBound[29 ] <=  0  ;
evilLeftBound[30 ] <=  0  ;
evilLeftBound[31 ] <=  0  ;
evilLeftBound[32 ] <=  0  ;
evilLeftBound[33 ] <=  0  ;
evilLeftBound[34 ] <=  0  ;
evilLeftBound[35 ] <=  0  ;
evilLeftBound[36 ] <=  0  ;
evilLeftBound[37 ] <=  0  ;
evilLeftBound[38 ] <=  0  ;
evilLeftBound[39 ] <=  0  ;
evilLeftBound[40 ] <=  0  ;
evilLeftBound[41 ] <=  0  ;
evilLeftBound[42 ] <=  0  ;
evilLeftBound[43 ] <=  0  ;
evilLeftBound[44 ] <=  0  ;
evilLeftBound[45 ] <=  0  ;
evilLeftBound[46 ] <=  0  ;
evilLeftBound[47 ] <=  0  ;
evilLeftBound[48 ] <=  0  ;
evilLeftBound[49 ] <=  0  ;
evilLeftBound[50 ] <=  0  ;
evilLeftBound[51 ] <=  0  ;
evilLeftBound[52 ] <=  0  ;
evilLeftBound[53 ] <=  0  ;
evilLeftBound[54 ] <=  0  ;
evilLeftBound[55 ] <=  0  ;
evilLeftBound[56 ] <=  0  ;
evilLeftBound[57 ] <=  0  ;
evilLeftBound[58 ] <=  0  ;
evilLeftBound[59 ] <=  0  ;
evilLeftBound[60 ] <=  0  ;
evilLeftBound[61 ] <=  0  ;
```

```
evilLeftBound[62  ] <=      0   ;
evilLeftBound[63  ] <=      0   ;
evilLeftBound[64  ] <=      0   ;
evilLeftBound[65  ] <=      0   ;
evilLeftBound[66  ] <=      0   ;
evilLeftBound[67  ] <=      0   ;
evilLeftBound[68  ] <=      0   ;
evilLeftBound[69  ] <=      0   ;
evilLeftBound[70  ] <=      0   ;
evilLeftBound[71  ] <=      0   ;
evilLeftBound[72  ] <=      0   ;
evilLeftBound[73  ] <=      0   ;
evilLeftBound[74  ] <=      0   ;
evilLeftBound[75  ] <=      0   ;
evilLeftBound[76  ] <=      0   ;
evilLeftBound[77  ] <=      0   ;
evilLeftBound[78  ] <=      0   ;
evilLeftBound[79  ] <=      0   ;
evilLeftBound[80  ] <=      0   ;
evilLeftBound[81  ] <=      0   ;
evilLeftBound[82  ] <=      0   ;
evilLeftBound[83  ] <=      0   ;
evilLeftBound[84  ] <=      0   ;
evilLeftBound[85  ] <=      0   ;
evilLeftBound[86  ] <=      0   ;
evilLeftBound[87  ] <=      0   ;
evilLeftBound[88  ] <=      0   ;
evilLeftBound[89  ] <=      0   ;
evilLeftBound[90  ] <=      0   ;
evilLeftBound[91  ] <=      0   ;
evilLeftBound[92  ] <=      0   ;
evilLeftBound[93  ] <=      0   ;
evilLeftBound[94  ] <=      0   ;
evilLeftBound[95  ] <=      0   ;
evilLeftBound[96  ] <=      0   ;
evilLeftBound[97  ] <=      0   ;
evilLeftBound[98  ] <=      0   ;
evilLeftBound[99  ] <=      0   ;
evilLeftBound[100 ] <=      0   ;
evilLeftBound[101 ] <=      0   ;
evilLeftBound[102 ] <=      0   ;
evilLeftBound[103 ] <=      0   ;
evilLeftBound[104 ] <=      0   ;
evilLeftBound[105 ] <=      0   ;
evilLeftBound[106 ] <=      0   ;
evilLeftBound[107 ] <=      0   ;
evilLeftBound[108 ] <=      0   ;
evilLeftBound[109 ] <=      0   ;
evilLeftBound[110 ] <=      0   ;
evilLeftBound[111 ] <=      0   ;
evilLeftBound[112 ] <=      0   ;
evilLeftBound[113 ] <=      0   ;
evilLeftBound[114 ] <=      0   ;
evilLeftBound[115 ] <=      0   ;
evilLeftBound[116 ] <=      0   ;
evilLeftBound[117 ] <=      0   ;
evilLeftBound[118 ] <=      0   ;
evilLeftBound[119 ] <=      0   ;
```

```
evilRightBound[  0  ] <=  0  ;
evilRightBound[  1  ] <=  0  ;
evilRightBound[  2  ] <=  0  ;
evilRightBound[  3  ] <=  0  ;
evilRightBound[  4  ] <=  0  ;
evilRightBound[  5  ] <=  0  ;
evilRightBound[  6  ] <=  0  ;
evilRightBound[  7  ] <=  0  ;
evilRightBound[  8  ] <=  0  ;
evilRightBound[  9  ] <=  0  ;
evilRightBound[  10  ] <=  0  ;
evilRightBound[  11  ] <=  0  ;
evilRightBound[  12  ] <=  0  ;
evilRightBound[  13  ] <=  0  ;
evilRightBound[  14  ] <=  0  ;
evilRightBound[  15  ] <=  0  ;
evilRightBound[  16  ] <=  0  ;
evilRightBound[  17  ] <=  0  ;
evilRightBound[  18  ] <=  0  ;
evilRightBound[  19  ] <=  0  ;
evilRightBound[  20  ] <=  0  ;
evilRightBound[  21  ] <=  0  ;
evilRightBound[  22  ] <=  0  ;
evilRightBound[  23  ] <=  0  ;
evilRightBound[  24  ] <=  0  ;
evilRightBound[  25  ] <=  0  ;
evilRightBound[  26  ] <=  0  ;
evilRightBound[  27  ] <=  0  ;
evilRightBound[  28  ] <=  0  ;
evilRightBound[  29  ] <=  0  ;
evilRightBound[  30  ] <=  0  ;
evilRightBound[  31  ] <=  0  ;
evilRightBound[  32  ] <=  0  ;
evilRightBound[  33  ] <=  0  ;
evilRightBound[  34  ] <=  0  ;
evilRightBound[  35  ] <=  0  ;
evilRightBound[  36  ] <=  0  ;
evilRightBound[  37  ] <=  0  ;
evilRightBound[  38  ] <=  0  ;
evilRightBound[  39  ] <=  0  ;
evilRightBound[  40  ] <=  0  ;
evilRightBound[  41  ] <=  0  ;
evilRightBound[  42  ] <=  0  ;
evilRightBound[  43  ] <=  0  ;
evilRightBound[  44  ] <=  0  ;
evilRightBound[  45  ] <=  0  ;
evilRightBound[  46  ] <=  0  ;
evilRightBound[  47  ] <=  0  ;
evilRightBound[  48  ] <=  0  ;
evilRightBound[  49  ] <=  0  ;
evilRightBound[  50  ] <=  0  ;
evilRightBound[  51  ] <=  0  ;
evilRightBound[  52  ] <=  0  ;
evilRightBound[  53  ] <=  0  ;
evilRightBound[  54  ] <=  0  ;
evilRightBound[  55  ] <=  0  ;
evilRightBound[  56  ] <=  0  ;
```

```
evilRightBound[  57 ] <=  0 ;
evilRightBound[  58 ] <=  0 ;
evilRightBound[  59 ] <=  0 ;
evilRightBound[  60 ] <=  0 ;
evilRightBound[  61 ] <=  0 ;
evilRightBound[  62 ] <=  0 ;
evilRightBound[  63 ] <=  0 ;
evilRightBound[  64 ] <=  0 ;
evilRightBound[  65 ] <=  0 ;
evilRightBound[  66 ] <=  0 ;
evilRightBound[  67 ] <=  0 ;
evilRightBound[  68 ] <=  0 ;
evilRightBound[  69 ] <=  0 ;
evilRightBound[  70 ] <=  0 ;
evilRightBound[  71 ] <=  0 ;
evilRightBound[  72 ] <=  0 ;
evilRightBound[  73 ] <=  0 ;
evilRightBound[  74 ] <=  0 ;
evilRightBound[  75 ] <=  0 ;
evilRightBound[  76 ] <=  0 ;
evilRightBound[  77 ] <=  0 ;
evilRightBound[  78 ] <=  0 ;
evilRightBound[  79 ] <=  0 ;
evilRightBound[  80 ] <=  0 ;
evilRightBound[  81 ] <=  0 ;
evilRightBound[  82 ] <=  0 ;
evilRightBound[  83 ] <=  0 ;
evilRightBound[  84 ] <=  0 ;
evilRightBound[  85 ] <=  0 ;
evilRightBound[  86 ] <=  0 ;
evilRightBound[  87 ] <=  0 ;
evilRightBound[  88 ] <=  0 ;
evilRightBound[  89 ] <=  0 ;
evilRightBound[  90 ] <=  0 ;
evilRightBound[  91 ] <=  0 ;
evilRightBound[  92 ] <=  0 ;
evilRightBound[  93 ] <=  0 ;
evilRightBound[  94 ] <=  0 ;
evilRightBound[  95 ] <=  0 ;
evilRightBound[  96 ] <=  0 ;
evilRightBound[  97 ] <=  0 ;
evilRightBound[  98 ] <=  0 ;
evilRightBound[  99 ] <=  0 ;
evilRightBound[ 100 ] <=  0 ;
evilRightBound[ 101 ] <=  0 ;
evilRightBound[ 102 ] <=  0 ;
evilRightBound[ 103 ] <=  0 ;
evilRightBound[ 104 ] <=  0 ;
evilRightBound[ 105 ] <=  0 ;
evilRightBound[ 106 ] <=  0 ;
evilRightBound[ 107 ] <=  0 ;
evilRightBound[ 108 ] <=  0 ;
evilRightBound[ 109 ] <=  0 ;
evilRightBound[ 110 ] <=  0 ;
evilRightBound[ 111 ] <=  0 ;
evilRightBound[ 112 ] <=  0 ;
evilRightBound[ 113 ] <=  0 ;
evilRightBound[ 114 ] <=  0 ;
```

```
                evilRightBound[   115 ] <=      0   ;
                evilRightBound[   116 ] <=      0   ;
                evilRightBound[   117 ] <=      0   ;
                evilRightBound[   118 ] <=      0   ;
                evilRightBound[   119 ] <=      0   ;

        end
else
    begin
                                        evilLeftBound[0   ] <=      57  ;
                evilLeftBound[  1   ] <=      51  ;
                evilLeftBound[  2   ] <=      47  ;
                evilLeftBound[  3   ] <=      44  ;
                evilLeftBound[  4   ] <=      42  ;
                evilLeftBound[  5   ] <=      38  ;
                evilLeftBound[  6   ] <=      36  ;
                evilLeftBound[  7   ] <=      36  ;
                evilLeftBound[  8   ] <=      33  ;
                evilLeftBound[  9   ] <=      32  ;
                evilLeftBound[  10  ] <=      31  ;
                evilLeftBound[  11  ] <=      29  ;
                evilLeftBound[  12  ] <=      28  ;
                evilLeftBound[  13  ] <=      26  ;
                evilLeftBound[  14  ] <=      24  ;
                evilLeftBound[  15  ] <=      24  ;
                evilLeftBound[  16  ] <=      20  ;
                evilLeftBound[  17  ] <=      20  ;
                evilLeftBound[  18  ] <=      20  ;
                evilLeftBound[  19  ] <=      20  ;
                evilLeftBound[  20  ] <=      19  ;
                evilLeftBound[  21  ] <=      18  ;
                evilLeftBound[  22  ] <=      18  ;
                evilLeftBound[  23  ] <=      16  ;
                evilLeftBound[  24  ] <=      16  ;
                evilLeftBound[  25  ] <=      16  ;
                evilLeftBound[  26  ] <=      13  ;
                evilLeftBound[  27  ] <=      13  ;
                evilLeftBound[  28  ] <=      13  ;
                evilLeftBound[  29  ] <=      13  ;
                evilLeftBound[  30  ] <=      12  ;
                evilLeftBound[  31  ] <=      10  ;
                evilLeftBound[  32  ] <=      11  ;
                evilLeftBound[  33  ] <=      10  ;
                evilLeftBound[  34  ] <=      9   ;
                evilLeftBound[  35  ] <=      10  ;
                evilLeftBound[  36  ] <=      9   ;
                evilLeftBound[  37  ] <=      9   ;
                evilLeftBound[  38  ] <=      9   ;
                evilLeftBound[  39  ] <=      9   ;
                evilLeftBound[  40  ] <=      9   ;
                evilLeftBound[  41  ] <=      7   ;
                evilLeftBound[  42  ] <=      7   ;
                evilLeftBound[  43  ] <=      7   ;
                evilLeftBound[  44  ] <=      7   ;
                evilLeftBound[  45  ] <=      7   ;
                evilLeftBound[  46  ] <=      7   ;
                evilLeftBound[  47  ] <=      7   ;
                evilLeftBound[  48  ] <=      6   ;
```

```
evilLeftBound[  49  ] <=    7  ;
evilLeftBound[  50  ] <=    7  ;
evilLeftBound[  51  ] <=    6  ;
evilLeftBound[  52  ] <=    6  ;
evilLeftBound[  53  ] <=    6  ;
evilLeftBound[  54  ] <=    6  ;
evilLeftBound[  55  ] <=    6  ;
evilLeftBound[  56  ] <=    6  ;
evilLeftBound[  57  ] <=    6  ;
evilLeftBound[  58  ] <=    6  ;
evilLeftBound[  59  ] <=    6  ;
evilLeftBound[  60  ] <=    7  ;
evilLeftBound[  61  ] <=    7  ;
evilLeftBound[  62  ] <=    7  ;
evilLeftBound[  63  ] <=    7  ;
evilLeftBound[  64  ] <=    7  ;
evilLeftBound[  65  ] <=    7  ;
evilLeftBound[  66  ] <=    7  ;
evilLeftBound[  67  ] <=    8  ;
evilLeftBound[  68  ] <=    8  ;
evilLeftBound[  69  ] <=    9  ;
evilLeftBound[  70  ] <=    9  ;
evilLeftBound[  71  ] <=    10 ;
evilLeftBound[  72  ] <=    10 ;
evilLeftBound[  73  ] <=    10 ;
evilLeftBound[  74  ] <=    11 ;
evilLeftBound[  75  ] <=    11 ;
evilLeftBound[  76  ] <=    11 ;
evilLeftBound[  77  ] <=    12 ;
evilLeftBound[  78  ] <=    14 ;
evilLeftBound[  79  ] <=    14 ;
evilLeftBound[  80  ] <=    15 ;
evilLeftBound[  81  ] <=    15 ;
evilLeftBound[  82  ] <=    16 ;
evilLeftBound[  83  ] <=    17 ;
evilLeftBound[  84  ] <=    18 ;
evilLeftBound[  85  ] <=    19 ;
evilLeftBound[  86  ] <=    20 ;
evilLeftBound[  87  ] <=    19 ;
evilLeftBound[  88  ] <=    21 ;
evilLeftBound[  89  ] <=    23 ;
evilLeftBound[  90  ] <=    24 ;
evilLeftBound[  91  ] <=    25 ;
evilLeftBound[  92  ] <=    23 ;
evilLeftBound[  93  ] <=    27 ;
evilLeftBound[  94  ] <=    27 ;
evilLeftBound[  95  ] <=    28 ;
evilLeftBound[  96  ] <=    28 ;
evilLeftBound[  97  ] <=    28 ;
evilLeftBound[  98  ] <=    28 ;
evilLeftBound[  99  ] <=    27 ;
evilLeftBound[  100 ] <=    27 ;
evilLeftBound[  101 ] <=    27 ;
evilLeftBound[  102 ] <=    27 ;
evilLeftBound[  103 ] <=    27 ;
evilLeftBound[  104 ] <=    27 ;
evilLeftBound[  105 ] <=    27 ;
evilLeftBound[  106 ] <=    27 ;
```

```
evilLeftBound[  107  ] <=      27   ;
evilLeftBound[  108  ] <=      28   ;
evilLeftBound[  109  ] <=      27   ;
evilLeftBound[  110  ] <=      27   ;
evilLeftBound[  111  ] <=      27   ;
evilLeftBound[  112  ] <=      27   ;
evilLeftBound[  113  ] <=      28   ;
evilLeftBound[  114  ] <=      28   ;
evilLeftBound[  115  ] <=      28   ;
evilLeftBound[  116  ] <=      29   ;
evilLeftBound[  117  ] <=      29   ;
evilLeftBound[  118  ] <=      29   ;
evilLeftBound[  119  ] <=      30   ;

evilRightBound[0     ] <=      58   ;
evilRightBound[1     ] <=      70   ;
evilRightBound[2     ] <=      74   ;
evilRightBound[3     ] <=      77   ;
evilRightBound[4     ] <=      82   ;
evilRightBound[5     ] <=      81   ;
evilRightBound[6     ] <=      84   ;
evilRightBound[7     ] <=      85   ;
evilRightBound[8     ] <=      87   ;
evilRightBound[9     ] <=      90   ;
evilRightBound[10    ] <=      90   ;
evilRightBound[11    ] <=      91   ;
evilRightBound[12    ] <=      93   ;
evilRightBound[13    ] <=      94   ;
evilRightBound[14    ] <=      95   ;
evilRightBound[15    ] <=      96   ;
evilRightBound[16    ] <=      97   ;
evilRightBound[17    ] <=      21   ;
evilRightBound[18    ] <=      99   ;
evilRightBound[19    ] <=      100  ;
evilRightBound[20    ] <=      101  ;
evilRightBound[21    ] <=      101  ;
evilRightBound[22    ] <=      102  ;
evilRightBound[23    ] <=      103  ;
evilRightBound[24    ] <=      103  ;
evilRightBound[25    ] <=      104  ;
evilRightBound[26    ] <=      104  ;
evilRightBound[27    ] <=      106  ;
evilRightBound[28    ] <=      107  ;
evilRightBound[29    ] <=      107  ;
evilRightBound[30    ] <=      107  ;
evilRightBound[31    ] <=      107  ;
evilRightBound[32    ] <=      108  ;
evilRightBound[33    ] <=      109  ;
evilRightBound[34    ] <=      109  ;
evilRightBound[35    ] <=      109  ;
evilRightBound[36    ] <=      110  ;
evilRightBound[37    ] <=      110  ;
evilRightBound[38    ] <=      110  ;
evilRightBound[39    ] <=      111  ;
evilRightBound[40    ] <=      111  ;
evilRightBound[41    ] <=      112  ;
evilRightBound[42    ] <=      112  ;
evilRightBound[43    ] <=      112  ;
```

```
evilRightBound[44  ] <=      112 ;
evilRightBound[45  ] <=      112 ;
evilRightBound[46  ] <=      113 ;
evilRightBound[47  ] <=      113 ;
evilRightBound[48  ] <=      113 ;
evilRightBound[49  ] <=      114 ;
evilRightBound[50  ] <=      114 ;
evilRightBound[51  ] <=      114 ;
evilRightBound[52  ] <=      114 ;
evilRightBound[53  ] <=      114 ;
evilRightBound[54  ] <=      114 ;
evilRightBound[55  ] <=      114 ;
evilRightBound[56  ] <=      114 ;
evilRightBound[57  ] <=      114 ;
evilRightBound[58  ] <=      114 ;
evilRightBound[59  ] <=      114 ;
evilRightBound[60  ] <=      114 ;
evilRightBound[61  ] <=      114 ;
evilRightBound[62  ] <=      114 ;
evilRightBound[63  ] <=      114 ;
evilRightBound[64  ] <=      113 ;
evilRightBound[65  ] <=      113 ;
evilRightBound[66  ] <=      113 ;
evilRightBound[67  ] <=      113 ;
evilRightBound[68  ] <=      112 ;
evilRightBound[69  ] <=      112 ;
evilRightBound[70  ] <=      112 ;
evilRightBound[71  ] <=      111 ;
evilRightBound[72  ] <=      112 ;
evilRightBound[73  ] <=      110 ;
evilRightBound[74  ] <=      110 ;
evilRightBound[75  ] <=      110 ;
evilRightBound[76  ] <=      109 ;
evilRightBound[77  ] <=      109 ;
evilRightBound[78  ] <=      108 ;
evilRightBound[79  ] <=      108 ;
evilRightBound[80  ] <=      108 ;
evilRightBound[81  ] <=      108 ;
evilRightBound[82  ] <=      106 ;
evilRightBound[83  ] <=      105 ;
evilRightBound[84  ] <=      104 ;
evilRightBound[85  ] <=      104 ;
evilRightBound[86  ] <=      104 ;
evilRightBound[87  ] <=      102 ;
evilRightBound[88  ] <=      103 ;
evilRightBound[89  ] <=      100 ;
evilRightBound[90  ] <=      99  ;
evilRightBound[91  ] <=      98  ;
evilRightBound[92  ] <=      97  ;
evilRightBound[93  ] <=      95  ;
evilRightBound[94  ] <=      95  ;
evilRightBound[95  ] <=      94  ;
evilRightBound[96  ] <=      94  ;
evilRightBound[97  ] <=      94  ;
evilRightBound[98  ] <=      94  ;
evilRightBound[99  ] <=      94  ;
evilRightBound[100 ] <=      94  ;
evilRightBound[101 ] <=      94  ;
```

```
                                evilRightBound[102  ] <=      94   ;
                                evilRightBound[103  ] <=      94   ;
                                evilRightBound[104  ] <=      94   ;
                                evilRightBound[105  ] <=      94   ;
                                evilRightBound[106  ] <=      94   ;
                                evilRightBound[107  ] <=      94   ;
                                evilRightBound[108  ] <=      94   ;
                                evilRightBound[109  ] <=      94   ;
                                evilRightBound[110  ] <=      94   ;
                                evilRightBound[111  ] <=      94   ;
                                evilRightBound[112  ] <=      94   ;
                                evilRightBound[113  ] <=      94   ;
                                evilRightBound[114  ] <=      93   ;
                                evilRightBound[115  ] <=      94   ;
                                evilRightBound[116  ] <=      93   ;
                                evilRightBound[117  ] <=      93   ;
                                evilRightBound[118  ] <=      93   ;
                                evilRightBound[119  ] <=      92   ;
        end
end

assign mole0[0] = moleControl[0] ? 1: 0;
    assign mole0[1] = moleControl[1] ? 1: 0;
    assign updn0 = moleControl[2] ? 1: 0;

    assign mole1[0] = moleControl[3] ? 1: 0;
    assign mole1[1] = moleControl[4] ? 1: 0;
    assign updn1 = moleControl[5] ? 1: 0;

    assign mole2[0] = moleControl[6] ? 1: 0;
    assign mole2[1] = moleControl[7] ? 1: 0;
    assign updn2 = moleControl[8] ? 1: 0;


    assign mole3[0] = moleControl[9] ? 1: 0;
    assign mole3[1] = moleControl[10] ? 1: 0;
    assign updn3 = moleControl[11] ? 1: 0;

    assign mole4[0] = moleControl[12] ? 1: 0;
    assign mole4[1] = moleControl[13] ? 1: 0;
    assign updn4 = moleControl[14] ? 1: 0;

    assign mole5[0] = moleControl[15] ? 1: 0;
    assign mole5[1] = moleControl[16] ? 1: 0;
    assign updn5 = moleControl[17] ? 1: 0;

    assign mole6[0] = moleControl[18] ? 1: 0;
    assign mole6[1] = moleControl[19] ? 1: 0;
    assign updn6 = moleControl[20] ? 1: 0;

    assign mole7[0] = moleControl[21] ? 1: 0;
    assign mole7[1] = moleControl[22] ? 1: 0;
    assign updn7 = moleControl[23] ? 1: 0;

    assign mole8[0] = moleControl[24] ? 1: 0;
    assign mole8[1] = moleControl[25] ? 1: 0;
    assign updn8 = moleControl[26] ? 1: 0;
```

```
//Calculate the height of the mole0
always@(posedge iCLK or negedge iRST_n)
	begin
		if(!iRST_n)
			begin
			  moleHeight[0] <= 0;
			  counter00 <=0;
			 end
		 else if(updn0==1 && moleHeight[0]<118)
		    begin
				counter00 <= counter00 +1;
				 if(counter00 == 30000)
				    begin
				    moleHeight[0] <= moleHeight[0] +1;
					counter00 <=0;
					 end
		  end
		 else if(updn0==0)
			begin
				moleHeight[0] <= 0;
				 counter00 <=0;
			end
		 else
			begin
				moleHeight[0] <= moleHeight[0];
				 counter00 <=0;
			end
	  end

	  //Calculate the height of the mole1
always@(posedge iCLK or negedge iRST_n)
	begin
		if(!iRST_n)
			begin
			  moleHeight[1] <= 0;
			  counter11 <=0;
			 end
		 else if(updn1==1 && moleHeight[1]<118)
		    begin
				counter11 <= counter11 +1;
				 if(counter11 == 30000)
				    begin
				    moleHeight[1] <= moleHeight[1] +1;
					counter11 <=0;
					 end
		  end
		 else if(updn1==0)
			begin
				moleHeight[1] <= 0;
				 counter11 <=0;
			end
		 else
			begin
				moleHeight[1] <= moleHeight[1];
				 counter11 <=0;
			end
	  end
```

```
        //Calculate the height of the mole2
always@(posedge iCLK or negedge iRST_n)
    begin
        if(!iRST_n)
            begin
              moleHeight[2] <= 0;
              counter22 <=0;
             end
         else if(updn2==1 && moleHeight[2]<118)
            begin
                counter22 <= counter22 +1;
                 if(counter22 == 30000)
                    begin
                    moleHeight[2] <= moleHeight[2] +1;
                        counter22 <=0;
                     end
          end
         else if(updn2==0)
            begin
                moleHeight[2] <= 0;
                 counter22 <=0;
            end
         else
            begin
                moleHeight[2] <= moleHeight[2];
                 counter22 <=0;
            end
      end


        //Calculate the height of the mole3
always@(posedge iCLK or negedge iRST_n)
    begin
        if(!iRST_n)
            begin
              moleHeight[3] <= 0;
              counter33 <=0;
             end
         else if(updn3==1 && moleHeight[3]<118)
            begin
                counter33 <= counter33 +1;
                 if(counter33 == 30000)
                    begin
                    moleHeight[3] <= moleHeight[3] +1;
                        counter33 <=0;
                     end
          end
         else if(updn3==0)
            begin
                moleHeight[3] <= 0;
                 counter33 <=0;
            end
         else
            begin
                moleHeight[3] <= moleHeight[3];
                 counter33 <=0;
```

```
            end
        end


        //Calculate the height of the mole4
always@(posedge iCLK or negedge iRST_n)
    begin
        if(!iRST_n)
            begin
              moleHeight[4] <= 0;
              counter44 <=0;
             end
          else if(updn4==1 && moleHeight[4]<118)
             begin
                  counter44 <= counter44 +1;
                   if(counter44 == 30000)
                      begin
                      moleHeight[4] <= moleHeight[4] +1;
                          counter44 <=0;
                       end
           end
          else if(updn4==0)
              begin
                  moleHeight[4] <= 0;
                   counter44 <=0;
              end
          else
              begin
                  moleHeight[4] <= moleHeight[4];
                   counter44 <=0;
              end
        end


        //Calculate the height of the mole5
always@(posedge iCLK or negedge iRST_n)
    begin
        if(!iRST_n)
            begin
              moleHeight[5] <= 0;
              counter55 <=0;
             end
          else if(updn5==1 && moleHeight[5]<118)
             begin
                  counter55 <= counter55 +1;
                   if(counter55 == 30000)
                      begin
                      moleHeight[5] <= moleHeight[5] +1;
                          counter55 <=0;
                       end
           end
          else if(updn5==0)
              begin
                  moleHeight[5] <= 0;
                   counter55 <=0;
              end
          else
              begin
```

```
                    moleHeight[5] <= moleHeight[5];
                     counter55 <=0;
                end
        end

        //Calculate the height of the mole6
always@(posedge iCLK or negedge iRST_n)
    begin
        if(!iRST_n)
            begin
               moleHeight[6] <= 0;
               counter66 <=0;
             end
          else if(updn6==1 && moleHeight[6]<118)
             begin
                    counter66 <= counter66 +1;
                     if(counter66 == 30000)
                        begin
                        moleHeight[6] <= moleHeight[6] +1;
                            counter66 <=0;
                         end
           end
          else if(updn6==0)
            begin
                    moleHeight[6] <= 0;
                     counter66 <=0;
                end
          else
            begin
                    moleHeight[6] <= moleHeight[6];
                     counter66 <=0;
                end
        end

        //Calculate the height of the mole7
always@(posedge iCLK or negedge iRST_n)
    begin
        if(!iRST_n)
            begin
               moleHeight[7] <= 0;
               counter77 <=0;
             end
          else if(updn7==1 && moleHeight[7]<118)
             begin
                    counter77 <= counter77 +1;
                     if(counter77 == 30000)
                        begin
                        moleHeight[7] <= moleHeight[7] +1;
                            counter77 <=0;
                         end
           end
          else if(updn7==0)
            begin
                    moleHeight[7] <= 0;
                     counter77 <=0;
                end
          else
            begin
```

```
                    moleHeight[7] <= moleHeight[7];
                     counter77 <=0;
                end
        end

        //Calculate the height of the mole8
always@(posedge iCLK or negedge iRST_n)
      begin
          if(!iRST_n)
               begin
                  moleHeight[8] <= 0;
                  counter88 <=0;
                end
            else if(updn8==1 && moleHeight[8]<118)
               begin
                    counter88 <= counter88 +1;
                     if(counter88 == 30000)
                        begin
                        moleHeight[8] <= moleHeight[8] +1;
                            counter88 <=0;
                         end
             end
            else if(updn8==0)
               begin
                    moleHeight[8] <= 0;
                     counter88 <=0;
               end
            else
               begin
                    moleHeight[8] <= moleHeight[8];
                     counter88 <=0;
               end
        end




//Detect which area you are in// 0~14 different areas
assign area[0] = ((x_cnt>(Hsync_Blank-1+400)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-200))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                                ))    ? 1'b1 : 1'b0 ; //mole0
assign area[1] = ((x_cnt>(Hsync_Blank-1+200)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-400))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                                ))    ? 1'b1 : 1'b0;//mole1
assign area[2] = ((x_cnt>(Hsync_Blank-1)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-600))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                                ))    ? 1'b1 : 1'b0 ;//mole2
assign area[3] = ((x_cnt>(Hsync_Blank-1+400)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-200))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
```

```
                                ))    ? 1'b1 : 1'b0 ;    //mole3
assign area[4] = ((x_cnt>(Hsync_Blank-1+200)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-400))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                                ))    ? 1'b1 : 1'b0 ; //mole4
assign area[5] = ((x_cnt>(Hsync_Blank-1)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-600))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                                ))    ? 1'b1 : 1'b0 ;//mole5
assign area[6] = ((x_cnt>(Hsync_Blank-1+400)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-200))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0 ;    //mole6
assign area[7] = ((x_cnt>(Hsync_Blank-1+200)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-400))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0; //mole7
assign area[8] = ((x_cnt>(Hsync_Blank-1)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-600))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0 ;//mole8
assign area[9] = ((x_cnt>(Hsync_Blank-1+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-400))
                                ))    ? 1'b1 : 1'b0 ;//area 9 Time
assign area[10] = ((x_cnt>(Hsync_Blank-1+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+80))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                                ))    ? 1'b1 : 1'b0 ;//area 10 life
assign area[11] = ((x_cnt>(Hsync_Blank-1+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-240))
                                ))    ? 1'b1 : 1'b0 ;//area 11 score
assign area[12] = ((x_cnt>(Hsync_Blank-1+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+240))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                                ))    ? 1'b1 : 1'b0 ;//area 12 start/pause
assign area[13] = ((x_cnt>(Hsync_Blank-1+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-80))
                                ))    ? 1'b1 : 1'b0 ;//area 13 exit
assign area[14] = ((x_cnt>(Hsync_Blank-1+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+400))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0 ;//area 14 label
assign area[15] = 1'b0;
//area 15 is the logo of the team defalt black
```

```
//Test --Allocate color to each block
always@(posedge iCLK or negedge iRST_n)
	begin
	if (!iRST_n)
		begin
		mole_address <= moleBase;
		end
	else
		case(area)
				16'b0000000000000001: begin
					x_offset <= Hsync_Blank + 400;
					y_offset <= Vertical_Back_Porch;
				//get the diff between the current x_cnt and the left boundary of the hole
					bound_x <=	-x_cnt+x_offset+200-40;
				//get the diff between the current y_cnt and the horizontal center of the hole
						if(	y_cnt>120+y_offset)
							begin
							 abs_y		<=	y_cnt-120-y_offset;
							 end
						else
							begin
							  abs_y		<=	-y_cnt+120+y_offset;
						    end

						//get the diff between the current x_cnt and the vertical center of the hole
						if(x_cnt>100+x_offset)
							begin
							  abs_x		<=	x_cnt-100-x_offset;
							 end
						else
							begin
							  abs_x		<=	-x_cnt+100+x_offset;
							 end

						//mole out of the hole
						if(moleHeight[0]>0)
							begin
							  case(mole0)
							    2'b00:begin	//mole
								//mole out
								// inside mole area
							      if (y_cnt < y_offset + 135 && y_cnt > y_offset + 135 - moleHeight[0]&& bound_x > moleLeftBound[y_cnt-135-y_offset+moleHeight[0]]+1 &&bound_x < moleRightBound[y_cnt-135-y_offset+moleHeight[0]]-1 )
									begin
									//update the
```

```
mole_address
                                                    mole_address <=
moleBase + (y_cnt-135-y_offset+moleHeight[0])*120 + x_cnt-x_offset-40;
                                                        moleExist
<= 1;
                                                    end
                                                     //hole area
                                                else    if(    abs_y<15    &&
abs_x<hole[abs_y] )
                                                    begin
                                                        moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                    end
                                                else
                                                    begin
                                                        moleExist
<= 0;

mole_address <= 18'bZ ;
                                                    end
                                                end
                                                2'b10:begin    //bottle
                                                      // bottle out
                                                     // inside bottle area
                                                  if    (y_cnt    <    y_offset    +
135    &&    y_cnt    >    y_offset    +    135    -    moleHeight[0]&&    bound_x    >
bottleLeftBound[y_cnt-135-y_offset+moleHeight[0]]+1              &&bound_x              <
bottleRightBound[y_cnt-135-y_offset+moleHeight[0]]-1    )
                                                     begin
                                                           //update    the
mole_address
                                                        mole_address <=
moleBase+bottleOffset + (y_cnt-135-y_offset+moleHeight[0])*120 + x_cnt-x_offset-40;
                                                        moleExist
<= 1;
                                                    end
                                                     //hole area
                                                else    if(    abs_y<15    &&
abs_x<hole[abs_y] )
                                                    begin
                                                        moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                    end
                                                else
                                                    begin
                                                        moleExist
<= 0;

mole_address <= 18'bZ ;
                                                    end
                                                end
                                                2'b01:begin    //evil
                                                      // bottle out
                                                     // inside bottle area
```

```
                                                    if (y_cnt < y_offset + 135 && y_cnt > y_offset + 135 - moleHeight[0]&& bound_x > evilLeftBound[y_cnt-135-y_offset+moleHeight[0]]+1 &&bound_x < evilRightBound[y_cnt-135-y_offset+moleHeight[0]]-1 )
                                                        begin
                                                            //update the mole_address
                                                            mole_address <= moleBase+evilOffset + (y_cnt-135-y_offset+moleHeight[0])*120 + x_cnt-x_offset-40;
                                                            moleExist <= 1;
                                                        end
                                                        //hole area
                                                    else if( abs_y<15 && abs_x<hole[abs_y] )
                                                        begin
                                                            moleExist <= 1;

mole_address <= moleBase + 120*120;
                                                        end
                                                    else
                                                        begin
                                                            moleExist <= 0;

mole_address <= 18'bZ ;
                                                        end
                                                end

                                            endcase
                                                end
                                        //no mole
                                        else
                                            if( abs_y<15 && abs_x<hole[abs_y] )
                                                begin
                                                    moleExist <= 1;
                                                    mole_address <= moleBase + 120*120;
                                                end
                                        else
                                                begin
                                                    moleExist <= 0;
                                                    mole_address <= 18'bZ ;
                                                end
                                    end



            16'b0000000000000010: begin x_offset <= Hsync_Blank + 200;
                                        y_offset <= Vertical_Back_Porch;
                                        //get the diff between the current x_cnt and the left boundary of the hole
                                        bound_x <= -x_cnt+x_offset+200-40;
                                        //get the diff between the current
```

```
y_cnt and the horizontal center of the hole
                                                    if( y_cnt>120+y_offset)
                                                      begin
                                                       abs_y                    <=
      y_cnt-120-y_offset;
                                                       end
                                                   else
                                                      begin
                                                         abs_y                  <=
      -y_cnt+120+y_offset;
                                                     end
                                                   //get the diff between the current
x_cnt and the vertical center of the hole
                                                   if(x_cnt>100+x_offset)
                                                      begin
                                                        abs_x                   <=
      x_cnt-100-x_offset;
                                                       end
                                                   else
                                                      begin
                                                         abs_x                  <=
      -x_cnt+100+x_offset;
                                                       end


                                                   //mole out of the hole
                                                   if(moleHeight[1]>0)
                                                     begin
                                                           case(mole1)
                                                              2'b00:begin     //mole

                                                                   //mole out
                                                                   // inside mole area
                                                                if    (y_cnt    <    y_offset    +
135    &&    y_cnt    >    y_offset    +    135    -    moleHeight[1]&&    bound_x    >
moleLeftBound[y_cnt-135-y_offset+moleHeight[1]]+1          &&bound_x                <
moleRightBound[y_cnt-135-y_offset+moleHeight[1]]-1    )
                                                                   begin
                                                                          //update the
mole_address
                                                                      mole_address <=
moleBase + (y_cnt-135-y_offset+moleHeight[1])*120 + x_cnt-x_offset-40;
                                                                          moleExist
<= 1;
                                                                  end
                                                                   //hole area
                                                               else    if(    abs_y<15    &&
abs_x<hole[abs_y] )
                                                                  begin
                                                                          moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                                   end
                                                               else
                                                                  begin
                                                                          moleExist
<= 0;
```

```
mole_address <= 18'bZ ;
                                                                    end

                                                                end

                                                                    2'b10:begin
//bottle

                                                                    //bottle out
                                                                    // inside bottle area
                                                                if (y_cnt < y_offset +
135 && y_cnt > y_offset + 135 - moleHeight[1]&& bound_x >
bottleLeftBound[y_cnt-135-y_offset+moleHeight[1]]+1 &&bound_x <
bottleRightBound[y_cnt-135-y_offset+moleHeight[1]]-1 )
                                                                    begin
                                                                        //update the
mole_address
                                                                    mole_address <=
bottleOffset + moleBase + (y_cnt-135-y_offset+moleHeight[1])*120 + x_cnt-x_offset-40;
                                                                        moleExist
<= 1;
                                                                    end
                                                                    //hole area
                                                                else if( abs_y<15 &&
abs_x<hole[abs_y] )
                                                                    begin
                                                                        moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                                    end
                                                                else
                                                                    begin
                                                                        moleExist
<= 0;

mole_address <= 18'bZ ;
                                                                    end

                                                                end

                                                                    2'b01:begin     //evil

                                                                    //evil out
                                                                    // inside evil area
                                                                if (y_cnt < y_offset +
135 && y_cnt > y_offset + 135 - moleHeight[1]&& bound_x >
evilLeftBound[y_cnt-135-y_offset+moleHeight[1]]+1 &&bound_x <
evilRightBound[y_cnt-135-y_offset+moleHeight[1]]-1 )
                                                                    begin
                                                                        //update the
mole_address
                                                                    mole_address <=
evilOffset + moleBase + (y_cnt-135-y_offset+moleHeight[1])*120 + x_cnt-x_offset-40;
                                                                        moleExist
<= 1;
                                                                    end
```

```
                                                        //hole area
                                                    else    if(    abs_y<15    &&
abs_x<hole[abs_y] )
                                                        begin
                                                                moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                        end
                                                    else
                                                        begin
                                                                moleExist
<= 0;

mole_address <= 18'bZ ;
                                                        end

                                                        end


                                                endcase
                                                    end
                                            //no mole
                                             else
                                                if(             abs_y<15             &&
abs_x<hole[abs_y] )
                                                    begin
                                                            moleExist <= 1;
                                                            mole_address        <=
moleBase + 120*120;
                                                     end
                                                else
                                                    begin
                                                             moleExist <= 0;
                                                             mole_address      <=
18'bZ ;
                                                     end
                                        end


                16'b0000000000000100: begin    x_offset <= Hsync_Blank;
                                                y_offset <= Vertical_Back_Porch;
                                                    //get the diff between the current x_cnt
and the left boundary of the hole
                                                 bound_x <=    -x_cnt+x_offset+200-40;
                                                       //get the diff between the current
y_cnt and the horizontal center of the hole
                                                    if( y_cnt>120+y_offset)
                                                       begin
                                                         abs_y                          <=
      y_cnt-120-y_offset;
                                                        end
                                                   else
                                                        begin
                                                           abs_y                        <=
      -y_cnt+120+y_offset;
                                                       end
                                                   //get the diff between the current
```

```
x_cnt and the vertical center of the hole
                                                    if(x_cnt>100+x_offset)
                                                        begin
                                                          abs_x                    <=
        x_cnt-100-x_offset;
                                                         end
                                                    else
                                                        begin
                                                          abs_x                    <=
        -x_cnt+100+x_offset;
                                                         end


                                                    //mole out of the hole
                                                    if(moleHeight[2]>0)
                                                        begin
                                                            case(mole2)
                                                              2'b00:begin     //mole
                                                                    //mole out
                                                                    // inside mole area
                                                                if    (y_cnt    <    y_offset    +
135    &&    y_cnt    >    y_offset    +    135    -    moleHeight[2]&&    bound_x    >
moleLeftBound[y_cnt-135-y_offset+moleHeight[2]]+1            &&bound_x                <
moleRightBound[y_cnt-135-y_offset+moleHeight[2]]-1    )
                                                                    begin
                                                                          //update    the
mole_address
                                                                       mole_address <=
moleBase + (y_cnt-135-y_offset+moleHeight[2])*120 + x_cnt-x_offset-40;
                                                                          moleExist
<= 1;
                                                                    end
                                                                    //hole area
                                                                else    if(    abs_y<15    &&
abs_x<hole[abs_y] )
                                                                    begin
                                                                          moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                                    end
                                                                else
                                                                    begin
                                                                          moleExist
<= 0;

mole_address <= 18'bZ ;
                                                                    end

                                                                    end

                                                                  2'b10:begin
//bottle
                                                                    //mole out
                                                                    // inside mole area
                                                                if    (y_cnt    <    y_offset    +
135    &&    y_cnt    >    y_offset    +    135    -    moleHeight[2]&&    bound_x    >
bottleLeftBound[y_cnt-135-y_offset+moleHeight[2]]+1            &&bound_x                <
```

```
bottleRightBound[y_cnt-135-y_offset+moleHeight[2]]-1    )
                                                                    begin
                                                                        //update the
mole_address
                                                                    mole_address <=
bottleOffset+moleBase + (y_cnt-135-y_offset+moleHeight[2])*120 + x_cnt-x_offset-40;
                                                                    moleExist
<= 1;
                                                                end
                                                                //hole area
                                                            else if( abs_y<15 &&
abs_x<hole[abs_y] )
                                                                begin
                                                                    moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                                end
                                                            else
                                                                begin
                                                                    moleExist
<= 0;

mole_address <= 18'bZ ;
                                                                end

                                                                end
                                                                2'b01:begin
//evil
                                                                //mole out
                                                                // inside mole area
                                                            if (y_cnt < y_offset +
135 && y_cnt > y_offset + 135 - moleHeight[2]&& bound_x >
evilLeftBound[y_cnt-135-y_offset+moleHeight[2]]+1 &&bound_x <
evilRightBound[y_cnt-135-y_offset+moleHeight[2]]-1    )
                                                                    begin
                                                                        //update the
mole_address
                                                                    mole_address <=
evilOffset + moleBase + (y_cnt-135-y_offset+moleHeight[2])*120 + x_cnt-x_offset-40;
                                                                    moleExist
<= 1;
                                                                end
                                                                //hole area
                                                            else if( abs_y<15 &&
abs_x<hole[abs_y] )
                                                                begin
                                                                    moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                                end
                                                            else
                                                                begin
                                                                    moleExist
<= 0;

mole_address <= 18'bZ ;
```

```
                                                    end

                                                    end

                                                endcase
                                                    end
                                                //no mole
                                                 else
                                                   if(              abs_y<15              &&
abs_x<hole[abs_y] )
                                                       begin
                                                            moleExist <= 1;
                                                            mole_address        <=
moleBase + 120*120;
                                                        end
                                                 else
                                                       begin
                                                            moleExist <= 0;
                                                            mole_address       <=
18'bZ ;
                                                        end
                                             end
                    16'b0000000000001000: begin    x_offset <= Hsync_Blank + 400;
                                                    y_offset <= Vertical_Back_Porch + 160;
                                                    //get the diff between the current x_cnt
and the left boundary of the hole
                                                    bound_x <=    -x_cnt+x_offset+200-40;
                                                    //get the diff between the current
y_cnt and the horizontal center of the hole
                                                    if( y_cnt>120+y_offset)
                                                       begin
                                                         abs_y                          <=
      y_cnt-120-y_offset;
                                                        end
                                                    else
                                                       begin
                                                          abs_y                         <=
      -y_cnt+120+y_offset;
                                                       end
                                                    //get the diff between the current
x_cnt and the vertical center of the hole
                                                    if(x_cnt>100+x_offset)
                                                       begin
                                                         abs_x                          <=
      x_cnt-100-x_offset;
                                                        end
                                                    else
                                                       begin
                                                          abs_x                         <=
      -x_cnt+100+x_offset;
                                                        end


                                                    //mole out of the hole
                                                    if(moleHeight[3]>0)
                                                       begin
                                                            case(mole3)
                                                              2'b00:begin      //mole
```

```
                                                                    //mole out
                                                                    // inside mole area
                                                                if (y_cnt < y_offset + 135 && y_cnt > y_offset + 135 - moleHeight[3]&& bound_x > moleLeftBound[y_cnt-135-y_offset+moleHeight[3]]+1 &&bound_x < moleRightBound[y_cnt-135-y_offset+moleHeight[3]]-1 )
                                                                    begin
                                                                        //update the mole_address
                                                                        mole_address <= moleBase + (y_cnt-135-y_offset+moleHeight[3])*120 + x_cnt-x_offset-40;
                                                                        moleExist <= 1;
                                                                    end
                                                                    //hole area
                                                                else if( abs_y<15 && abs_x<hole[abs_y] )
                                                                    begin
                                                                        moleExist <= 1;

mole_address <= moleBase + 120*120;
                                                                    end
                                                                else
                                                                    begin
                                                                        moleExist <= 0;

mole_address <= 18'bZ ;
                                                                    end
                                                                end
                                                                2'b10:begin //bottle
                                                                    //mole out
                                                                    // inside mole area
                                                                if (y_cnt < y_offset + 135 && y_cnt > y_offset + 135 - moleHeight[3]&& bound_x > bottleLeftBound[y_cnt-135-y_offset+moleHeight[3]]+1 &&bound_x < bottleRightBound[y_cnt-135-y_offset+moleHeight[3]]-1 )
                                                                    begin
                                                                        //update the mole_address
                                                                        mole_address <= bottleOffset + moleBase + (y_cnt-135-y_offset+moleHeight[3])*120 + x_cnt-x_offset-40;
                                                                        moleExist <= 1;
                                                                    end
                                                                    //hole area
                                                                else if( abs_y<15 && abs_x<hole[abs_y] )
                                                                    begin
                                                                        moleExist <= 1;

mole_address <= moleBase + 120*120;
                                                                    end
                                                                else
                                                                    begin
                                                                        moleExist
```

```
<= 0;

mole_address <= 18'bZ ;
                                                                    end
                                                                end

                                                                2'b01:begin     //evil
                                                                    //mole out
                                                                    // inside mole area
                                                                if (y_cnt < y_offset + 135 && y_cnt > y_offset + 135 - moleHeight[3]&& bound_x > evilLeftBound[y_cnt-135-y_offset+moleHeight[3]]+1 &&bound_x < evilRightBound[y_cnt-135-y_offset+moleHeight[3]]-1 )
                                                                    begin
                                                                        //update the mole_address
                                                                        mole_address <= evilOffset + moleBase + (y_cnt-135-y_offset+moleHeight[3])*120 + x_cnt-x_offset-40;
                                                                        moleExist <= 1;
                                                                    end
                                                                    //hole area
                                                                else if( abs_y<15 && abs_x<hole[abs_y] )
                                                                    begin
                                                                        moleExist <= 1;

mole_address <= moleBase + 120*120;
                                                                    end
                                                                else
                                                                    begin
                                                                        moleExist <= 0;

mole_address <= 18'bZ ;
                                                                    end
                                                                end




                                                            endcase
                                                        end
                                                    //no mole
                                                    else
                                                        if( abs_y<15 && abs_x<hole[abs_y] )
                                                            begin
                                                                moleExist <= 1;
                                                                mole_address <= moleBase + 120*120;
                                                            end
                                                    else
                                                            begin
                                                                moleExist <= 0;
```

```
                                                                mole_address      <=
18'bZ ;
                                                            end
                                                    end
                    16'b0000000000010000: begin    x_offset <= Hsync_Blank + 200;
                                                        y_offset <= Vertical_Back_Porch + 160;
                                                        //get the diff between the current x_cnt
and the left boundary of the hole
                                                     bound_x <=    -x_cnt+x_offset+200-40;
                                                        //get the diff between the current
y_cnt and the horizontal center of the hole
                                                      if( y_cnt>120+y_offset)
                                                        begin
                                                          abs_y                          <=
      y_cnt-120-y_offset;
                                                          end
                                                    else
                                                        begin
                                                          abs_y                          <=
      -y_cnt+120+y_offset;
                                                      end
                                                    //get the diff between the current
x_cnt and the vertical center of the hole
                                                    if(x_cnt>100+x_offset)
                                                        begin
                                                          abs_x                          <=
      x_cnt-100-x_offset;
                                                          end
                                                    else
                                                        begin
                                                          abs_x                          <=
      -x_cnt+100+x_offset;
                                                          end


                                                    //mole out of the hole
                                                    if(moleHeight[4]>0)
                                                        begin
                                                            case(mole4)
                                                              2'b00:begin     //mole
                                                                    //mole out
                                                                    // inside mole area
                                                                if    (y_cnt  <  y_offset  +
135    &&    y_cnt    >    y_offset    +    135    -    moleHeight[4]&&    bound_x    >
moleLeftBound[y_cnt-135-y_offset+moleHeight[4]]+1                &&bound_x                <
moleRightBound[y_cnt-135-y_offset+moleHeight[4]]-1    )
                                                                    begin
                                                                        //update the
mole_address
                                                                    mole_address <=
moleBase + (y_cnt-135-y_offset+moleHeight[4])*120 + x_cnt-x_offset-40;
                                                                    moleExist
<= 1;
                                                                end
                                                                //hole area
                                                            else    if(    abs_y<15    &&
abs_x<hole[abs_y] )
                                                                begin
```

```
                                                                moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                            end
                                                        else
                                                            begin
                                                                moleExist
<= 0;

mole_address <= 18'bZ ;
                                                            end
                                                            end

                                                             2'b10:begin
//bottle
                                                             //mole out
                                                             // inside mole area
                                                        if   (y_cnt  <  y_offset  +
135  &&  y_cnt  >  y_offset  +  135  -  moleHeight[4]&&  bound_x  >
bottleLeftBound[y_cnt-135-y_offset+moleHeight[4]]+1          &&bound_x          <
bottleRightBound[y_cnt-135-y_offset+moleHeight[4]]-1   )
                                                             begin
                                                                    //update  the
mole_address
                                                                mole_address <=
bottleOffset + moleBase + (y_cnt-135-y_offset+moleHeight[4])*120 + x_cnt-x_offset-40;
                                                                moleExist
<= 1;
                                                            end
                                                             //hole area
                                                        else   if(   abs_y<15   &&
abs_x<hole[abs_y] )
                                                            begin
                                                                moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                            end
                                                        else
                                                            begin
                                                                moleExist
<= 0;

mole_address <= 18'bZ ;
                                                            end
                                                            end

                                                            2'b01:begin     //evil
                                                             //mole out
                                                             // inside mole area
                                                        if   (y_cnt  <  y_offset  +
135  &&  y_cnt  >  y_offset  +  135  -  moleHeight[4]&&  bound_x  >
evilLeftBound[y_cnt-135-y_offset+moleHeight[4]]+1          &&bound_x          <
evilRightBound[y_cnt-135-y_offset+moleHeight[4]]-1   )
                                                             begin
                                                                    //update  the
mole_address
```

```
                                                                    mole_address <=
evilOffset + moleBase + (y_cnt-135-y_offset+moleHeight[4])*120 + x_cnt-x_offset-40;
                                                                        moleExist
<= 1;
                                                                    end
                                                                     //hole area
                                                                else    if(    abs_y<15    &&
abs_x<hole[abs_y] )
                                                                    begin
                                                                        moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                                    end
                                                                else
                                                                    begin
                                                                        moleExist
<= 0;

mole_address <= 18'bZ ;
                                                                    end
                                                                    end




                                                                endcase
                                                                    end
                                                            //no mole
                                                             else
                                                                if(              abs_y<15              &&
abs_x<hole[abs_y] )
                                                                    begin
                                                                        moleExist <= 1;
                                                                        mole_address        <=
moleBase + 120*120;
                                                                     end
                                                             else
                                                                    begin
                                                                        moleExist <= 0;
                                                                        mole_address      <=
18'bZ ;
                                                                     end
                                                          end
                    16'b0000000000100000: begin    x_offset <= Hsync_Blank ;
                                                        y_offset <= Vertical_Back_Porch +160;
                                                            //get the diff between the current x_cnt
and the left boundary of the hole
                                                         bound_x <=     -x_cnt+x_offset+200-40;
                                                               //get the diff between the current
y_cnt and the horizontal center of the hole
                                                                 if( y_cnt>120+y_offset)
                                                                    begin
                                                                      abs_y                          <=
       y_cnt-120-y_offset;
                                                                     end
                                                                else
```

```
                                                    begin
                                                        abs_y                    <=
    -y_cnt+120+y_offset;
                                                    end
                                                //get the diff between the current
x_cnt and the vertical center of the hole
                                                if(x_cnt>100+x_offset)
                                                    begin
                                                      abs_x                      <=
    x_cnt-100-x_offset;
                                                     end
                                                else
                                                    begin
                                                        abs_x                    <=
    -x_cnt+100+x_offset;
                                                     end


                                                //mole out of the hole
                                                if(moleHeight[5]>0)
                                                    begin
                                                        case(mole5)
                                                           2'b00:begin          //mole


                                                                  //mole out
                                                                  // inside mole area
                                                               if    (y_cnt    <    y_offset    +
135    &&    y_cnt    >    y_offset    +    135    -    moleHeight[5]&&    bound_x    >
moleLeftBound[y_cnt-135-y_offset+moleHeight[5]]+1          &&bound_x          <
moleRightBound[y_cnt-135-y_offset+moleHeight[5]]-1    )
                                                                  begin
                                                                        //update the
mole_address
                                                                     mole_address <=
moleBase + (y_cnt-135-y_offset+moleHeight[5])*120 + x_cnt-x_offset-40;
                                                                        moleExist
<= 1;
                                                                  end
                                                                   //hole area
                                                              else    if(    abs_y<15    &&
abs_x<hole[abs_y] )
                                                                  begin
                                                                        moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                                  end
                                                              else
                                                                  begin
                                                                        moleExist
<= 0;

mole_address <= 18'bZ ;
                                                                  end
                                                                  end

                                                                  2'b10:begin
```

```
//bottle

                                                                    //mole out
                                                                    // inside mole area
                                                                if (y_cnt < y_offset + 135 && y_cnt > y_offset + 135 - moleHeight[5]&& bound_x > bottleLeftBound[y_cnt-135-y_offset+moleHeight[5]]+1 &&bound_x < bottleRightBound[y_cnt-135-y_offset+moleHeight[5]]-1 )
                                                                    begin
                                                                        //update the mole_address
                                                                        mole_address <= bottleOffset + moleBase + (y_cnt-135-y_offset+moleHeight[5])*120 + x_cnt-x_offset-40;
                                                                        moleExist <= 1;
                                                                    end
                                                                    //hole area
                                                                else if( abs_y<15 && abs_x<hole[abs_y] )
                                                                    begin
                                                                        moleExist <= 1;

mole_address <= moleBase + 120*120;
                                                                    end
                                                                else
                                                                    begin
                                                                        moleExist <= 0;

mole_address <= 18'bZ ;
                                                                    end
                                                                    end

                                                                    2'b01:begin     //evil

                                                                    //mole out
                                                                    // inside mole area
                                                                if (y_cnt < y_offset + 135 && y_cnt > y_offset + 135 - moleHeight[5]&& bound_x > evilLeftBound[y_cnt-135-y_offset+moleHeight[5]]+1 &&bound_x < evilRightBound[y_cnt-135-y_offset+moleHeight[5]]-1 )
                                                                    begin
                                                                        //update the mole_address
                                                                        mole_address <= evilOffset + moleBase + (y_cnt-135-y_offset+moleHeight[5])*120 + x_cnt-x_offset-40;
                                                                        moleExist <= 1;
                                                                    end
                                                                    //hole area
                                                                else if( abs_y<15 && abs_x<hole[abs_y] )
                                                                    begin
                                                                        moleExist <= 1;

mole_address <= moleBase + 120*120;
```

```
                                                    end
                                                else
                                                    begin
                                                        moleExist
<= 0;

mole_address <= 18'bZ ;
                                                    end
                                                    end



                                                endcase
                                                    end
                                            //no mole
                                              else
                                                if(          abs_y<15          &&
abs_x<hole[abs_y] )
                                                    begin
                                                        moleExist <= 1;
                                                        mole_address      <=
moleBase + 120*120;
                                                     end
                                                else
                                                    begin
                                                        moleExist <= 0;
                                                        mole_address      <=
18'bZ ;
                                                     end
                                            end
                16'b0000000001000000: begin    x_offset <= Hsync_Blank + 400;
                                                y_offset <= Vertical_Back_Porch +320;
                                                    //get the diff between the current x_cnt
and the left boundary of the hole
                                                 bound_x <=    -x_cnt+x_offset+200-40;
                                                    //get the diff between the current
y_cnt and the horizontal center of the hole
                                                  if( y_cnt>120+y_offset)
                                                    begin
                                                      abs_y                      <=
      y_cnt-120-y_offset;
                                                      end
                                                else
                                                    begin
                                                       abs_y                      <=
      -y_cnt+120+y_offset;
                                                   end
                                                //get the diff between the current
x_cnt and the vertical center of the hole
                                                if(x_cnt>100+x_offset)
                                                    begin
                                                      abs_x                      <=
      x_cnt-100-x_offset;
                                                     end
                                                else
                                                    begin
                                                       abs_x                      <=
      -x_cnt+100+x_offset;
```

```
                                                    end


                                                //mole out of the hole
                                                if(moleHeight[6]>0)
                                                    begin
                                                        case(mole6)
                                                            2'b00:begin          //mole


                                                                //mole out
                                                                // inside mole area
                                                            if    (y_cnt  <  y_offset  +
135    &&    y_cnt    >    y_offset    +    135    -    moleHeight[6]&&    bound_x    >
moleLeftBound[y_cnt-135-y_offset+moleHeight[6]]+1              &&bound_x              <
moleRightBound[y_cnt-135-y_offset+moleHeight[6]]-1    )
                                                                begin
                                                                        //update  the
mole_address
                                                                    mole_address <=
moleBase + (y_cnt-135-y_offset+moleHeight[6])*120 + x_cnt-x_offset-40;
                                                                        moleExist
<= 1;
                                                                end
                                                                //hole area
                                                            else    if(    abs_y<15    &&
abs_x<hole[abs_y] )
                                                                begin
                                                                        moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                                end
                                                            else
                                                                begin
                                                                        moleExist
<= 0;

mole_address <= 18'bZ ;
                                                                end
                                                                end


                                                                2'b10:begin
//mole

                                                                //mole out
                                                                // inside mole area
                                                            if    (y_cnt  <  y_offset  +
135    &&    y_cnt    >    y_offset    +    135    -    moleHeight[6]&&    bound_x    >
bottleLeftBound[y_cnt-135-y_offset+moleHeight[6]]+1              &&bound_x              <
bottleRightBound[y_cnt-135-y_offset+moleHeight[6]]-1    )
                                                                begin
                                                                        //update  the
mole_address
                                                                    mole_address <=
bottleOffset + moleBase + (y_cnt-135-y_offset+moleHeight[6])*120 + x_cnt-x_offset-40;
                                                                        moleExist
<= 1;
```

```
                                                    end
                                                    //hole area
                                                else if( abs_y<15 &&
abs_x<hole[abs_y] )
                                                    begin
                                                        moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                    end
                                                else
                                                    begin
                                                        moleExist
<= 0;

mole_address <= 18'bZ ;
                                                    end
                                                    end

                                                    2'b01:begin
//mole

                                                    //mole out
                                                    // inside mole area
                                                if (y_cnt < y_offset +
135 && y_cnt > y_offset + 135 - moleHeight[6]&& bound_x >
evilLeftBound[y_cnt-135-y_offset+moleHeight[6]]+1 &&bound_x <
evilRightBound[y_cnt-135-y_offset+moleHeight[6]]-1 )
                                                    begin
                                                        //update the
mole_address
                                                    mole_address <=
evilOffset + moleBase + (y_cnt-135-y_offset+moleHeight[6])*120 + x_cnt-x_offset-40;
                                                        moleExist
<= 1;
                                                    end
                                                    //hole area
                                                else if( abs_y<15 &&
abs_x<hole[abs_y] )
                                                    begin
                                                        moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                    end
                                                else
                                                    begin
                                                        moleExist
<= 0;

mole_address <= 18'bZ ;
                                                    end
                                                    end
```

```
                                        endcase
                                            end
                                    //no mole
                                     else
                                       if(          abs_y<15          &&
abs_x<hole[abs_y] )
                                           begin
                                                   moleExist <= 1;
                                                   mole_address      <=
moleBase + 120*120;
                                            end
                                     else
                                           begin
                                                    moleExist <= 0;
                                                    mole_address     <=
18'bZ ;
                                            end

                                  end
                16'b0000000010000000: begin   x_offset <= Hsync_Blank + 200;
                                        y_offset <= Vertical_Back_Porch +320;
                                          //get the diff between the current x_cnt
and the left boundary of the hole
                                         bound_x <=    -x_cnt+x_offset+200-40;
                                          //get the diff between the current
y_cnt and the horizontal center of the hole
                                           if( y_cnt>120+y_offset)
                                              begin
                                                abs_y                       <=
      y_cnt-120-y_offset;
                                               end
                                    else
                                          begin
                                              abs_y                         <=
      -y_cnt+120+y_offset;
                                           end
                                    //get the diff between the current
x_cnt and the vertical center of the hole
                                    if(x_cnt>100+x_offset)
                                          begin
                                            abs_x                         <=
      x_cnt-100-x_offset;
                                           end
                                    else
                                          begin
                                              abs_x                       <=
      -x_cnt+100+x_offset;
                                           end


                                    //mole out of the hole
                                    if(moleHeight[7]>0)
                                           begin
                                               case(mole7)
                                                  2'b00:begin          //mole


                                                          //mole out
```

```
                                                    // inside mole area
                                                if (y_cnt < y_offset +
135 && y_cnt > y_offset + 135 - moleHeight[7]&& bound_x >
moleLeftBound[y_cnt-135-y_offset+moleHeight[7]]+1 &&bound_x <
moleRightBound[y_cnt-135-y_offset+moleHeight[7]]-1 )
                                                    begin
                                                        //update the
mole_address
                                                    mole_address <=
moleBase + (y_cnt-135-y_offset+moleHeight[7])*120 + x_cnt-x_offset-40;
                                                        moleExist
<= 1;
                                                    end
                                                    //hole area
                                                else if( abs_y<15 &&
abs_x<hole[abs_y] )
                                                    begin
                                                        moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                    end
                                                else
                                                    begin
                                                        moleExist
<= 0;

mole_address <= 18'bZ ;
                                                    end
                                                    end

                                                    2'b10:begin
//mole

                                                    //mole out
                                                    // inside mole area
                                                if (y_cnt < y_offset +
135 && y_cnt > y_offset + 135 - moleHeight[7]&& bound_x >
bottleLeftBound[y_cnt-135-y_offset+moleHeight[7]]+1 &&bound_x <
bottleRightBound[y_cnt-135-y_offset+moleHeight[7]]-1 )
                                                    begin
                                                        //update the
mole_address
                                                    mole_address <=
bottleOffset + moleBase + (y_cnt-135-y_offset+moleHeight[7])*120 + x_cnt-x_offset-40;
                                                        moleExist
<= 1;
                                                    end
                                                    //hole area
                                                else if( abs_y<15 &&
abs_x<hole[abs_y] )
                                                    begin
                                                        moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                    end
                                                else
```

```
                                                                    begin
                                                                        moleExist
<= 0;

mole_address <= 18'bZ ;
                                                                    end
                                                                    end

                                                                    2'b01:begin
//mole

                                                                     //mole out
                                                                     // inside mole area
                                                                  if  (y_cnt  <  y_offset  +
135  &&  y_cnt  >  y_offset  +  135  -  moleHeight[7]&&  bound_x  >
evilLeftBound[y_cnt-135-y_offset+moleHeight[7]]+1          &&bound_x          <
evilRightBound[y_cnt-135-y_offset+moleHeight[7]]-1   )
                                                                     begin
                                                                         //update  the
mole_address
                                                                        mole_address <=
evilOffset + moleBase + (y_cnt-135-y_offset+moleHeight[7])*120 + x_cnt-x_offset-40;
                                                                        moleExist
<= 1;
                                                                    end
                                                                     //hole area
                                                                 else  if(  abs_y<15  &&
abs_x<hole[abs_y] )
                                                                    begin
                                                                        moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                                    end
                                                                 else
                                                                    begin
                                                                        moleExist
<= 0;

mole_address <= 18'bZ ;
                                                                    end
                                                                    end




                                                               endcase
                                                                   end
                                                            //no mole
                                                              else
                                                                if(          abs_y<15          &&
abs_x<hole[abs_y] )
                                                                   begin
                                                                        moleExist <= 1;
                                                                        mole_address      <=
moleBase + 120*120;
                                                                    end
                                                              else
```

```
                                                    begin
                                                        moleExist <= 0;
                                                        mole_address      <=
18'bZ ;
                                                    end
                                                end
                    16'b0000000100000000: begin x_offset <= Hsync_Blank;
                                                y_offset <= Vertical_Back_Porch+320;
                                                //get the diff between the current x_cnt
and the left boundary of the hole
                                                bound_x <=    -x_cnt+x_offset+200-40;
                                                //get the diff between the current
y_cnt and the horizontal center of the hole
                                                if( y_cnt>120+y_offset)
                                                    begin
                                                        abs_y                    <=
    y_cnt-120-y_offset;
                                                    end
                                                else
                                                    begin
                                                        abs_y                    <=
    -y_cnt+120+y_offset;
                                                    end
                                                //get the diff between the current
x_cnt and the vertical center of the hole
                                                if(x_cnt>100+x_offset)
                                                    begin
                                                        abs_x                    <=
    x_cnt-100-x_offset;
                                                    end
                                                else
                                                    begin
                                                        abs_x                    <=
    -x_cnt+100+x_offset;
                                                    end


                                                //mole out of the hole
                                                if(moleHeight[8]>0)
                                                    begin
                                                        case(mole8)
                                                            2'b00:begin          //mole


                                                                //mole out
                                                                // inside mole area
                                                            if    (y_cnt    <    y_offset    +
135    &&    y_cnt    >    y_offset    +    135    -    moleHeight[8]&&    bound_x    >
moleLeftBound[y_cnt-135-y_offset+moleHeight[8]]+1          &&bound_x          <
moleRightBound[y_cnt-135-y_offset+moleHeight[8]]-1    )
                                                                begin
                                                                    //update the
mole_address
                                                                    mole_address <=
moleBase + (y_cnt-135-y_offset+moleHeight[8])*120 + x_cnt-x_offset-40;
                                                                    moleExist
<= 1;
                                                                end
```

```
                                                        //hole area
                                                    else if( abs_y<15 &&
abs_x<hole[abs_y] )
                                                        begin
                                                            moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                        end
                                                    else
                                                        begin
                                                            moleExist
<= 0;

mole_address <= 18'bZ ;
                                                        end
                                                    end

                                                    2'b10:begin     //mole


                                                        //mole out
                                                        // inside mole area
                                                    if (y_cnt < y_offset +
135 && y_cnt > y_offset + 135 - moleHeight[8]&& bound_x >
bottleLeftBound[y_cnt-135-y_offset+moleHeight[8]]+1 &&bound_x <
bottleRightBound[y_cnt-135-y_offset+moleHeight[8]]-1 )
                                                        begin
                                                            //update the
mole_address
                                                            mole_address <=
bottleOffset+ moleBase + (y_cnt-135-y_offset+moleHeight[8])*120 + x_cnt-x_offset-40;
                                                            moleExist
<= 1;
                                                        end
                                                        //hole area
                                                    else if( abs_y<15 &&
abs_x<hole[abs_y] )
                                                        begin
                                                            moleExist
<= 1;

mole_address <= moleBase + 120*120;
                                                        end
                                                    else
                                                        begin
                                                            moleExist
<= 0;

mole_address <= 18'bZ ;
                                                        end
                                                    end

                                                    2'b01:begin     //mole


                                                        //mole out
                                                        // inside mole area
```

```
                                                    if (y_cnt < y_offset + 135 && y_cnt > y_offset + 135 - moleHeight[8]&& bound_x > evilLeftBound[y_cnt-135-y_offset+moleHeight[8]]+1 &&bound_x < evilRightBound[y_cnt-135-y_offset+moleHeight[8]]-1 )
                                                        begin
                                                            //update the mole_address
                                                            mole_address <= evilOffset+ moleBase + (y_cnt-135-y_offset+moleHeight[8])*120 + x_cnt-x_offset-40;
                                                            moleExist <= 1;
                                                        end
                                                    //hole area
                                                    else if( abs_y<15 && abs_x<hole[abs_y] )
                                                        begin
                                                            moleExist <= 1;

mole_address <= moleBase + 120*120;
                                                        end
                                                    else
                                                        begin
                                                            moleExist <= 0;

mole_address <= 18'bZ ;
                                                        end
                                                end



                                            endcase
                                        end
                                    //no mole
                                    else
                                        if( abs_y<15 && abs_x<hole[abs_y] )
                                            begin
                                                moleExist <= 1;
                                                mole_address <= moleBase + 120*120;
                                            end
                                        else
                                            begin
                                                moleExist <= 0;
                                                mole_address <= 18'bZ ;
                                            end
                                    end
                16'b0000001000000000: begin moleExist <= 0;
                                                mole_address <= 18'bZ ;end
                16'b0000010000000000: begin moleExist <= 0;
                                                mole_address <= 18'bZ ;end
                16'b0000100000000000: begin moleExist <= 0;
```

```
                                                                    mole_address      <=
18'bZ ;end
                16'b0001000000000000: begin moleExist <= 0;
                                                                    mole_address      <=
18'bZ ;end
                16'b0010000000000000: begin moleExist <= 0;
                                                                    mole_address      <=
18'bZ ;end
                16'b0100000000000000: begin moleExist <= 0;
                                                                    mole_address      <=
18'bZ ;end
                16'b1000000000000000: begin moleExist <= 0;
                                                                    mole_address      <=
18'bZ ;end
                default: begin moleExist <= 0;
                                                                    mole_address      <=
18'bZ ;     end
            endcase
        end


endmodule
```

musiscontroller.vhd

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity musiccontroller is
port (

        clk             : in    std_logic;
        reset_n         : in    std_logic;
        read             : in    std_logic;
        write           : in    std_logic;
        chipselect : in    std_logic;
        address         : in    std_logic_vector(16 downto 0);
        readdata        : out std_logic_vector(15 downto 0);
        writedata     : in    std_logic_vector(15 downto 0);
        irq             : out std_logic;


        AUD_ADCLRCK    : out    std_logic;      --       Audio CODEC ADC LR Clock
        AUD_ADCDAT      : in      std_logic;      --       Audio CODEC ADC Data
        AUD_DACLRCK    : out    std_logic;      --       Audio CODEC DAC LR Clock
        AUD_DACDAT      : out    std_logic;      --       Audio CODEC DAC Data
        AUD_BCLK         : inout std_logic; --       Audio CODEC Bit-Stream Clock
        AUD_XCK          : out std_logic;
        clk_18            : in std_logic
    );

    end musiccontroller;

    architecture mc of musiccontroller is
```

```
   signal audio_request : std_logic;
   signal audio_clock : unsigned(1 downto 0) := "00";
   signal store : std_logic;
--    signal clk_18:std_logic;



     component de2_wm8731_audio is port(
                clk_chip : in std_logic;
                  clk : in std_logic;              --    Audio CODEC Chip Clock AUD_XCK (18.43 MHz)
                    reset_n : in std_logic;
                  test_mode : in std_logic;              --       Audio CODEC controller test mode
                  audio_request  :  out  std_logic_vector(15  downto  0);  --       Audio  controller
request new data
                  data             : in std_logic_vector(15 downto 0);
                    address        : in    std_logic_vector(16 downto 0);
                    write          : in std_logic;
                    chipselect : in std_logic;
              irq               : out std_logic;

                  -- Audio interface signals
                    AUD_ADCLRCK    : out    std_logic;      --       Audio CODEC ADC LR Clock
                  AUD_ADCDAT      : in      std_logic;      --       Audio CODEC ADC Data
                  AUD_DACLRCK    : out    std_logic;      --       Audio CODEC DAC LR Clock
                  AUD_DACDAT      : out    std_logic;      --       Audio CODEC DAC Data
                  AUD_BCLK         : inout std_logic--           Audio CODEC Bit-Stream Clock

              );
              end component de2_wm8731_audio;



              component de2_audio_pll is
PORT
(
inclk0             : IN STD_LOGIC    := '0';
c0          : OUT STD_LOGIC
);end component de2_audio_pll;



begin

  AUD_XCK <= clk_18;

process (clk)
   begin
     if rising_edge(clk) then
           audio_clock <= audio_clock + "1";
       end if;
end process;

--     process (clk)
--     begin
--           if rising_edge(clk) then
--                 if reset_n = '0' then
--                           store <= '0';
--                 else
```

```
--                          if chipSelect = '1' and write = '1'    then
--                                store <= '1';
--                          end if;
--                    end if;
--              end if;
--      end process;


V1: de2_wm8731_audio port map (
        clk_chip => clk,
        clk => clk_18,
        reset_n      => '1',
        test_mode => '0',
        audio_request => readdata,
        data =>    writedata ,
          address => address,
          write      => write,
          chipselect => chipselect,
          irq          =>    irq,

        -- Audio interface signals
        AUD_ADCLRCK    => AUD_ADCLRCK,
        AUD_ADCDAT      => AUD_ADCDAT,
        AUD_DACLRCK    => AUD_DACLRCK,
        AUD_DACDAT      => AUD_DACDAT,
        AUD_BCLK          => AUD_BCLK
    );


--    V2: de2_audio_pll port map(
--    inclk0 => clk_27,
--    c0          => clk_18
--    );
    end architecture;
```

No_GEN.v

```
//////////////////////Number Display Module//////////////////////////
module No_GEN(
                          iclk,
                          iReset_n,
                          ixcount,
                          iycount,
                          iled_pos_x,
                          iled_pos_y,
                          inumber,
                          oOVERRIDE,
                          oR,
                          oG,
                          oB
                          );

//Port IO
input iclk;
input iReset_n;
input [3:0]inumber;
```

```
input [10:0] ixcount;
input [9:0]    iycount;
input [10:0] iled_pos_x;
input [10:0] iled_pos_y;
output oOVERRIDE;
output [7:0] oR;
output [7:0] oG;
output [7:0] oB;

//Wire & Reg
reg [7:0]    oR;
reg [7:0]    oG;
reg [7:0]    oB;
reg oOVERRIDE;
wire display_area;
wire number_area;
wire a;
wire b;
wire c;
wire d;
wire e;
wire f;
wire g;
wire a_en;
wire b_en;
wire c_en;
wire d_en;
wire e_en;
wire f_en;
wire g_en;

//Structure
assign display_area = ((ixcount > (iled_pos_x -1))
                                        && (ixcount < (iled_pos_x+ 60) )
                                        && (iycount > (iled_pos_y -1))
                                        && (iycount < (iled_pos_y +80))) ? 1'b1:1'b0;

assign number_area = ((ixcount > (iled_pos_x +4))
                                        && (ixcount < (iled_pos_x+ 35) )
                                        && (iycount > (iled_pos_y + 9))
                                        && (iycount < (iled_pos_y +70))) ? 1'b1:1'b0;

assign a = ((ixcount > (iled_pos_x + 4))
                        && (ixcount < (iled_pos_x + 35))
                        &&(iycount > (iled_pos_y + 9))
                        &&(iycount < (iled_pos_y + 18))) ? 1'b1 : 1'b0;
assign b =        ((ixcount > (iled_pos_x + 4))
                        && (ixcount < (iled_pos_x + 13))
                        &&(iycount > (iled_pos_y + 9))
                        &&(iycount < (iled_pos_y + 40))) ? 1'b1 : 1'b0;
assign c =    ((ixcount > (iled_pos_x + 4))
                        && (ixcount < (iled_pos_x + 13))
                        &&(iycount > (iled_pos_y + 39))
                        &&(iycount < (iled_pos_y + 70))) ? 1'b1 : 1'b0;
assign d =          ((ixcount > (iled_pos_x + 4))
                        && (ixcount < (iled_pos_x + 35))
                        &&(iycount > (iled_pos_y + 61))
                        &&(iycount < (iled_pos_y + 70))) ? 1'b1 : 1'b0;
```

```
assign e =      ((ixcount > (iled_pos_x + 26))
                    && (ixcount < (iled_pos_x + 35))
                    &&(iycount > (iled_pos_y + 39))
                    &&(iycount < (iled_pos_y + 70))) ? 1'b1 : 1'b0;
assign f =      ((ixcount > (iled_pos_x + 26))
                    && (ixcount < (iled_pos_x + 35))
                    &&(iycount > (iled_pos_y + 9))
                    &&(iycount < (iled_pos_y + 40))) ? 1'b1 : 1'b0;
assign g =      ((ixcount > (iled_pos_x + 4))
                    && (ixcount < (iled_pos_x + 35))
                    &&(iycount > (iled_pos_y + 35))
                    &&(iycount < (iled_pos_y + 44))) ? 1'b1 : 1'b0;

//assign a_en = ((inumber != 1) && (inumber != 4)) ? 1'b1 : 1'b0;
//assign b_en = ((inumber != 5) && (inumber != 6)) ? 1'b1 : 1'b0;
//assign c_en = ((inumber != 2)) ? 1'b1 : 1'b0;
//assign d_en = ((inumber != 1) && (inumber != 4) && (inumber != 7)) ? 1'b1 : 1'b0;
//assign e_en = ((inumber == 2) || (inumber == 6) || (inumber == 8) || (inumber == 0)) ? 1'b1:
1'b0;
//assign f_en = ((inumber == 4) || (inumber == 5) || (inumber == 6) || (inumber == 8)
//                              || (inumber == 9) || (inumber == 0)) ? 1'b1: 1'b0;
//assign g_en = ((inumber != 1) && (inumber != 7) && (inumber != 0)) ? 1'b1 : 1'b0;

always @(posedge iclk or negedge iReset_n)
begin
    if(!iReset_n)
            oOVERRIDE <= 1'b0;
    else
    case(inumber)
        0: oOVERRIDE <= (a||b||c||d||e||f);
        1: oOVERRIDE <= (b||c);
        2: oOVERRIDE <= (a||b||g||e||d);
        3: oOVERRIDE <= (a||b||c||d||g);
        4: oOVERRIDE <= (b||c||f||g);
        5: oOVERRIDE <= (a||c||d||f||g);
        6: oOVERRIDE <= (a||c||d||e||f||g);
        7: oOVERRIDE <= (a||b||c);
        8: oOVERRIDE <= (a||b||c||d||e||f||g);
        9: oOVERRIDE <= (a||b||c||d||f||g);
        default : oOVERRIDE <= 1'b0;
    endcase
    oR <= 8'd255;
    oG <= 8'd255;
    oB <= 8'd255;
end
endmodule
```

number.v

```
//////////////////////Number Display Module//////////////////////////
module number(
                    iclk,
                    iReset_n,
                    ixcount,
                    iycount,
                    iled_pos_x,
```

```
                        iled_pos_y,
                        inumber,
                        oOVERRIDE,
                        );

//Port IO
input iclk;
input iReset_n;
input [3:0]inumber;
input [10:0] ixcount;
input [9:0]    iycount;
input [10:0] iled_pos_x;
input [10:0] iled_pos_y;
output oOVERRIDE;

//Wire & Reg
reg oOVERRIDE;
wire display_area;
wire number_area;
wire a;
wire b;
wire c;
wire d;
wire e;
wire f;
wire g;
wire a_en;
wire b_en;
wire c_en;
wire d_en;
wire e_en;
wire f_en;
wire g_en;

//Structure
assign display_area = ((ixcount > (iled_pos_x -1))
                                        && (ixcount < (iled_pos_x+ 60) )
                                        && (iycount > (iled_pos_y -1))
                                        && (iycount < (iled_pos_y +80))) ? 1'b1:1'b0;

assign number_area = ((ixcount > (iled_pos_x +4))
                                        && (ixcount < (iled_pos_x+ 35) )
                                        && (iycount > (iled_pos_y + 9))
                                        && (iycount < (iled_pos_y +70))) ? 1'b1:1'b0;

assign a = ((ixcount > (iled_pos_x + 4))
                        && (ixcount < (iled_pos_x + 35))
                        &&(iycount > (iled_pos_y + 9))
                        &&(iycount < (iled_pos_y + 18))) ? 1'b1 : 1'b0;
assign b =        ((ixcount > (iled_pos_x + 4))
                        && (ixcount < (iled_pos_x + 13))
                        &&(iycount > (iled_pos_y + 9))
                        &&(iycount < (iled_pos_y + 40))) ? 1'b1 : 1'b0;
assign c =    ((ixcount > (iled_pos_x + 4))
                        && (ixcount < (iled_pos_x + 13))
                        &&(iycount > (iled_pos_y + 39))
                        &&(iycount < (iled_pos_y + 70))) ? 1'b1 : 1'b0;
assign d =          ((ixcount > (iled_pos_x + 4))
```

```
                    && (ixcount < (iled_pos_x + 35))
                    &&(iycount > (iled_pos_y + 61))
                    &&(iycount < (iled_pos_y + 70))) ? 1'b1 : 1'b0;
assign e =      ((ixcount > (iled_pos_x + 26))
                    && (ixcount < (iled_pos_x + 35))
                    &&(iycount > (iled_pos_y + 39))
                    &&(iycount < (iled_pos_y + 70))) ? 1'b1 : 1'b0;
assign f =      ((ixcount > (iled_pos_x + 26))
                    && (ixcount < (iled_pos_x + 35))
                    &&(iycount > (iled_pos_y + 9))
                    &&(iycount < (iled_pos_y + 40))) ? 1'b1 : 1'b0;
assign g =      ((ixcount > (iled_pos_x + 4))
                    && (ixcount < (iled_pos_x + 35))
                    &&(iycount > (iled_pos_y + 35))
                    &&(iycount < (iled_pos_y + 44))) ? 1'b1 : 1'b0;

//assign a_en = ((inumber != 1) && (inumber != 4)) ? 1'b1 : 1'b0;
//assign b_en = ((inumber != 5) && (inumber != 6)) ? 1'b1 : 1'b0;
//assign c_en = ((inumber != 2)) ? 1'b1 : 1'b0;
//assign d_en = ((inumber != 1) && (inumber != 4) && (inumber != 7)) ? 1'b1 : 1'b0;
//assign e_en = ((inumber == 2) || (inumber == 6) || (inumber == 8) || (inumber == 0)) ? 1'b1:
1'b0;
//assign f_en = ((inumber == 4) || (inumber == 5) || (inumber == 6) || (inumber == 8)
//                    || (inumber == 9) || (inumber == 0)) ? 1'b1: 1'b0;
//assign g_en = ((inumber != 1) && (inumber != 7) && (inumber != 0)) ? 1'b1 : 1'b0;

always @(posedge iclk or negedge iReset_n)
begin
    if(!iReset_n)
        oOVERRIDE <= 1'b0;
    else
    case(inumber)
        0: oOVERRIDE <= (a||b||c||d||e||f);
        1: oOVERRIDE <= (b||c);
        2: oOVERRIDE <= (a||b||g||e||d);
        3: oOVERRIDE <= (a||b||c||d||g);
        4: oOVERRIDE <= (b||c||f||g);
        5: oOVERRIDE <= (a||c||d||f||g);
        6: oOVERRIDE <= (a||c||d||e||f||g);
        7: oOVERRIDE <= (a||b||c);
        8: oOVERRIDE <= (a||b||c||d||e||f||g);
        9: oOVERRIDE <= (a||b||c||d||f||g);
        default : oOVERRIDE <= 1'b0;
    endcase
end
endmodule
```

panel_control.v

```
module panel_ctrl(
                    clk_ltm,
                    reset_n, //top level connection
                    x_cnt, // input from lcd controlelr
                    y_cnt, // input from lcd controller
                    iPANELCTRL, // command from nios containing 32 bits
                    oOVERRIDE,//override output to the lcd_controller
```

```
                        oADDR, //the output address to the lcd controller
                        //ostate
                        );
//===============
//PARAMETER
//==================
parameter BASE_ADDR = 89024;
parameter H_LINE = 1056;
parameter V_LINE = 525;
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
parameter Vertical_Front_Porch = 10;
//=================================
//IO PORT
//=================================
input clk_ltm;
input reset_n;
input [10:0] x_cnt;
input [9:0] y_cnt;
input [31:0] iPANELCTRL;
output oOVERRIDE;
output [17:0] oADDR;
//output [3:0] ostate;
//=================================
//REG and WIRE
//=================================
wire oOVERRIDE;
wire [17:0] oADDR; // output address to lcd controller
wire [15:0] area; // 15 areas in total
wire [17:0] iADDR [0:5]; // address from the 6 peripheral areas
wire [5:0] override; //6 bit override signal from 6 area
wire [3:0] life;
wire [3:0] score0;
wire [3:0] score1;
wire [3:0] score2;
wire [3:0] state; // init->start-> pause

assign          state = iPANELCTRL[3:0];
assign          life =    iPANELCTRL[7:4];
assign          score0 = iPANELCTRL[11:8];
assign          score1 = iPANELCTRL[15:12];
assign          score2 = iPANELCTRL[19:16];
assign          ostate = state;

Timmer Timmer1(
                .clk_ltm(clk_ltm),
                .reset_n(reset_n),
                .x_cnt(x_cnt),
                .y_cnt(y_cnt),
                .state(state),
                .oOVERRIDE(override[0]),
                .oADDR(iADDR[0])
                );

Life Life1(
                .clk_ltm(clk_ltm),
                .reset_n(reset_n),
```

```
                .x_cnt(x_cnt),
                .y_cnt(y_cnt),
                .life(life),
                .oOVERRIDE(override[1]),
                .oADDR(iADDR[1])
                );

Score Score1(
                .clk_ltm(clk_ltm),
                .reset_n(reset_n),
                .x_cnt(x_cnt),
                .y_cnt(y_cnt),
                .iScore0(score0),
                .iScore1(score1),
                .iScore2(score2),
                .oOVERRIDE(override[2]),
                .oADDR(iADDR[2])
                );

quit quit1 (
                .iclk(clk_ltm),
                .ireset_n(reset_n),
                .ix_cnt(x_cnt),
                .iy_cnt(y_cnt),
                .oOVERRIDE(override[5]),
                .oADDR(iADDR[5]));

start start1 (
                .iclk(clk_ltm),
                .ireset_n(reset_n),
                .ix_cnt(x_cnt),
                .iy_cnt(y_cnt),
                .oOVERRIDE(override[3]),
                .oADDR(iADDR[3])
                );

pause pause1 (
                .iclk(clk_ltm),
                .ireset_n(reset_n),
                .ix_cnt(x_cnt),
                .iy_cnt(y_cnt),
                .oOVERRIDE(override[4]),
                .oADDR(iADDR[4])
                );



//Detect which area you are in// 0~14 different areas//offset corrected
assign area[0] = ((x_cnt>(Hsync_Blank-2+400)&& //>214
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-200))&& //< 1015
                                (y_cnt>(Vertical_Back_Porch-1))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                                ))    ? 1'b1 : 1'b0 ; //mole0
assign area[1] = ((x_cnt>(Hsync_Blank-2+200)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-400))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                                ))    ? 1'b1 : 1'b0;//mole1
```

```
assign area[2] = ((x_cnt>(Hsync_Blank-2)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-600))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                                ))    ? 1'b1 : 1'b0 ;//mole2
assign area[3] = ((x_cnt>(Hsync_Blank-2+400)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-200))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                                ))    ? 1'b1 : 1'b0 ;    //mole3
assign area[4] = ((x_cnt>(Hsync_Blank-2+200)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-400))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                                ))    ? 1'b1 : 1'b0 ; //mole4
assign area[5] = ((x_cnt>(Hsync_Blank-2)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-600))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                                ))    ? 1'b1 : 1'b0 ;//mole5
assign area[6] = ((x_cnt>(Hsync_Blank-2+400)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-200))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0 ;    //mole6
assign area[7] = ((x_cnt>(Hsync_Blank-2+200)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-400))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0; //mole7
assign area[8] = ((x_cnt>(Hsync_Blank-2)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-600))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0 ;//mole8
assign area[9] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-400))
                                ))    ? 1'b1 : 1'b0 ;//area 9 Time
assign area[10] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+80))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                                ))    ? 1'b1 : 1'b0 ;//area 10 life
assign area[11] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-240))
                                ))    ? 1'b1 : 1'b0 ;//area 11 score
assign area[12] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+240))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                                ))    ? 1'b1 : 1'b0 ;//area 12 start/pause
assign area[13] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
```

```
                                (y_cnt<(V_LINE - Vertical_Front_Porch-80))
                                ))    ? 1'b1 : 1'b0 ;//area 13 exit
assign area[14] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+400))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0 ;//area 14 label


assign oOVERRIDE = override[0] || override[1] || override[2] || override[3] || override[4] ||
override[5];
assign oADDR = (area[9] && override[0]) ? iADDR [0] :
                                (area[10] && override[1]) ? iADDR [1] :
                                (area[11] && override[2]) ? iADDR [2] :
                                (area[12] && override[3]) ? iADDR [3] :
                                (area[13] && override[4]) ? iADDR [4] :
                                (area[14] && override[5]) ? iADDR [5] : BASE_ADDR;
endmodule
```

pause.v

```
module pause(
                iclk,
                ireset_n,
                ix_cnt,
                iy_cnt,
                oOVERRIDE,
                oADDR
                        );

//================================================
//I/O DECALARATION==============================
//================================================
input iclk;
input ireset_n;
input [10:0] ix_cnt;
input [9:0] iy_cnt;
output oOVERRIDE;
output [17:0] oADDR;

//================================================
//WIRE & REG====================================
//================================================
wire [10:0]iletter_pos_x;
wire [9:0] iletter_pos_y;
wire iletter;
wire [4:0]override;
wire [17:0] address [0:4];

//================================================
//PARAMETER=====================================
//================================================
parameter A = 5'd1;
parameter B = 5'd2;
parameter C = 5'd3;
parameter D = 5'd4;
```

```
parameter E = 5'd5;
parameter F = 5'd6;
parameter G = 5'd7;
parameter H = 5'd8;
parameter I = 5'd9;
parameter J = 5'd10;
parameter K = 5'd11;
parameter L = 5'd12;
parameter M = 5'd13;
parameter N = 5'd14;
parameter O = 5'd15;
parameter P = 5'd16;
parameter Q = 5'd17;
parameter R = 5'd18;
parameter S = 5'd19;
parameter T = 5'd20;
parameter U = 5'd21;
parameter V = 5'd22;
parameter W = 5'd23;
parameter X = 5'd24;
parameter Y = 5'd25;
parameter Z = 5'd26;
parameter H_LINE = 1056;
parameter V_LINE = 525;
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
parameter Vertical_Front_Porch = 10;
//=============================================
//Structured logci==============================
//=============================================

letter letter0(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(Hsync_Blank-2+620),
                        .iletter_pos_y(Vertical_Back_Porch-1+344),
                        .iletter(E),
                        .oOVERRIDE(override[0]),
                        .oADDR(address[0]));

letter letter1(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(Hsync_Blank-2+652),
                        .iletter_pos_y(Vertical_Back_Porch-1+344),
                        .iletter(S),
                        .oOVERRIDE(override[1]),
                        .oADDR(address[1]));

letter letter2(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
```

```
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(Hsync_Blank-2+684),
                        .iletter_pos_y(Vertical_Back_Porch-1+344),
                        .iletter(U),
                        .oOVERRIDE(override[2]),
                        .oADDR(address[2]));

letter letter3(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(Hsync_Blank-2+716),
                        .iletter_pos_y(Vertical_Back_Porch-1+344),
                        .iletter(A),
                        .oOVERRIDE(override[3]),
                        .oADDR(address[3]));

letter letter4(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(Hsync_Blank-2+748),
                        .iletter_pos_y(Vertical_Back_Porch-1+344),
                        .iletter(P),
                        .oOVERRIDE(override[4]),
                        .oADDR(address[4]));

assign oOVERRIDE = (override[0] || override[1] || override [2] || override[3]|| override[4]);
assign oADDR = override[0] ? address[0] :
                                override[1] ? address[1] :
                                override[2] ? address[2] :
                                override[3] ? address[3] :
                                override[4] ? address[4] : 18'bZ;
endmodule
```

play.v

```
module play(
                        iclk,
                        ireset_n,
                        ix_cnt, // input from lcd controlelr
                        iy_cnt, // input from lcd controller
                        iPANELCTRL, // command from nios containing 32 bits
                        iMOLECTRL,
                        oADDR, //the output address to the lcd controller
                                );
//=============================================================================
// PARAMETER declarations
//=============================================================================
parameter H_LINE = 1056;
parameter V_LINE = 525;
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
```

```
parameter Vertical_Front_Porch = 10;
parameter offset = 32000; //control panel image address offset

//=============================================
//I/O DECALARATION=============================
//=============================================
input iclk;
input ireset_n;
input [10:0] ix_cnt;
input [9:0] iy_cnt;
input [31:0] iPANELCTRL;
input [31:0] iMOLECTRL;
output [17:0] oADDR;

//=============================================
//WIRE & REG=============================
//=============================================
wire [1:0] override;
wire [17:0] MOLE_ADDR;
wire [17:0] PANEL_ADDR;
reg [17:0] BACK_ADDR;
wire [15:0] area;
wire [10:0] x_cnt;
wire [9:0] y_cnt;
reg [15:0] area_counter[0:15];
wire state = iPANELCTRL[3:0];

assign oADDR = (override[1]) ? MOLE_ADDR : (override[0]) ? PANEL_ADDR : BACK_ADDR;
assign x_cnt = ix_cnt;
assign y_cnt = iy_cnt;

mole_ctrl mole_ctrl1(
                        .iCLK(iclk),                    // LCD display clock
                        .iRST_n(ireset_n),              // systen reset
                       .x_cnt(x_cnt),
                  .y_cnt(y_cnt),
                        .moleControl(iMOLECTRL),
                        .moleExist(override[1]),
                        .mole_address(MOLE_ADDR),
                        );

panel_ctrl panel_ctrl1(
                      .clk_ltm(iclk),
                      .reset_n(ireset_n), //top level connection
                      .x_cnt(x_cnt), // input from lcd controlelr
                      .y_cnt(y_cnt), // input from lcd controller
                      .iPANELCTRL(iPANELCTRL), // command from nios containing 32 bits
                      .oOVERRIDE(override[0]),//override output to the lcd_controller
                      .oADDR(PANEL_ADDR) //the output address to the lcd controller
                      );

//Detect which area you are in// 0~14 different areas//offset corrected
assign area[0] = ((x_cnt>(Hsync_Blank-2+400)&& //>214
                        (x_cnt<(H_LINE-Hsync_Front_Porch-1-200))&& //< 1015
                        (y_cnt>(Vertical_Back_Porch-1))&&
                        (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                        ))    ? 1'b1 : 1'b0 ; //mole0
assign area[1] = ((x_cnt>(Hsync_Blank-2+200)&& //>215
```

```
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-400))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                                ))    ? 1'b1 : 1'b0;//mole1
assign area[2] = ((x_cnt>(Hsync_Blank-2)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-600))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                                ))    ? 1'b1 : 1'b0 ;//mole2
assign area[3] = ((x_cnt>(Hsync_Blank-2+400)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-200))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                                ))    ? 1'b1 : 1'b0 ;    //mole3
assign area[4] = ((x_cnt>(Hsync_Blank-2+200)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-400))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                                ))    ? 1'b1 : 1'b0 ; //mole4
assign area[5] = ((x_cnt>(Hsync_Blank-2)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-600))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
                                ))    ? 1'b1 : 1'b0 ;//mole5
assign area[6] = ((x_cnt>(Hsync_Blank-2+400)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-200))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0 ;    //mole6
assign area[7] = ((x_cnt>(Hsync_Blank-2+200)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-400))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0; //mole7
assign area[8] = ((x_cnt>(Hsync_Blank-2)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1-600))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0 ;//mole8
assign area[9] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-400))
                                ))    ? 1'b1 : 1'b0 ;//area 9 Time
assign area[10] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+80))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-320))
                                ))    ? 1'b1 : 1'b0 ;//area 10 life
assign area[11] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+160))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-240))
                                ))    ? 1'b1 : 1'b0 ;//area 11 score
assign area[12] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+240))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-160))
```

```
                                ))    ? 1'b1 : 1'b0 ;//area 12 start/pause
assign area[13] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+320))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch-80))
                                ))    ? 1'b1 : 1'b0 ;//area 13 exit
assign area[14] = ((x_cnt>(Hsync_Blank-2+600)&& //>215
                                (x_cnt<(H_LINE-Hsync_Front_Porch-1))&& //< 1016
                                (y_cnt>(Vertical_Back_Porch-1+400))&&
                                (y_cnt<(V_LINE - Vertical_Front_Porch))
                                ))    ? 1'b1 : 1'b0 ;//area 14 label


always@(posedge iclk or negedge ireset_n)
begin
      if(!ireset_n)
            BACK_ADDR <= 18'bZ;
      else
         BACK_ADDR <=                area[0] ? area_counter[0] :
                                             area[1] ? area_counter[1] :
                                             area[2] ? area_counter[2] :
                                             area[3] ? area_counter[3] :
                                             area[4] ? area_counter[4] :
                                             area[5] ? area_counter[5] :
                                             area[6] ? area_counter[6] :
                                             area[7] ? area_counter[7] :
                                             area[8] ? area_counter[8] :
                                             area[9] ? (area_counter[9] + offset):
                                             area[10] ? (area_counter[10] + offset):
                                             area[11] ? (area_counter[11] + offset):
                                             area[12] ? (area_counter[12] + offset):
                                             area[13] ? (area_counter[13] + offset):
                                             area[14] ? (area_counter[14] + offset): 18'bZ;
end

always@(posedge iclk or negedge ireset_n)
      begin
      if (!ireset_n)
            begin
            area_counter[0] <= 0;
            area_counter[1] <= 0;
            area_counter[2] <= 0;
            area_counter[3] <= 0;
            area_counter[4] <= 0;
            area_counter[5] <= 0;
            area_counter[6] <= 0;
            area_counter[7] <= 0;
            area_counter[8] <= 0;
            area_counter[9] <= 0;
            area_counter[10] <= 0;
            area_counter[11] <= 0;
            area_counter[12] <= 0;
            area_counter[13] <= 0;
            area_counter[14] <= 0;
            end
      else
            case(area)
                  16'b0000000000000001:
```

```
begin
if(area_counter[0] == 15'd31999)
	area_counter[0] <= 0;
else
	area_counter[0] <= area_counter[0] +1;
end//area 0

16'b0000000000000010:
begin
if(area_counter[1] == 15'd31999)
	area_counter[1] <= 0;
else
	area_counter[1] <= area_counter[1] +1;
end//area 1

16'b0000000000000100:
begin
if(area_counter[2] == 15'd31999)
	area_counter[2] <= 0;
else
	area_counter[2] <= area_counter[2] +1;
end//area 2

16'b0000000000001000:
begin
if(area_counter[3] == 15'd31999)
	area_counter[3] <= 0;
else
	area_counter[3] <= area_counter[3] +1;
end//area 3

16'b0000000000010000:
begin
if(area_counter[4] == 15'd31999)
	area_counter[4] <= 0;
else
	area_counter[4] <= area_counter[4] +1;
end//area 4

16'b0000000000100000:
begin
if(area_counter[5] == 15'd31999)
	area_counter[5] <= 0;
else
	area_counter[5] <= area_counter[5] +1;
end//area 5

16'b0000000001000000:
begin
if(area_counter[6] == 15'd31999)
	area_counter[6] <= 0;
else
	area_counter[6] <= area_counter[6] +1;
end//area 6

16'b0000000010000000:
begin
if(area_counter[7] == 15'd31999)
```

```
        area_counter[7] <= 0;
else
        area_counter[7] <= area_counter[7] +1;
end//area 7

16'b0000000100000000:
begin
if(area_counter[8] == 15'd31999)
        area_counter[8] <= 0;
else
        area_counter[8] <= area_counter[8] +1;
end//area 8

16'b0000001000000000:
begin
if(area_counter[9] == 15'd15999)
        area_counter[9] <= 0;
else
        area_counter[9] <= area_counter[9] +1;
end//area 9

16'b0000010000000000:
        begin
if(area_counter[10] == 15'd15999)
        area_counter[10] <= 0;
else
        area_counter[10] <= area_counter[10] +1;
end//area 10

16'b0000100000000000:
begin
if(area_counter[11] == 15'd15999)
        area_counter[11] <= 0;
else
        area_counter[11] <= area_counter[11] +1;
end//area 11

16'b0001000000000000:
begin
if(area_counter[12] == 15'd15999)
        area_counter[12] <= 0;
else
        area_counter[12] <= area_counter[12] +1;
end//area 12

16'b0010000000000000:
begin
if(area_counter[13] == 15'd15999)
        area_counter[13] <= 0;
else
        area_counter[13] <= area_counter[13] +1;
end//area 13

16'b0100000000000000:
begin
if(area_counter[14] == 15'd15999)
        area_counter[14] <= 0;
else
```

```
                    area_counter[14] <= area_counter[14] +1;
                end//area 14

                //default: begin red_1 <= 8'd255;green_1 <= 8'd255;blue_1 <= 8'd255;     end
            endcase
        end
endmodule
```

quit.v

```
module quit(
                iclk,
                ireset_n,
                ix_cnt,
                iy_cnt,
                oOVERRIDE,
                oADDR);

//================================================
//I/O DECALARATION================================
//================================================
input iclk;
input ireset_n;
input [10:0] ix_cnt;
input [9:0] iy_cnt;
output oOVERRIDE;
output [17:0] oADDR;

//================================================
//WIRE & REG======================================
//================================================
wire [10:0]iletter_pos_x;
wire [9:0] iletter_pos_y;
wire iletter;
wire [3:0]override;
wire [17:0] address [0:3];

//================================================
//PARAMETER=======================================
//================================================
parameter A = 5'd1;
parameter B = 5'd2;
parameter C = 5'd3;
parameter D = 5'd4;
parameter E = 5'd5;
parameter F = 5'd6;
parameter G = 5'd7;
parameter H = 5'd8;
parameter I = 5'd9;
parameter J = 5'd10;
parameter K = 5'd11;
parameter L = 5'd12;
parameter M = 5'd13;
parameter N = 5'd14;
parameter O = 5'd15;
parameter P = 5'd16;
```

```
parameter Q = 5'd17;
parameter R = 5'd18;
parameter S = 5'd19;
parameter T = 5'd20;
parameter U = 5'd21;
parameter V = 5'd22;
parameter W = 5'd23;
parameter X = 5'd24;
parameter Y = 5'd25;
parameter Z = 5'd26;
parameter H_LINE = 1056;
parameter V_LINE = 525;
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
parameter Vertical_Front_Porch = 10;
//=============================================
//Structured logci==============================
//=============================================

letter letter0(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(Hsync_Blank-2+636),
                        .iletter_pos_y(Vertical_Back_Porch-1+424),
                        .iletter(T),
                        .oOVERRIDE(override[0]),
                        .oADDR(address[0]));

letter letter1(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(Hsync_Blank-2+668),
                        .iletter_pos_y(Vertical_Back_Porch-1+424),
                        .iletter(I),
                        .oOVERRIDE(override[1]),
                        .oADDR(address[1]));

letter letter2(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(Hsync_Blank-2+700),
                        .iletter_pos_y(Vertical_Back_Porch-1+424),
                        .iletter(U),
                        .oOVERRIDE(override[2]),
                        .oADDR(address[2]));

letter letter3(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
```

```
                    .iletter_pos_x(Hsync_Blank-2+732),
                    .iletter_pos_y(Vertical_Back_Porch-1+424),
                    .iletter(Q),
                    .oOVERRIDE(override[3]),
                    .oADDR(address[3]));

assign oOVERRIDE = (override[0] || override[1] || override [2] || override[3]);
assign oADDR = override[0] ? address[0] :
                            override[1] ? address[1] :
                            override[2] ? address[2] :
                            override[3] ? address[3] : 18'bZ;
endmodule
```

score.v

```
module Score(
            clk_ltm,
            reset_n,
            x_cnt,
            y_cnt,
            iScore0,
            iScore1,
            iScore2,
            oOVERRIDE,
            oADDR
            );

input clk_ltm;
input reset_n;
input [10:0] x_cnt;
input [9:0] y_cnt;
input [4:0] iScore0;
input [4:0] iScore1;
input [4:0] iScore2;
output oOVERRIDE;
output [17:0] oADDR;
//PARAMETER
parameter BASE_ADDR = 89025;
parameter INIT = 2'b00;
parameter START = 2'b01;
parameter PAUSE = 2'b10;
parameter H_LINE = 1056;
parameter V_LINE = 525;
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
parameter Vertical_Front_Porch = 10;
parameter coin_base = 18'd96239;
//WIRE & REG

wire [3:0] OVERRIDE;
wire [4:0] score[0:2];
wire [17:0] address;
assign score[0] = iScore0;
assign score[1] = iScore1;
assign score[2] = iScore2;
```

```
symbol coin(
                        .iclk(clk_ltm),
                        .ireset_n(reset_n),
                        .ix_cnt(x_cnt),
                        .iy_cnt(y_cnt),
                        .isymbol_pos_x(Hsync_Blank-1+730),
                        .isymbol_pos_y(Vertical_Back_Porch+170),
                        .iBASE_ADDR(coin_base),
                        .oOVERRIDE(OVERRIDE[3]),
                        .oADDR(address)
);

number score0(
                        .iclk(clk_ltm),
                        .iReset_n(reset_n),
                        .ixcount(x_cnt),
                        .iycount(y_cnt),
                        .iled_pos_x(Hsync_Blank-1+600),
                        .iled_pos_y(Vertical_Back_Porch+160),
                        .inumber(score[0]),
                        .oOVERRIDE(OVERRIDE[0])
);

number score1(
                        .iclk(clk_ltm),
                        .iReset_n(reset_n),
                        .ixcount(x_cnt),
                        .iycount(y_cnt),
                        .iled_pos_x(Hsync_Blank-1+640),
                        .iled_pos_y(Vertical_Back_Porch+160),
                        .inumber(score[1]),
                        .oOVERRIDE(OVERRIDE[1])
);

number score2(
                        .iclk(clk_ltm),
                        .iReset_n(reset_n),
                        .ixcount(x_cnt),
                        .iycount(y_cnt),
                        .iled_pos_x(Hsync_Blank-1+680),
                        .iled_pos_y(Vertical_Back_Porch+160),
                        .inumber(score[2]),
                        .oOVERRIDE(OVERRIDE[2])
);
////OUTPUT
assign oOVERRIDE = OVERRIDE[0] || OVERRIDE [1] || OVERRIDE[2] || OVERRIDE[3];
assign oADDR = (OVERRIDE[0] || OVERRIDE [1] || OVERRIDE[2]) ? BASE_ADDR :
                                OVERRIDE[3] ? address : 18'bZ;

endmodule
```

reset_delay.v

```
module    Reset_Delay(iCLK,iRST,oRST_0,oRST_1,oRST_2);

input             iCLK;
```

```
input           iRST;
output reg      oRST_0;
output reg      oRST_1;
output reg      oRST_2;

reg  [21:0]     Cont;

always@(posedge iCLK or negedge iRST)
begin
    if(!iRST)
    begin
        Cont<=  0;
        oRST_0  <=  0;
        oRST_1  <=  0;
        oRST_2  <=  0;
    end
    else
    begin
        if(Cont!=22'h3FFFFF)
        Cont<=  Cont+1;
        if(Cont>=22'h1FFFFF)
        oRST_0  <=  1;
        if(Cont>=22'h2FFFFF)
        oRST_1  <=  1;
        if(Cont>=22'h3FFFFF)
        oRST_2  <=  1;
    end
end
```

```
endmodule
```

SEG7_LUT_8.v

```
//>>
module SEG7_LUT_8 (
	output	[6:0]oSEG0,
	output	[6:0]oSEG1,
	output	[6:0]oSEG2,
	output	[6:0]oSEG3,
	output	[6:0]oSEG4,
	output	[6:0]oSEG5,
	output	[6:0]oSEG6,
	output	[6:0]oSEG7,
	input	[31:0]iDIG,
	input	[7:0]ON_OFF
  );
//7-Seg 0//
	SEG7_LUT u0(
		.iDIG	(iDIG[3:0]),
		.oSEG	(oSEG0),
		.ON_OFF(ON_OFF[0])
	  );
//7-Seg 1//
	SEG7_LUT u1(
		.iDIG	(iDIG[7:4]),
		.oSEG	(oSEG1),
		.ON_OFF(ON_OFF[1])
	  );
//7-Seg 2//
```

```
	SEG7_LUT u2(
		.iDIG	(iDIG[11:8]),
		.oSEG	(oSEG2),
		.ON_OFF(ON_OFF[2])
	 );
//7-Seg 3//
	SEG7_LUT u3(
		.iDIG	(iDIG[15:12]),
		.oSEG	(oSEG3),
		.ON_OFF(ON_OFF[3])
	 );
//7-Seg 4//
	SEG7_LUT u4(
		.iDIG	(iDIG[19:16]),
		.oSEG	(oSEG4),
		.ON_OFF(ON_OFF[4])
	 );
//7-Seg 5//
	SEG7_LUT u5(
		.iDIG	(iDIG[23:20]),
		.oSEG	(oSEG5),
		.ON_OFF(ON_OFF[5])
	 );
//7-Seg 6//
	SEG7_LUT u6(
		.iDIG	(iDIG[27:24]),
		.oSEG	(oSEG6),
		.ON_OFF(ON_OFF[6])
	 );
```

```
//7-Seg 7//
	SEG7_LUT u7(
		.iDIG	(iDIG[31:28]),
		.oSEG	(oSEG7),
		.ON_OFF(ON_OFF[7])
	 );
endmodule
```

SEG_LUT.v

```
module SEG7_LUT	(
	input		[3:0]iDIG,
	output	reg [6:0]oSEG,
	input			ON_OFF
);

	always @({iDIG,ON_OFF})begin
		if (!ON_OFF)
			oSEG=7'b1111111;
		else begin
		case(iDIG)
		4'h1: oSEG = 7'b1111001;	// ---t----
		4'h2: oSEG = 7'b0100100;	// |	|
		4'h3: oSEG = 7'b0110000;	// lt	rt
		4'h4: oSEG = 7'b0011001;	// |	|
		4'h5: oSEG = 7'b0010010;	// ---m----
		4'h6: oSEG = 7'b0000010;	// |	|
		4'h7: oSEG = 7'b1111000;	// lb	rb
		4'h8: oSEG = 7'b0000000;	// |	|
		4'h9: oSEG = 7'b0011000;	// ---b----
```

```
            4'ha: oSEG = 7'b0001000;

            4'hb: oSEG = 7'b0000011;

            4'hc: oSEG = 7'b1000110;

            4'hd: oSEG = 7'b0100001;

            4'he: oSEG = 7'b0000110;

            4'hf: oSEG = 7'b0001110;

            4'h0: oSEG = 7'b1000000;

            endcase

            end

      end


endmodule
```

single_clk_irq.v

```
module single_clk_irq(
                        clk,
                        reset_n,
                        idisplay_mode,
                        irq
);

input clk;
input reset_n;
input idisplay_mode;
output irq;

reg irq;
reg [4:0]flag;

always@(posedge clk or negedge reset_n)
begin
        if (!reset_n)
            begin
                irq <= 0;
                flag <= 5'b0;
            end
        else  if(idisplay_mode == 0)
            begin
                irq <= 0;
                flag <= 5'b0;
            end
        else if(idisplay_mode == 1 && flag < 16)
            begin
```

```
                        irq <= 1;
                        flag <= flag +1;
                end
        else
                        irq <= 0;
end

endmodule
```

sram_mux.v

```
//library ieee;
//use ieee.std_logic_1164.all;
module sram_mux(
//              chipselect,
                write,
                read,
                address,
                writedata,
                readdata,
//              byteenable,
                SRAM_DQ,
                SRAM_ADDR,
                SRAM_UB_N,
                SRAM_LB_N,
                SRAM_WE_N,
                SRAM_CE_N,
                SRAM_OE_N,
                VGA_DQ,
                VGA_ADDR,
//              VGA_UB_N,
//              VGA_LB_N,
                VGA_WE_N,
//              VGA_CE_N,
                VGA_OE_N
                );

//input chipselect;
input write;
input read;
input [17:0] address;
input [15:0] writedata;
output [15:0] readdata;
//input [1:0] byteenable;
inout [15:0] SRAM_DQ;
output [17:0] SRAM_ADDR;
output SRAM_UB_N;
output SRAM_LB_N;
output SRAM_WE_N;
output SRAM_CE_N;
output SRAM_OE_N;
output [15:0] VGA_DQ;
input [17:0] VGA_ADDR;
//input VGA_UB_N;
//input VGA_LB_N;
input VGA_WE_N;
```

```
//input VGA_CE_N;
input VGA_OE_N;


assign	SRAM_DQ = (write || read) ? writedata : 16'bZ;
assign	readdata = SRAM_DQ;
assign	VGA_DQ = SRAM_DQ;
assign	SRAM_ADDR = (write || read) ? address : VGA_ADDR;
assign	SRAM_UB_N = 0;
assign	SRAM_LB_N = 0;
assign	SRAM_WE_N = (write || read) ? !write : !VGA_WE_N;
assign	SRAM_CE_N = 0;
assign	SRAM_OE_N = (write || read) ? !read : !VGA_OE_N;

endmodule
```

sram.v

```
// sram.v

// Generated using ACDS version 12.1 177 at 2013.03.31.17:14:42

`timescale 1 ps / 1 ps
module sram (
		input	wire		chipselect, // avalon_slave_0.chipselect
		input	wire		write,		//			.write
		input	wire		read,		//			.read
		input	wire [17:0] address,	//			.address
		output wire [15:0] readdata,	//			.readdata
		input	wire [15:0] writedata,	//			.writedata
		input	wire [1:0]	byteenable, //			.byteenable
		inout	wire [15:0] SRAM_DQ,	//	conduit_end.export
		output wire [17:0] SRAM_ADDR,	//			.export
		output wire		SRAM_UB_N,	//			.export
		output wire		SRAM_LB_N,	//			.export
		output wire		SRAM_WE_N,	//			.export
		output wire		SRAM_CE_N,	//			.export
		output wire		SRAM_OE_N	//			.export
	);

	de2_sram_controller sram_inst (
		.chipselect (chipselect), // avalon_slave_0.chipselect
		.write		(write),	//			.write
		.read		(read),		//			.read
		.address	(address),	//			.address
		.readdata	(readdata),	//			.readdata
		.writedata	(writedata),	//			.writedata
		.byteenable (byteenable), //			.byteenable
		.SRAM_DQ	(SRAM_DQ),	//	conduit_end.export
		.SRAM_ADDR	(SRAM_ADDR),	//			.export
		.SRAM_UB_N	(SRAM_UB_N),	//			.export
		.SRAM_LB_N	(SRAM_LB_N),	//			.export
		.SRAM_WE_N	(SRAM_WE_N),	//			.export
		.SRAM_CE_N	(SRAM_CE_N),	//			.export
		.SRAM_OE_N	(SRAM_OE_N)	//			.export
	);
```

```
endmodule
```

start.v

```
module start(
                    iclk,
                    ireset_n,
                    ix_cnt,
                    iy_cnt,
                    oOVERRIDE,
                    oADDR
                        );

//================================================
//I/O DECALARATION==============================
//================================================
input iclk;
input ireset_n;
input [10:0] ix_cnt;
input [9:0] iy_cnt;
output oOVERRIDE;
output [17:0] oADDR;

//================================================
//WIRE & REG====================================
//================================================
wire [10:0]iletter_pos_x;
wire [9:0] iletter_pos_y;
wire iletter;
wire [4:0]override;
wire [17:0] address [0:4];

//================================================
//PARAMETER=====================================
//================================================
parameter A = 5'd1;
parameter B = 5'd2;
parameter C = 5'd3;
parameter D = 5'd4;
parameter E = 5'd5;
parameter F = 5'd6;
parameter G = 5'd7;
parameter H = 5'd8;
parameter I = 5'd9;
parameter J = 5'd10;
parameter K = 5'd11;
parameter L = 5'd12;
parameter M = 5'd13;
parameter N = 5'd14;
parameter O = 5'd15;
parameter P = 5'd16;
parameter Q = 5'd17;
parameter R = 5'd18;
parameter S = 5'd19;
parameter T = 5'd20;
```

```
parameter U = 5'd21;
parameter V = 5'd22;
parameter W = 5'd23;
parameter X = 5'd24;
parameter Y = 5'd25;
parameter Z = 5'd26;
parameter H_LINE = 1056;
parameter V_LINE = 525;
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
parameter Vertical_Front_Porch = 10;
//=============================================
//Structured logci==============================
//=============================================

letter letter0(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(Hsync_Blank-2+620),
                        .iletter_pos_y(Vertical_Back_Porch-1+264),
                        .iletter(T),
                        .oOVERRIDE(override[0]),
                        .oADDR(address[0]));

letter letter1(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(Hsync_Blank-2+652),
                        .iletter_pos_y(Vertical_Back_Porch-1+264),
                        .iletter(R),
                        .oOVERRIDE(override[1]),
                        .oADDR(address[1]));

letter letter2(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(Hsync_Blank-2+684),
                        .iletter_pos_y(Vertical_Back_Porch-1+264),
                        .iletter(A),
                        .oOVERRIDE(override[2]),
                        .oADDR(address[2]));

letter letter3(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(Hsync_Blank-2+716),
                        .iletter_pos_y(Vertical_Back_Porch-1+264),
                        .iletter(T),
                        .oOVERRIDE(override[3]),
```

```
                        .oADDR(address[3]));

letter letter4(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(Hsync_Blank-2+748),
                        .iletter_pos_y(Vertical_Back_Porch-1+264),
                        .iletter(S),
                        .oOVERRIDE(override[4]),
                        .oADDR(address[4]));

assign oOVERRIDE = (override[0] || override[1] || override [2] || override[3] || override[4]);
assign oADDR = override[0] ? address[0] :
                                override[1] ? address[1] :
                                override[2] ? address[2] :
                                override[3] ? address[3] :
                                override[4] ? address[4] : 18'bZ;
endmodule
```

symbol.v

```
module symbol(
                        iclk,
                        ireset_n,
                        ix_cnt,
                        iy_cnt,
                        isymbol_pos_x,
                        isymbol_pos_y,
                        iBASE_ADDR,
                        oOVERRIDE,
                        oADDR
                        );

//=============================================
//I/O DECALARATION=============================
//=============================================
input iclk;
input ireset_n;
input [10:0] ix_cnt;
input [9:0] iy_cnt;
input [10:0]isymbol_pos_x;
input [9:0]isymbol_pos_y;
input [17:0] iBASE_ADDR;
output oOVERRIDE;
output [17:0] oADDR;


//=============================================
//WIRE & REG==================================
//=============================================
reg    oOVERRIDE;
reg [17:0] oADDR;
reg [5:0] counter;
wire display_area;
```

```
reg white[0:3599];

//================================================
//Structured logic================================
//================================================
assign display_area = ((ix_cnt > isymbol_pos_x-1) && (ix_cnt < isymbol_pos_x + 60)
                                        && (iy_cnt > isymbol_pos_y -1) && (iy_cnt <
isymbol_pos_y + 60)) ? 1'b1:1'b0;


always@(negedge ireset_n)
begin
      if(!ireset_n)
            begin
            case(iBASE_ADDR)
            //clock
            18'd89039: begin
            white[ 0 ]<=0;
            white[ 1 ]<=0;
            white[ 2 ]<=0;
            white[ 3 ]<=0;
            white[ 4 ]<=0;
            white[ 5 ]<=0;
            white[ 6 ]<=0;
            white[ 7 ]<=0;
            white[ 8 ]<=0;
            white[ 9 ]<=0;
            white[ 10 ]<=0;
            white[ 11 ]<=0;
            white[ 12 ]<=0;
            white[ 13 ]<=0;
            white[ 14 ]<=0;
            white[ 15 ]<=1;
            white[ 16 ]<=1;
            white[ 17 ]<=1;
            white[ 18 ]<=1;
            white[ 19 ]<=1;
            white[ 20 ]<=1;
            white[ 21 ]<=1;
            white[ 22 ]<=0;
            white[ 23 ]<=0;
            white[ 24 ]<=0;
            white[ 25 ]<=0;
            white[ 26 ]<=0;
            white[ 27 ]<=0;
            white[ 28 ]<=0;
            white[ 29 ]<=0;
            white[ 30 ]<=0;
            white[ 31 ]<=0;
            white[ 32 ]<=0;
            white[ 33 ]<=0;
            white[ 34 ]<=0;
            white[ 35 ]<=0;
            white[ 36 ]<=0;
            white[ 37 ]<=0;
            white[ 38 ]<=1;
            white[ 39 ]<=1;
            white[ 40 ]<=1;
```

```
white[ 41 ]<=1;
white[ 42 ]<=1;
white[ 43 ]<=1;
white[ 44 ]<=1;
white[ 45 ]<=0;
white[ 46 ]<=0;
white[ 47 ]<=0;
white[ 48 ]<=0;
white[ 49 ]<=0;
white[ 50 ]<=0;
white[ 51 ]<=0;
white[ 52 ]<=0;
white[ 53 ]<=0;
white[ 54 ]<=0;
white[ 55 ]<=0;
white[ 56 ]<=0;
white[ 57 ]<=0;
white[ 58 ]<=0;
white[ 59 ]<=0;
white[ 60 ]<=0;
white[ 61 ]<=0;
white[ 62 ]<=0;
white[ 63 ]<=0;
white[ 64 ]<=0;
white[ 65 ]<=0;
white[ 66 ]<=0;
white[ 67 ]<=0;
white[ 68 ]<=0;
white[ 69 ]<=0;
white[ 70 ]<=0;
white[ 71 ]<=0;
white[ 72 ]<=0;
white[ 73 ]<=1;
white[ 74 ]<=1;
white[ 75 ]<=1;
white[ 76 ]<=1;
white[ 77 ]<=1;
white[ 78 ]<=1;
white[ 79 ]<=1;
white[ 80 ]<=1;
white[ 81 ]<=1;
white[ 82 ]<=1;
white[ 83 ]<=1;
white[ 84 ]<=0;
white[ 85 ]<=0;
white[ 86 ]<=0;
white[ 87 ]<=0;
white[ 88 ]<=0;
white[ 89 ]<=0;
white[ 90 ]<=0;
white[ 91 ]<=0;
white[ 92 ]<=0;
white[ 93 ]<=0;
white[ 94 ]<=0;
white[ 95 ]<=0;
white[ 96 ]<=1;
white[ 97 ]<=1;
white[ 98 ]<=1;
```

```
white[ 99 ]<=1;
white[ 100 ]<=1;
white[ 101 ]<=1;
white[ 102 ]<=1;
white[ 103 ]<=1;
white[ 104 ]<=1;
white[ 105 ]<=1;
white[ 106 ]<=1;
white[ 107 ]<=0;
white[ 108 ]<=0;
white[ 109 ]<=0;
white[ 110 ]<=0;
white[ 111 ]<=0;
white[ 112 ]<=0;
white[ 113 ]<=0;
white[ 114 ]<=0;
white[ 115 ]<=0;
white[ 116 ]<=0;
white[ 117 ]<=0;
white[ 118 ]<=0;
white[ 119 ]<=0;
white[ 120 ]<=0;
white[ 121 ]<=0;
white[ 122 ]<=0;
white[ 123 ]<=0;
white[ 124 ]<=0;
white[ 125 ]<=0;
white[ 126 ]<=0;
white[ 127 ]<=0;
white[ 128 ]<=0;
white[ 129 ]<=0;
white[ 130 ]<=0;
white[ 131 ]<=0;
white[ 132 ]<=1;
white[ 133 ]<=1;
white[ 134 ]<=1;
white[ 135 ]<=1;
white[ 136 ]<=1;
white[ 137 ]<=1;
white[ 138 ]<=1;
white[ 139 ]<=1;
white[ 140 ]<=1;
white[ 141 ]<=1;
white[ 142 ]<=1;
white[ 143 ]<=1;
white[ 144 ]<=0;
white[ 145 ]<=0;
white[ 146 ]<=0;
white[ 147 ]<=0;
white[ 148 ]<=0;
white[ 149 ]<=0;
white[ 150 ]<=0;
white[ 151 ]<=0;
white[ 152 ]<=0;
white[ 153 ]<=0;
white[ 154 ]<=0;
white[ 155 ]<=0;
white[ 156 ]<=1;
```

```
white[ 157 ]<=1;
white[ 158 ]<=1;
white[ 159 ]<=1;
white[ 160 ]<=1;
white[ 161 ]<=1;
white[ 162 ]<=1;
white[ 163 ]<=1;
white[ 164 ]<=1;
white[ 165 ]<=1;
white[ 166 ]<=1;
white[ 167 ]<=1;
white[ 168 ]<=0;
white[ 169 ]<=0;
white[ 170 ]<=0;
white[ 171 ]<=0;
white[ 172 ]<=0;
white[ 173 ]<=0;
white[ 174 ]<=0;
white[ 175 ]<=0;
white[ 176 ]<=0;
white[ 177 ]<=0;
white[ 178 ]<=0;
white[ 179 ]<=0;
white[ 180 ]<=0;
white[ 181 ]<=0;
white[ 182 ]<=0;
white[ 183 ]<=0;
white[ 184 ]<=0;
white[ 185 ]<=0;
white[ 186 ]<=0;
white[ 187 ]<=0;
white[ 188 ]<=0;
white[ 189 ]<=0;
white[ 190 ]<=0;
white[ 191 ]<=1;
white[ 192 ]<=1;
white[ 193 ]<=1;
white[ 194 ]<=1;
white[ 195 ]<=1;
white[ 196 ]<=1;
white[ 197 ]<=1;
white[ 198 ]<=1;
white[ 199 ]<=1;
white[ 200 ]<=1;
white[ 201 ]<=1;
white[ 202 ]<=1;
white[ 203 ]<=1;
white[ 204 ]<=1;
white[ 205 ]<=0;
white[ 206 ]<=0;
white[ 207 ]<=0;
white[ 208 ]<=0;
white[ 209 ]<=0;
white[ 210 ]<=0;
white[ 211 ]<=0;
white[ 212 ]<=0;
white[ 213 ]<=0;
white[ 214 ]<=0;
```

```
white[ 215 ]<=1;
white[ 216 ]<=1;
white[ 217 ]<=1;
white[ 218 ]<=1;
white[ 219 ]<=1;
white[ 220 ]<=1;
white[ 221 ]<=1;
white[ 222 ]<=1;
white[ 223 ]<=1;
white[ 224 ]<=1;
white[ 225 ]<=1;
white[ 226 ]<=1;
white[ 227 ]<=1;
white[ 228 ]<=1;
white[ 229 ]<=0;
white[ 230 ]<=0;
white[ 231 ]<=0;
white[ 232 ]<=0;
white[ 233 ]<=0;
white[ 234 ]<=0;
white[ 235 ]<=0;
white[ 236 ]<=0;
white[ 237 ]<=0;
white[ 238 ]<=0;
white[ 239 ]<=0;
white[ 240 ]<=0;
white[ 241 ]<=0;
white[ 242 ]<=0;
white[ 243 ]<=0;
white[ 244 ]<=0;
white[ 245 ]<=0;
white[ 246 ]<=0;
white[ 247 ]<=0;
white[ 248 ]<=0;
white[ 249 ]<=1;
white[ 250 ]<=1;
white[ 251 ]<=1;
white[ 252 ]<=1;
white[ 253 ]<=1;
white[ 254 ]<=1;
white[ 255 ]<=1;
white[ 256 ]<=1;
white[ 257 ]<=1;
white[ 258 ]<=1;
white[ 259 ]<=1;
white[ 260 ]<=1;
white[ 261 ]<=1;
white[ 262 ]<=1;
white[ 263 ]<=1;
white[ 264 ]<=1;
white[ 265 ]<=1;
white[ 266 ]<=0;
white[ 267 ]<=0;
white[ 268 ]<=0;
white[ 269 ]<=0;
white[ 270 ]<=0;
white[ 271 ]<=0;
white[ 272 ]<=0;
```

```
white[ 273 ]<=0;
white[ 274 ]<=1;
white[ 275 ]<=1;
white[ 276 ]<=1;
white[ 277 ]<=1;
white[ 278 ]<=1;
white[ 279 ]<=1;
white[ 280 ]<=1;
white[ 281 ]<=1;
white[ 282 ]<=1;
white[ 283 ]<=1;
white[ 284 ]<=1;
white[ 285 ]<=1;
white[ 286 ]<=1;
white[ 287 ]<=1;
white[ 288 ]<=1;
white[ 289 ]<=1;
white[ 290 ]<=1;
white[ 291 ]<=0;
white[ 292 ]<=0;
white[ 293 ]<=0;
white[ 294 ]<=0;
white[ 295 ]<=0;
white[ 296 ]<=0;
white[ 297 ]<=0;
white[ 298 ]<=0;
white[ 299 ]<=0;
white[ 300 ]<=0;
white[ 301 ]<=0;
white[ 302 ]<=0;
white[ 303 ]<=0;
white[ 304 ]<=0;
white[ 305 ]<=0;
white[ 306 ]<=0;
white[ 307 ]<=0;
white[ 308 ]<=1;
white[ 309 ]<=1;
white[ 310 ]<=1;
white[ 311 ]<=1;
white[ 312 ]<=1;
white[ 313 ]<=1;
white[ 314 ]<=1;
white[ 315 ]<=1;
white[ 316 ]<=1;
white[ 317 ]<=1;
white[ 318 ]<=1;
white[ 319 ]<=1;
white[ 320 ]<=1;
white[ 321 ]<=1;
white[ 322 ]<=1;
white[ 323 ]<=1;
white[ 324 ]<=1;
white[ 325 ]<=1;
white[ 326 ]<=0;
white[ 327 ]<=0;
white[ 328 ]<=0;
white[ 329 ]<=0;
white[ 330 ]<=0;
```

```
white[ 331 ]<=0;
white[ 332 ]<=0;
white[ 333 ]<=0;
white[ 334 ]<=1;
white[ 335 ]<=1;
white[ 336 ]<=1;
white[ 337 ]<=1;
white[ 338 ]<=1;
white[ 339 ]<=1;
white[ 340 ]<=1;
white[ 341 ]<=1;
white[ 342 ]<=1;
white[ 343 ]<=1;
white[ 344 ]<=1;
white[ 345 ]<=1;
white[ 346 ]<=1;
white[ 347 ]<=1;
white[ 348 ]<=1;
white[ 349 ]<=1;
white[ 350 ]<=1;
white[ 351 ]<=1;
white[ 352 ]<=0;
white[ 353 ]<=0;
white[ 354 ]<=0;
white[ 355 ]<=0;
white[ 356 ]<=0;
white[ 357 ]<=0;
white[ 358 ]<=0;
white[ 359 ]<=0;
white[ 360 ]<=0;
white[ 361 ]<=0;
white[ 362 ]<=0;
white[ 363 ]<=0;
white[ 364 ]<=0;
white[ 365 ]<=0;
white[ 366 ]<=0;
white[ 367 ]<=1;
white[ 368 ]<=1;
white[ 369 ]<=1;
white[ 370 ]<=1;
white[ 371 ]<=1;
white[ 372 ]<=1;
white[ 373 ]<=1;
white[ 374 ]<=1;
white[ 375 ]<=1;
white[ 376 ]<=1;
white[ 377 ]<=1;
white[ 378 ]<=1;
white[ 379 ]<=1;
white[ 380 ]<=1;
white[ 381 ]<=1;
white[ 382 ]<=0;
white[ 383 ]<=0;
white[ 384 ]<=0;
white[ 385 ]<=0;
white[ 386 ]<=0;
white[ 387 ]<=0;
white[ 388 ]<=0;
```

```
white[ 389 ]<=0;
white[ 390 ]<=0;
white[ 391 ]<=0;
white[ 392 ]<=0;
white[ 393 ]<=0;
white[ 394 ]<=0;
white[ 395 ]<=0;
white[ 396 ]<=0;
white[ 397 ]<=0;
white[ 398 ]<=1;
white[ 399 ]<=1;
white[ 400 ]<=1;
white[ 401 ]<=1;
white[ 402 ]<=1;
white[ 403 ]<=1;
white[ 404 ]<=1;
white[ 405 ]<=1;
white[ 406 ]<=1;
white[ 407 ]<=1;
white[ 408 ]<=1;
white[ 409 ]<=1;
white[ 410 ]<=1;
white[ 411 ]<=1;
white[ 412 ]<=1;
white[ 413 ]<=0;
white[ 414 ]<=0;
white[ 415 ]<=0;
white[ 416 ]<=0;
white[ 417 ]<=0;
white[ 418 ]<=0;
white[ 419 ]<=0;
white[ 420 ]<=0;
white[ 421 ]<=0;
white[ 422 ]<=0;
white[ 423 ]<=0;
white[ 424 ]<=0;
white[ 425 ]<=0;
white[ 426 ]<=1;
white[ 427 ]<=1;
white[ 428 ]<=1;
white[ 429 ]<=1;
white[ 430 ]<=1;
white[ 431 ]<=1;
white[ 432 ]<=1;
white[ 433 ]<=1;
white[ 434 ]<=1;
white[ 435 ]<=1;
white[ 436 ]<=1;
white[ 437 ]<=1;
white[ 438 ]<=1;
white[ 439 ]<=0;
white[ 440 ]<=0;
white[ 441 ]<=0;
white[ 442 ]<=0;
white[ 443 ]<=0;
white[ 444 ]<=1;
white[ 445 ]<=1;
white[ 446 ]<=1;
```

```
white[ 447 ]<=1;
white[ 448 ]<=1;
white[ 449 ]<=1;
white[ 450 ]<=1;
white[ 451 ]<=1;
white[ 452 ]<=1;
white[ 453 ]<=1;
white[ 454 ]<=1;
white[ 455 ]<=1;
white[ 456 ]<=0;
white[ 457 ]<=0;
white[ 458 ]<=0;
white[ 459 ]<=0;
white[ 460 ]<=0;
white[ 461 ]<=1;
white[ 462 ]<=1;
white[ 463 ]<=1;
white[ 464 ]<=1;
white[ 465 ]<=1;
white[ 466 ]<=1;
white[ 467 ]<=1;
white[ 468 ]<=1;
white[ 469 ]<=1;
white[ 470 ]<=1;
white[ 471 ]<=1;
white[ 472 ]<=1;
white[ 473 ]<=1;
white[ 474 ]<=0;
white[ 475 ]<=0;
white[ 476 ]<=0;
white[ 477 ]<=0;
white[ 478 ]<=0;
white[ 479 ]<=0;
white[ 480 ]<=0;
white[ 481 ]<=0;
white[ 482 ]<=0;
white[ 483 ]<=0;
white[ 484 ]<=0;
white[ 485 ]<=0;
white[ 486 ]<=1;
white[ 487 ]<=1;
white[ 488 ]<=1;
white[ 489 ]<=1;
white[ 490 ]<=1;
white[ 491 ]<=1;
white[ 492 ]<=1;
white[ 493 ]<=1;
white[ 494 ]<=1;
white[ 495 ]<=1;
white[ 496 ]<=1;
white[ 497 ]<=0;
white[ 498 ]<=0;
white[ 499 ]<=0;
white[ 500 ]<=1;
white[ 501 ]<=1;
white[ 502 ]<=1;
white[ 503 ]<=1;
white[ 504 ]<=1;
```

```
white[ 505 ]<=1;
white[ 506 ]<=1;
white[ 507 ]<=1;
white[ 508 ]<=1;
white[ 509 ]<=1;
white[ 510 ]<=1;
white[ 511 ]<=1;
white[ 512 ]<=1;
white[ 513 ]<=1;
white[ 514 ]<=1;
white[ 515 ]<=1;
white[ 516 ]<=1;
white[ 517 ]<=1;
white[ 518 ]<=1;
white[ 519 ]<=1;
white[ 520 ]<=0;
white[ 521 ]<=0;
white[ 522 ]<=0;
white[ 523 ]<=1;
white[ 524 ]<=1;
white[ 525 ]<=1;
white[ 526 ]<=1;
white[ 527 ]<=1;
white[ 528 ]<=1;
white[ 529 ]<=1;
white[ 530 ]<=1;
white[ 531 ]<=1;
white[ 532 ]<=1;
white[ 533 ]<=1;
white[ 534 ]<=0;
white[ 535 ]<=0;
white[ 536 ]<=0;
white[ 537 ]<=0;
white[ 538 ]<=0;
white[ 539 ]<=0;
white[ 540 ]<=0;
white[ 541 ]<=0;
white[ 542 ]<=0;
white[ 543 ]<=0;
white[ 544 ]<=0;
white[ 545 ]<=1;
white[ 546 ]<=1;
white[ 547 ]<=1;
white[ 548 ]<=1;
white[ 549 ]<=1;
white[ 550 ]<=1;
white[ 551 ]<=1;
white[ 552 ]<=1;
white[ 553 ]<=1;
white[ 554 ]<=1;
white[ 555 ]<=0;
white[ 556 ]<=0;
white[ 557 ]<=0;
white[ 558 ]<=1;
white[ 559 ]<=1;
white[ 560 ]<=1;
white[ 561 ]<=1;
white[ 562 ]<=1;
```

```
white[ 563 ]<=1;
white[ 564 ]<=1;
white[ 565 ]<=1;
white[ 566 ]<=1;
white[ 567 ]<=1;
white[ 568 ]<=1;
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white[ 2242 ]<=0;
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white[ 3595 ]<=0;
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white[ 3599 ]<=0;
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//heart
18'd92639: begin
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```

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white[ 1883 ]<=1;
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white[ 1885 ]<=1;
white[ 1886 ]<=1;
white[ 1887 ]<=1;
white[ 1888 ]<=1;
white[ 1889 ]<=1;
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white[ 3540 ]<=0;
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white[ 3569 ]<=0;
white[ 3570 ]<=0;
white[ 3571 ]<=0;
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```
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white[ 3576 ]<=0;
white[ 3577 ]<=0;
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white[ 3593 ]<=0;
white[ 3594 ]<=0;
white[ 3595 ]<=0;
white[ 3596 ]<=0;
white[ 3597 ]<=0;
white[ 3598 ]<=0;
white[ 3599 ]<=0;
end
    //coin
    18'd96239: begin
    white[ 0 ]<=0;
    white[ 1 ]<=0;
    white[ 2 ]<=0;
    white[ 3 ]<=0;
    white[ 4 ]<=0;
    white[ 5 ]<=0;
    white[ 6 ]<=0;
    white[ 7 ]<=0;
    white[ 8 ]<=0;
    white[ 9 ]<=0;
    white[ 10 ]<=0;
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    white[ 13 ]<=0;
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    white[ 15 ]<=0;
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    white[ 18 ]<=0;
    white[ 19 ]<=0;
    white[ 20 ]<=0;
    white[ 21 ]<=0;
    white[ 22 ]<=0;
    white[ 23 ]<=1;
    white[ 24 ]<=1;
    white[ 25 ]<=1;
    white[ 26 ]<=1;
```

```
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white[ 31 ]<=1;
white[ 32 ]<=1;
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white[ 78 ]<=0;
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white[ 80 ]<=1;
white[ 81 ]<=1;
white[ 82 ]<=1;
white[ 83 ]<=1;
white[ 84 ]<=1;
```

```
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white[ 140 ]<=1;
white[ 141 ]<=1;
white[ 142 ]<=1;
```

```
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```

```
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```

```
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```

```
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```
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white[ 490 ]<=1;
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```
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```
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white[ 602 ]<=0;
white[ 603 ]<=0;
white[ 604 ]<=0;
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```
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white[ 659 ]<=0;
white[ 660 ]<=0;
white[ 661 ]<=0;
white[ 662 ]<=0;
white[ 663 ]<=0;
white[ 664 ]<=0;
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```
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white[ 719 ]<=0;
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white[ 3503 ]<=1;
white[ 3504 ]<=1;
white[ 3505 ]<=1;
white[ 3506 ]<=1;
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white[ 3594 ]<=0;
white[ 3595 ]<=0;
white[ 3596 ]<=0;
white[ 3597 ]<=0;
white[ 3598 ]<=0;
white[ 3599 ]<=0;
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//indicator
18'd99839:begin
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white[ 3 ]<=0;
white[ 4 ]<=0;
white[ 5 ]<=0;
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white[ 14 ]<=0;
white[ 15 ]<=0;
white[ 16 ]<=0;
white[ 17 ]<=0;
white[ 18 ]<=0;
```

```
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```

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```

```
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white[ 3033 ]<=1;
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```

```
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```

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```

```
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```

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```

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white[ 3436 ]<=1;
white[ 3437 ]<=1;
white[ 3438 ]<=1;
white[ 3439 ]<=1;
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```

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white[ 3494 ]<=1;
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white[ 3496 ]<=1;
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```

```
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white[ 3551 ]<=1;
white[ 3552 ]<=1;
white[ 3553 ]<=1;
white[ 3554 ]<=1;
white[ 3555 ]<=1;
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```

```
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                white[ 3561 ]<=1;
                white[ 3562 ]<=1;
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                white[ 3583 ]<=1;
                white[ 3584 ]<=1;
                white[ 3585 ]<=1;
                white[ 3586 ]<=1;
                white[ 3587 ]<=1;
                white[ 3588 ]<=1;
                white[ 3589 ]<=1;
                white[ 3590 ]<=1;
                white[ 3591 ]<=1;
                white[ 3592 ]<=1;
                white[ 3593 ]<=1;
                white[ 3594 ]<=0;
                white[ 3595 ]<=0;
                white[ 3596 ]<=0;
                white[ 3597 ]<=0;
                white[ 3598 ]<=0;
                white[ 3599 ]<=0;
                end
endcase
end
end

always@(posedge iclk or negedge ireset_n)
begin
      if(!ireset_n)
      begin
            oOVERRIDE<= 0;
            oADDR <= 18'bZ;
            counter <= 6'd59;
      end
      else if(display_area)
      begin
```

```
            if(counter == 0)
                counter <= 6'd59;
            else
                counter <= counter-1;
            oOVERRIDE <=white[counter + 60*(iy_cnt-isymbol_pos_y)];
            oADDR <= iBASE_ADDR + counter + 60*(iy_cnt-isymbol_pos_y);
        end
        else
        begin
            oOVERRIDE <= 0;
            oADDR <= 18'bZ;
        end
end

endmodule
```

three_wire_controller.v

```
// --------------------------------------------------------------------

// Copyright (c) 2005 by Terasic Technologies Inc.

// --------------------------------------------------------------------

//

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//

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//

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//

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//     which illustrates how these types of functions can be implemented.

//     It is the user's responsibility to verify their design for

//     consistency and functionality through the use of formal

//     verification methods.    Terasic provides no warranty regarding the use

//     or functionality of this code.
```

```
//
// --------------------------------------------------------------------
//
//                          Terasic Technologies Inc
//                          356 Fu-Shin E. Rd Sec. 1. JhuBei City,
//                          HsinChu County, Taiwan
//                          302
//
//                          web: http://www.terasic.com/
//                          email: support@terasic.com
//
// --------------------------------------------------------------------
//
// Major Functions: 3-Wire Serial Bus Controller
//
// --------------------------------------------------------------------
//
// Revision History :
// --------------------------------------------------------------------
//     Ver  :| Author              :| Mod. Date :| Changes Made:
//     V1.0 :| Johnny Chen         :| 06/03/23  :|          Initial Revision
// --------------------------------------------------------------------

module three_wire_controller(     //     Host Side
                                  iCLK,
                                  iRST,
                                  iDATA,
                                  iSTR,
                                  oACK,
```

```
                                oRDY,
                                oCLK,
                                //  Serial Side
                                oSCEN,
                                SDA,
                                oSCLK    );
//  Host Side
input           iCLK;
input           iRST;
input           iSTR;
input   [15:0]  iDATA;
output          oACK;
output          oRDY;
output          oCLK;
//  Serial Side
output          oSCEN;
inout           SDA;
output          oSCLK;
//  Internal Register and Wire
reg             mSPI_CLK;
reg     [15:0]  mSPI_CLK_DIV;
reg             mSEN;
reg             mSDATA;
reg             mSCLK;
reg             mACK;
reg     [4:0] mST;

parameter   CLK_Freq =  50000000;   //  50  MHz
parameter   SPI_Freq  =  20000;     //  20  KHz
```

```
//  Serial Clock Generator
always@(posedge iCLK or negedge iRST)
begin
    if(!iRST)
    begin
        mSPI_CLK<=  0;
        mSPI_CLK_DIV<=  0;
    end
    else
    begin
        if( mSPI_CLK_DIV  < (CLK_Freq/SPI_Freq) )
        mSPI_CLK_DIV<=  mSPI_CLK_DIV+1;
        else
        begin
            mSPI_CLK_DIV<=  0;
            mSPI_CLK    <=  ~mSPI_CLK;
        end
    end
end
//  Parallel to Serial
always@(negedge mSPI_CLK or negedge iRST)
begin
    if(!iRST)
    begin
        mSEN    <=  1'b1;
        mSCLK   <=  1'b0;
        mSDATA  <=  1'bz;
        mACK    <=  1'b0;
```

```
        mST       <=   4'h00;
    end
    else
    begin
        if(iSTR)
        begin
            if(mST<17)
            mST <=   mST+1'b1;
            if(mST==0)
            begin
                mSEN     <=   1'b0;
                mSCLK    <=   1'b1;
            end
            else if(mST==8)
            mACK     <=   SDA;
            else if(mST==16 && mSCLK)
            begin
                mSEN     <=   1'b1;
                mSCLK    <=   1'b0;
            end
            if(mST<16)
            mSDATA  <=   iDATA[15-mST];
        end
        else
        begin
            mSEN     <=   1'b1;
            mSCLK    <=   1'b0;
            mSDATA  <=   1'bz;
            mACK     <=   1'b0;
```

```
                mST     <=  4'h00;
            end
        end
end

assign  oACK        =   mACK;
assign  oRDY        =   (mST==17)   ?   1'b1 :   1'b0;
assign  oSCEN       =   mSEN;
assign  oSCLK       =   mSCLK   &   mSPI_CLK;
assign  SDA =   (mST==8) ?  1'bz :
                            (mST==17)   ?   1'bz :
                                            mSDATA ;
assign  oCLK        =   mSPI_CLK;

endmodule
```

Timmer.v

```
module Timmer(
                clk_ltm,
                reset_n,
                x_cnt,
                y_cnt,
                state,
                oOVERRIDE,
                oADDR
                );

input clk_ltm;
input reset_n;
input [3:0] state;
input [10:0] x_cnt;
input [9:0] y_cnt;
output oOVERRIDE;
output [17:0] oADDR;
//PARAMETER
parameter BASE_ADDR = 89025;
parameter INIT = 4'b0100;
parameter START = 4'b0101;
parameter PAUSE = 4'b0110;
parameter H_LINE = 1056;
parameter V_LINE = 525;
```

```
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
parameter Vertical_Front_Porch = 10;
parameter clock_base = 18'd89039;
//WIRE & REG
reg [3:0] inumber_s;
reg [3:0] inumber_ts;
reg [3:0] inumber_min;
reg [26:0] counter;

wire [3:0] num_input_s;
wire [3:0] num_input_ts;
wire [3:0] num_input_min;
wire [26:0] oCNT;
wire [3:0] OVERRIDE;
wire flag1;
wire flag2;
wire [17:0] address;

symbol clock(
                        .iclk(clk_ltm),
                        .ireset_n(reset_n),
                        .ix_cnt(x_cnt),
                        .iy_cnt(y_cnt),
                        .isymbol_pos_x(Hsync_Blank-1+730),
                        .isymbol_pos_y(Vertical_Back_Porch+10),
                        .iBASE_ADDR(clock_base),
                        .oOVERRIDE(OVERRIDE[3]),
                        .oADDR(address)
);
//////////////////////Timmer//////////////////////////
number LED0(
                        .iclk(clk_ltm),
                        .iReset_n(reset_n),
                        .ixcount(x_cnt),
                        .iycount(y_cnt),
                        .iled_pos_x(Hsync_Blank-1+600),
                        .iled_pos_y(Vertical_Back_Porch),
                        .inumber(num_input_s),
                        .oOVERRIDE(OVERRIDE[0])
);

number LED1(
                        .iclk(clk_ltm),
                        .iReset_n(reset_n),
                        .ixcount(x_cnt),
                        .iycount(y_cnt),
                        .iled_pos_x(Hsync_Blank-1+640),
                        .iled_pos_y(Vertical_Back_Porch),
                        .inumber(num_input_ts),
                        .oOVERRIDE(OVERRIDE[1])
);

number LED2(
                        .iclk(clk_ltm),
                        .iReset_n(reset_n),
                        .ixcount(x_cnt),
```

```
                        .iycount(y_cnt),
                        .iled_pos_x(Hsync_Blank-1+680),
                        .iled_pos_y(Vertical_Back_Porch),
                        .inumber(num_input_min),
                        .oOVERRIDE(OVERRIDE[2])
);

assign flag1 = (oCNT == 26'd24999999) ? 1'b1 : 1'b0;
assign flag2 = (inumber_s == 0) ? 1'b1 : 1'b0;
assign num_input_s = inumber_s;
assign num_input_ts = inumber_ts;
assign num_input_min = inumber_min;
assign oCNT = counter;


always@(posedge clk_ltm or negedge reset_n)
begin
      if(!reset_n)
      begin
      inumber_min <= 4'd2;
      inumber_ts <= 4'd0;
      inumber_s <= 4'd0;
      counter <= 26'b0;
      end
      else if(state == INIT)
      begin
      inumber_min <= 4'd2;
      inumber_ts <= 4'd0;
      inumber_s <= 4'd0;
      counter <= 26'b0;
      end
      else if(state == PAUSE)
      begin
      inumber_min <= inumber_min;
      inumber_ts <= inumber_ts;
      inumber_s <= inumber_s;
      end
      else if(state == START)
            begin
            if(flag1)
            begin
                  if(flag2)
                        begin
                              if(inumber_ts != 0)
                                    begin
                                          inumber_ts <= inumber_ts - 1;
                                          inumber_s <= 4'd9;
                                          counter <= 26'b0;
                                    end
                              else
                                    begin
                                          if(inumber_min != 0)
                                                begin
                                                      inumber_min <= inumber_min -1;
                                                      inumber_ts    <= 4'd5;
                                                      inumber_s     <= 4'd9;
                                                      counter <= 26'b0;
                                                end
```

```
                                    else
                                        begin
                                            inumber_min <= 4'd2;
                                            inumber_ts <= 4'd0;
                                            inumber_s <= 4'd0;
                                            counter <= 26'b0;
                                        end
                                end
                            end
                        else
                        begin
                        inumber_s <= inumber_s-1;
                        counter <= 26'b0;
                        end
                end
        else
                counter <= counter +1;
        end
end

////OUTPUT
assign oOVERRIDE = OVERRIDE[0] || OVERRIDE[1] || OVERRIDE[2] || OVERRIDE[3];
assign oADDR = (OVERRIDE[0] || OVERRIDE[1] || OVERRIDE[2]) ? BASE_ADDR:
                            OVERRIDE[3] ? address : 18'bZ;

endmodule
```

touch_irq_detector.v

```
// --------------------------------------------------------------------

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// --------------------------------------------------------------------

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```

```
//      which illustrates how these types of functions can be implemented.
//      It is the user's responsibility to verify their design for
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//
// --------------------------------------------------------------------
//
//                                 Terasic Technologies Inc
//                                 356 Fu-Shin E. Rd Sec. 1. JhuBei City,
//                                 HsinChu County, Taiwan
//                                 302
//
//                                 web: http://www.terasic.com/
//                                 email: support@terasic.com
//
// --------------------------------------------------------------------
//
// Major Functions:
//
// --------------------------------------------------------------------
//
// Revision History :
// --------------------------------------------------------------------
//      Ver    :| Author                    :| Mod. Date :| Changes Made:
//      V1.0 :| Johnny Fan                 :| 07/06/30    :| Initial Revision
// --------------------------------------------------------------------
module touch_irq_detector   (
                                clk,
```

```
                        reset_n,
                        iTOUCH_IRQ,
                        iX_COORD,
                        iY_COORD,
                        iNEW_COORD,
                        oDISPLAY_MODE
                        );

//=============================================================================
// PARAMETER declarations
//=============================================================================

parameter      TOUCH_CNT_CLEAR = 24'h2fffff;    // total photo numbers

//=============================================================================
// PORT declarations
//=============================================================================
input      wire       clk;     // system clock 50Mhz
input      wire       reset_n;// system reset
input                 iTOUCH_IRQ;
input      [11:0]     iX_COORD;              // X coordinate form touch panel
input      [11:0]     iY_COORD;              // Y coordinate form touch panel
input                 iNEW_COORD;                 // new coordinates indicate
output     oDISPLAY_MODE;          // displaed photo number
//=============================================================================
// REG/WIRE declarations
//=============================================================================
reg                   touch_en;
reg                   touch_en_clr;
```

```
reg   [24:0]      touch_delay_cnt;
reg   oDISPLAY_MODE;
//=============================================================================
// Structural coding
//=============================================================================

always@(posedge clk or negedge reset_n)
      begin
            if (!reset_n)
                  touch_en <= 0;
            else if (touch_en_clr)
                  touch_en <= 0;
            else if (iTOUCH_IRQ)
                  touch_en <= 1;
      end



always@(posedge clk or negedge reset_n)
      begin
            if (!reset_n)
                  begin
                        touch_delay_cnt <= 0;
                        touch_en_clr <= 0;
                  end
            else if (touch_delay_cnt == TOUCH_CNT_CLEAR)
                  begin
                        touch_delay_cnt <= 0;
                        touch_en_clr <= 1;
                  end
```

```
        else if (touch_en)
            touch_delay_cnt <= touch_delay_cnt + 1;
        else
            begin
                touch_delay_cnt <= 0;
                touch_en_clr <= 0;
            end
    end


always@(posedge clk or negedge reset_n)
    begin
        if (!reset_n)
            oDISPLAY_MODE <= 0;
        else if(iTOUCH_IRQ ==0)
            oDISPLAY_MODE <= 0;
        else if (iTOUCH_IRQ && !touch_en)
            oDISPLAY_MODE <= oDISPLAY_MODE + 1;
    end

endmodule
```

welcome.v

```
module welcome(
                    iclk,
                    ireset_n,
                    ix_cnt,
                    iy_cnt,
                    istate,
                    oADDR);

//=============================================
//Parameter=============================
//=============================================
parameter A = 5'd1;
parameter B = 5'd2;
parameter C = 5'd3;
parameter D = 5'd4;
```

```
parameter E = 5'd5;
parameter F = 5'd6;
parameter G = 5'd7;
parameter H = 5'd8;
parameter I = 5'd9;
parameter J = 5'd10;
parameter K = 5'd11;
parameter L = 5'd12;
parameter M = 5'd13;
parameter N = 5'd14;
parameter O = 5'd15;
parameter P = 5'd16;
parameter Q = 5'd17;
parameter R = 5'd18;
parameter S = 5'd19;
parameter T = 5'd20;
parameter U = 5'd21;
parameter V = 5'd22;
parameter W = 5'd23;
parameter X = 5'd24;
parameter Y = 5'd25;
parameter Z = 5'd26;

parameter H_LINE = 1056;
parameter V_LINE = 525;
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
parameter Vertical_Front_Porch = 10;
parameter indicator_base = 18'd99839;
//=============================================
//I/O DECALARATION=============================
//=============================================
input iclk;
input ireset_n;
input [10:0] ix_cnt;
input [9:0] iy_cnt;
input [3:0] istate;
output [17:0] oADDR;

//=============================================
//WIRE & REG=============================
//=============================================
wire [4:0] letter[0:24];
wire [10:0] letter_pos_x[0:24];
wire [9:0] letter_pos_y[0:24];
wire [25:0] override;
wire [17:0] address[0:25];
reg [17:0] oADDR;
reg [10:0] symbol_pos_x;
reg [9:0] symbol_pos_y;
wire [3:0] state;

//=============================================
//Structured logic=============================
//=============================================
assign state = istate;
```

```
//Assign Letters
assign letter[0] = W;
assign letter[1] = H;
assign letter[2] = A;
assign letter[3] = C;
assign letter[4] = A;
assign letter[5] = M;
assign letter[6] = O;
assign letter[7] = L;
assign letter[8] = E;
assign letter[9] = E;
assign letter[10] = A;
assign letter[11] = S;
assign letter[12] = Y;
assign letter[13] = N;
assign letter[14] = O;
assign letter[15] = R;
assign letter[16] = M;
assign letter[17] = A;
assign letter[18] = L;
assign letter[19] = H;
assign letter[20] = A;
assign letter[21] = R;
assign letter[22] = D;
assign letter[23] = G;
assign letter[24] = O;

//assign letter position
//whac a mole
assign letter_pos_x[0] = Hsync_Blank-2+544;
assign letter_pos_x[1] = Hsync_Blank-2+512;
assign letter_pos_x[2] = Hsync_Blank-2+480;
assign letter_pos_x[3] = Hsync_Blank-2+448;
assign letter_pos_x[4] = Hsync_Blank-2+384;
assign letter_pos_x[5] = Hsync_Blank-2+320;
assign letter_pos_x[6] = Hsync_Blank-2+288;
assign letter_pos_x[7] = Hsync_Blank-2+256;
assign letter_pos_x[8] = Hsync_Blank-2+224;
//easy
assign letter_pos_x[9] = Hsync_Blank-2+432;
assign letter_pos_x[10] = Hsync_Blank-2+400;
assign letter_pos_x[11] = Hsync_Blank-2+368;
assign letter_pos_x[12] = Hsync_Blank-2+336;
//normal
assign letter_pos_x[13] = Hsync_Blank-2+464;
assign letter_pos_x[14] = Hsync_Blank-2+432;
assign letter_pos_x[15] = Hsync_Blank-2+400;
assign letter_pos_x[16] = Hsync_Blank-2+368;
assign letter_pos_x[17] = Hsync_Blank-2+336;
assign letter_pos_x[18] = Hsync_Blank-2+304;
//hard
assign letter_pos_x[19] = Hsync_Blank-2+432;
assign letter_pos_x[20] = Hsync_Blank-2+400;
assign letter_pos_x[21] = Hsync_Blank-2+368;
assign letter_pos_x[22] = Hsync_Blank-2+336;
//go
assign letter_pos_x[23] = Hsync_Blank-2+74;
assign letter_pos_x[24] = Hsync_Blank-2+42;
```

```
assign letter_pos_y[0] = Vertical_Back_Porch-1+80;
assign letter_pos_y[1] = Vertical_Back_Porch-1+75;
assign letter_pos_y[2] = Vertical_Back_Porch-1+70;
assign letter_pos_y[3] = Vertical_Back_Porch-1+65;
assign letter_pos_y[4] = Vertical_Back_Porch-1+60;
assign letter_pos_y[5] = Vertical_Back_Porch-1+65;
assign letter_pos_y[6] = Vertical_Back_Porch-1+70;
assign letter_pos_y[7] = Vertical_Back_Porch-1+75;
assign letter_pos_y[8] = Vertical_Back_Porch-1+80;

assign letter_pos_y[9] = Vertical_Back_Porch-1+160;
assign letter_pos_y[10] = Vertical_Back_Porch-1+160;
assign letter_pos_y[11] = Vertical_Back_Porch-1+160;
assign letter_pos_y[12] = Vertical_Back_Porch-1+160;

assign letter_pos_y[13] = Vertical_Back_Porch-1+240;
assign letter_pos_y[14] = Vertical_Back_Porch-1+240;
assign letter_pos_y[15] = Vertical_Back_Porch-1+240;
assign letter_pos_y[16] = Vertical_Back_Porch-1+240;
assign letter_pos_y[17] = Vertical_Back_Porch-1+240;
assign letter_pos_y[18] = Vertical_Back_Porch-1+240;

assign letter_pos_y[19] = Vertical_Back_Porch-1+320;
assign letter_pos_y[20] = Vertical_Back_Porch-1+320;
assign letter_pos_y[21] = Vertical_Back_Porch-1+320;
assign letter_pos_y[22] = Vertical_Back_Porch-1+320;

assign letter_pos_y[23] = Vertical_Back_Porch-1+408;
assign letter_pos_y[24] = Vertical_Back_Porch-1+408;

letter letter0(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[0]),
                        .iletter_pos_y(letter_pos_y[0]),
                        .iletter(letter[0]),
                        .oOVERRIDE(override[0]),
                        .oADDR(address[0])
                        );

letter letter1(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[1]),
                        .iletter_pos_y(letter_pos_y[1]),
                        .iletter(letter[1]),
                        .oOVERRIDE(override[1]),
                        .oADDR(address[1])
                        );

letter letter2(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
```

```
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[2]),
                .iletter_pos_y(letter_pos_y[2]),
                .iletter(letter[2]),
                .oOVERRIDE(override[2]),
                .oADDR(address[2])
                );

letter letter3(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[3]),
                .iletter_pos_y(letter_pos_y[3]),
                .iletter(letter[3]),
                .oOVERRIDE(override[3]),
                .oADDR(address[3])
                );

letter letter4(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[4]),
                .iletter_pos_y(letter_pos_y[4]),
                .iletter(letter[4]),
                .oOVERRIDE(override[4]),
                .oADDR(address[4])
                );

letter letter5(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[5]),
                .iletter_pos_y(letter_pos_y[5]),
                .iletter(letter[5]),
                .oOVERRIDE(override[5]),
                .oADDR(address[5])
                );

letter letter6(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[6]),
                .iletter_pos_y(letter_pos_y[6]),
                .iletter(letter[6]),
                .oOVERRIDE(override[6]),
                .oADDR(address[6])
                );

letter letter7(
```

```
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[7]),
                .iletter_pos_y(letter_pos_y[7]),
                .iletter(letter[7]),
                .oOVERRIDE(override[7]),
                .oADDR(address[7])
                );

letter letter8(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[8]),
                .iletter_pos_y(letter_pos_y[8]),
                .iletter(letter[8]),
                .oOVERRIDE(override[8]),
                .oADDR(address[8])
                );

letter letter9(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[9]),
                .iletter_pos_y(letter_pos_y[9]),
                .iletter(letter[9]),
                .oOVERRIDE(override[9]),
                .oADDR(address[9])
                );

letter letter10(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[10]),
                .iletter_pos_y(letter_pos_y[10]),
                .iletter(letter[10]),
                .oOVERRIDE(override[10]),
                .oADDR(address[10])
                );

letter letter11(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[11]),
                .iletter_pos_y(letter_pos_y[11]),
                .iletter(letter[11]),
                .oOVERRIDE(override[11]),
                .oADDR(address[11])
                );
```

```
letter letter12(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[12]),
                .iletter_pos_y(letter_pos_y[12]),
                .iletter(letter[12]),
                .oOVERRIDE(override[12]),
                .oADDR(address[12])
                );

letter letter13(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[13]),
                .iletter_pos_y(letter_pos_y[13]),
                .iletter(letter[13]),
                .oOVERRIDE(override[13]),
                .oADDR(address[13])
                );

letter letter14(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[14]),
                .iletter_pos_y(letter_pos_y[14]),
                .iletter(letter[14]),
                .oOVERRIDE(override[14]),
                .oADDR(address[14])
                );

letter letter15(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[15]),
                .iletter_pos_y(letter_pos_y[15]),
                .iletter(letter[15]),
                .oOVERRIDE(override[15]),
                .oADDR(address[15])
                );

letter letter16(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[16]),
                .iletter_pos_y(letter_pos_y[16]),
                .iletter(letter[16]),
                .oOVERRIDE(override[16]),
```

```
                .oADDR(address[16])
                );

letter letter17(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[17]),
                .iletter_pos_y(letter_pos_y[17]),
                .iletter(letter[17]),
                .oOVERRIDE(override[17]),
                .oADDR(address[17])
                );

letter letter18(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[18]),
                .iletter_pos_y(letter_pos_y[18]),
                .iletter(letter[18]),
                .oOVERRIDE(override[18]),
                .oADDR(address[18])
                );

letter letter19(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[19]),
                .iletter_pos_y(letter_pos_y[19]),
                .iletter(letter[19]),
                .oOVERRIDE(override[19]),
                .oADDR(address[19])
                );

letter letter20(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[20]),
                .iletter_pos_y(letter_pos_y[20]),
                .iletter(letter[20]),
                .oOVERRIDE(override[20]),
                .oADDR(address[20])
                );

letter letter21(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[21]),
                .iletter_pos_y(letter_pos_y[21]),
```

```
                        .iletter(letter[21]),
                        .oOVERRIDE(override[21]),
                        .oADDR(address[21])
                        );

letter letter22(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[22]),
                        .iletter_pos_y(letter_pos_y[22]),
                        .iletter(letter[22]),
                        .oOVERRIDE(override[22]),
                        .oADDR(address[22])
                        );


letter letter23(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[23]),
                        .iletter_pos_y(letter_pos_y[23]),
                        .iletter(letter[23]),
                        .oOVERRIDE(override[23]),
                        .oADDR(address[23])
                        );

letter letter24(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[24]),
                        .iletter_pos_y(letter_pos_y[24]),
                        .iletter(letter[24]),
                        .oOVERRIDE(override[24]),
                        .oADDR(address[24])
                        );

symbol indicator(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .isymbol_pos_x(symbol_pos_x),
                        .isymbol_pos_y(symbol_pos_y),
                        .iBASE_ADDR(indicator_base),
                        .oOVERRIDE(override[25]),
                        .oADDR(address[25])
                        );

always@(posedge iclk or negedge ireset_n)
begin
    if(!ireset_n)
    begin
```

```
            symbol_pos_x <= Hsync_Blank-2+528;
            symbol_pos_y <= Vertical_Back_Porch-1+144;
        end
        else if(state == 4'b0000)
        begin
            symbol_pos_x <= Hsync_Blank-2+528;
            symbol_pos_y <= Vertical_Back_Porch-1+144;
        end
        else if(state == 4'b0001)
        begin
            symbol_pos_x <= Hsync_Blank-2+528;
            symbol_pos_y <= Vertical_Back_Porch-1+224;
        end
        else if(state == 4'b0010)
        begin
            symbol_pos_x <= Hsync_Blank-2+528;
            symbol_pos_y <= Vertical_Back_Porch-1+304;
        end
end

always@(posedge iclk or negedge ireset_n)
begin
        if(!ireset_n)
            oADDR <= 18'bZ;
        else
            case(override)
            26'b00000000000000000000000001 : oADDR <= address[0];
            26'b00000000000000000000000010 : oADDR <= address[1];
            26'b00000000000000000000000100 : oADDR <= address[2];
            26'b00000000000000000000001000 : oADDR <= address[3];
            26'b00000000000000000000010000 : oADDR <= address[4];
            26'b00000000000000000000100000 : oADDR <= address[5];
            26'b00000000000000000001000000 : oADDR <= address[6];
            26'b00000000000000000010000000 : oADDR <= address[7];
            26'b00000000000000000100000000 : oADDR <= address[8];
            26'b00000000000000001000000000 : oADDR <= address[9];
            26'b00000000000000010000000000 : oADDR <= address[10];
            26'b00000000000000100000000000 : oADDR <= address[11];
            26'b00000000000001000000000000 : oADDR <= address[12];
            26'b00000000000010000000000000 : oADDR <= address[13];
            26'b00000000000100000000000000 : oADDR <= address[14];
            26'b00000000001000000000000000 : oADDR <= address[15];
            26'b00000000010000000000000000 : oADDR <= address[16];
            26'b00000000100000000000000000 : oADDR <= address[17];
            26'b00000001000000000000000000 : oADDR <= address[18];
            26'b00000010000000000000000000 : oADDR <= address[19];
            26'b00000100000000000000000000 : oADDR <= address[20];
            26'b00001000000000000000000000 : oADDR <= address[21];
            26'b00010000000000000000000000 : oADDR <= address[22];
            26'b00100000000000000000000000 : oADDR <= address[23];
            26'b01000000000000000000000000 : oADDR <= address[24];
            26'b10000000000000000000000000 : oADDR <= address[25];
            default: oADDR <= 18'd89025;
            endcase;
end

endmodule
```

win.v

```
module win(
                        iclk,
                        ireset_n,
                        ix_cnt,
                        iy_cnt,
                        oADDR);

//================================================
//Parameter=============================
//================================================
parameter A = 5'd1;
parameter B = 5'd2;
parameter C = 5'd3;
parameter D = 5'd4;
parameter E = 5'd5;
parameter F = 5'd6;
parameter G = 5'd7;
parameter H = 5'd8;
parameter I = 5'd9;
parameter J = 5'd10;
parameter K = 5'd11;
parameter L = 5'd12;
parameter M = 5'd13;
parameter N = 5'd14;
parameter O = 5'd15;
parameter P = 5'd16;
parameter Q = 5'd17;
parameter R = 5'd18;
parameter S = 5'd19;
parameter T = 5'd20;
parameter U = 5'd21;
parameter V = 5'd22;
parameter W = 5'd23;
parameter X = 5'd24;
parameter Y = 5'd25;
parameter Z = 5'd26;

parameter H_LINE = 1056;
parameter V_LINE = 525;
parameter Hsync_Blank = 216;
parameter Hsync_Front_Porch = 40;
parameter Vertical_Back_Porch = 35;
parameter Vertical_Front_Porch = 10;
//================================================
//I/O DECALARATION=============================
//================================================
input iclk;
input ireset_n;
input [10:0] ix_cnt;
input [9:0] iy_cnt;
output [17:0] oADDR;

//================================================
//WIRE & REG=============================
//================================================
wire [4:0] letter[0:20];
```

```
wire [10:0] letter_pos_x[0:20];
wire [9:0] letter_pos_y[0:20];
wire [20:0] override;
wire [17:0] address[0:20];
reg [17:0] oADDR;
//============================================
//Structured logic==============================
//============================================
//Assign Letters
assign letter[0] = Y;
assign letter[1] = O;
assign letter[2] = U;
assign letter[3] = W;
assign letter[4] = I;
assign letter[5] = N;
assign letter[6] = C;
assign letter[7] = O;
assign letter[8] = N;
assign letter[9] = G;
assign letter[10] = R;
assign letter[11] = A;
assign letter[12] = D;
assign letter[13] = U;
assign letter[14] = L;
assign letter[15] = A;
assign letter[16] = T;
assign letter[17] = I;
assign letter[18] = O;
assign letter[19] = N;
assign letter[20] = S;


//assign letter position
assign letter_pos_x[0] = Hsync_Blank-2+480;
assign letter_pos_x[1] = Hsync_Blank-2+448;
assign letter_pos_x[2] = Hsync_Blank-2+416;
assign letter_pos_x[3] = Hsync_Blank-2+352;
assign letter_pos_x[4] = Hsync_Blank-2+320;
assign letter_pos_x[5] = Hsync_Blank-2+288;

assign letter_pos_x[6] = Hsync_Blank-2+608;
assign letter_pos_x[7] = Hsync_Blank-2+576;
assign letter_pos_x[8] = Hsync_Blank-2+544;
assign letter_pos_x[9] = Hsync_Blank-2+512;
assign letter_pos_x[10] = Hsync_Blank-2+480;
assign letter_pos_x[11] = Hsync_Blank-2+448;
assign letter_pos_x[12] = Hsync_Blank-2+416;
assign letter_pos_x[13] = Hsync_Blank-2+384;
assign letter_pos_x[14] = Hsync_Blank-2+352;
assign letter_pos_x[15] = Hsync_Blank-2+320;
assign letter_pos_x[16] = Hsync_Blank-2+288;
assign letter_pos_x[17] = Hsync_Blank-2+256;
assign letter_pos_x[18] = Hsync_Blank-2+224;
assign letter_pos_x[19] = Hsync_Blank-2+192;
assign letter_pos_x[20] = Hsync_Blank-2+160;


assign letter_pos_y[0] = Vertical_Back_Porch-1+160;
```

```
assign letter_pos_y[1] = Vertical_Back_Porch-1+160;
assign letter_pos_y[2] = Vertical_Back_Porch-1+160;
assign letter_pos_y[3] = Vertical_Back_Porch-1+160;
assign letter_pos_y[4] = Vertical_Back_Porch-1+160;
assign letter_pos_y[5] = Vertical_Back_Porch-1+160;

assign letter_pos_y[6] = Vertical_Back_Porch-1+240;
assign letter_pos_y[7] = Vertical_Back_Porch-1+240;
assign letter_pos_y[8] = Vertical_Back_Porch-1+240;
assign letter_pos_y[9] = Vertical_Back_Porch-1+240;
assign letter_pos_y[10] = Vertical_Back_Porch-1+240;
assign letter_pos_y[11] = Vertical_Back_Porch-1+240;
assign letter_pos_y[12] = Vertical_Back_Porch-1+240;
assign letter_pos_y[13] = Vertical_Back_Porch-1+240;
assign letter_pos_y[14] = Vertical_Back_Porch-1+240;
assign letter_pos_y[15] = Vertical_Back_Porch-1+240;
assign letter_pos_y[16] = Vertical_Back_Porch-1+240;
assign letter_pos_y[17] = Vertical_Back_Porch-1+240;
assign letter_pos_y[18] = Vertical_Back_Porch-1+240;
assign letter_pos_y[19] = Vertical_Back_Porch-1+240;
assign letter_pos_y[20] = Vertical_Back_Porch-1+240;


letter letter0(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[0]),
                        .iletter_pos_y(letter_pos_y[0]),
                        .iletter(letter[0]),
                        .oOVERRIDE(override[0]),
                        .oADDR(address[0])
                        );

letter letter1(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[1]),
                        .iletter_pos_y(letter_pos_y[1]),
                        .iletter(letter[1]),
                        .oOVERRIDE(override[1]),
                        .oADDR(address[1])
                        );

letter letter2(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[2]),
                        .iletter_pos_y(letter_pos_y[2]),
                        .iletter(letter[2]),
                        .oOVERRIDE(override[2]),
                        .oADDR(address[2])
                        );
```

```
letter letter3(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[3]),
                .iletter_pos_y(letter_pos_y[3]),
                .iletter(letter[3]),
                .oOVERRIDE(override[3]),
                .oADDR(address[3])
                );

letter letter4(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[4]),
                .iletter_pos_y(letter_pos_y[4]),
                .iletter(letter[4]),
                .oOVERRIDE(override[4]),
                .oADDR(address[4])
                );

letter letter5(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[5]),
                .iletter_pos_y(letter_pos_y[5]),
                .iletter(letter[5]),
                .oOVERRIDE(override[5]),
                .oADDR(address[5])
                );

letter letter6(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[6]),
                .iletter_pos_y(letter_pos_y[6]),
                .iletter(letter[6]),
                .oOVERRIDE(override[6]),
                .oADDR(address[6])
                );

letter letter7(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[7]),
                .iletter_pos_y(letter_pos_y[7]),
                .iletter(letter[7]),
                .oOVERRIDE(override[7]),
```

```
                .oADDR(address[7])
                );

letter letter8(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[8]),
                .iletter_pos_y(letter_pos_y[8]),
                .iletter(letter[8]),
                .oOVERRIDE(override[8]),
                .oADDR(address[8])
                );

letter letter9(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[9]),
                .iletter_pos_y(letter_pos_y[9]),
                .iletter(letter[9]),
                .oOVERRIDE(override[9]),
                .oADDR(address[9])
                );

letter letter10(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[10]),
                .iletter_pos_y(letter_pos_y[10]),
                .iletter(letter[10]),
                .oOVERRIDE(override[10]),
                .oADDR(address[10])
                );

letter letter11(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[11]),
                .iletter_pos_y(letter_pos_y[11]),
                .iletter(letter[11]),
                .oOVERRIDE(override[11]),
                .oADDR(address[11])
                );

letter letter12(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[12]),
                .iletter_pos_y(letter_pos_y[12]),
```

```
                .iletter(letter[12]),
                .oOVERRIDE(override[12]),
                .oADDR(address[12])
                );

letter letter13(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[13]),
                .iletter_pos_y(letter_pos_y[13]),
                .iletter(letter[13]),
                .oOVERRIDE(override[13]),
                .oADDR(address[13])
                );

letter letter14(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[14]),
                .iletter_pos_y(letter_pos_y[14]),
                .iletter(letter[14]),
                .oOVERRIDE(override[14]),
                .oADDR(address[14])
                );

letter letter15(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[15]),
                .iletter_pos_y(letter_pos_y[15]),
                .iletter(letter[15]),
                .oOVERRIDE(override[15]),
                .oADDR(address[15])
                );

letter letter16(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
                .iletter_pos_x(letter_pos_x[16]),
                .iletter_pos_y(letter_pos_y[16]),
                .iletter(letter[16]),
                .oOVERRIDE(override[16]),
                .oADDR(address[16])
                );

letter letter17(
                .iclk(iclk),
                .ireset_n(ireset_n),
                .ix_cnt(ix_cnt),
                .iy_cnt(iy_cnt),
```

```
                        .iletter_pos_x(letter_pos_x[17]),
                        .iletter_pos_y(letter_pos_y[17]),
                        .iletter(letter[17]),
                        .oOVERRIDE(override[17]),
                        .oADDR(address[17])
                        );

letter letter18(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[18]),
                        .iletter_pos_y(letter_pos_y[18]),
                        .iletter(letter[18]),
                        .oOVERRIDE(override[18]),
                        .oADDR(address[18])
                        );

letter letter19(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[19]),
                        .iletter_pos_y(letter_pos_y[19]),
                        .iletter(letter[19]),
                        .oOVERRIDE(override[19]),
                        .oADDR(address[19])
                        );

letter letter20(
                        .iclk(iclk),
                        .ireset_n(ireset_n),
                        .ix_cnt(ix_cnt),
                        .iy_cnt(iy_cnt),
                        .iletter_pos_x(letter_pos_x[20]),
                        .iletter_pos_y(letter_pos_y[20]),
                        .iletter(letter[20]),
                        .oOVERRIDE(override[20]),
                        .oADDR(address[20])
                        );


always@(posedge iclk or negedge ireset_n)
begin
      if(!ireset_n)
            oADDR <= 18'bZ;
      else
            case(override)
            21'b000000000000000000001 : oADDR <= address[0];
            21'b000000000000000000010 : oADDR <= address[1];
            21'b000000000000000000100 : oADDR <= address[2];
            21'b000000000000000001000 : oADDR <= address[3];
            21'b000000000000000010000 : oADDR <= address[4];
            21'b000000000000000100000 : oADDR <= address[5];
            21'b000000000000001000000 : oADDR <= address[6];
            21'b000000000000010000000 : oADDR <= address[7];
```

```
        21'b000000000000100000000 : oADDR <= address[8];
        21'b000000000001000000000 : oADDR <= address[9];
        21'b000000000010000000000 : oADDR <= address[10];
        21'b000000000100000000000 : oADDR <= address[11];
        21'b000000001000000000000 : oADDR <= address[12];
        21'b000000010000000000000 : oADDR <= address[13];
        21'b000000100000000000000 : oADDR <= address[14];
        21'b000001000000000000000 : oADDR <= address[15];
        21'b000010000000000000000 : oADDR <= address[16];
        21'b000100000000000000000 : oADDR <= address[17];
        21'b001000000000000000000 : oADDR <= address[18];
        21'b010000000000000000000 : oADDR <= address[19];
        21'b100000000000000000000 : oADDR <= address[20];
        default: oADDR <= 18'd89025;
        endcase;
end

endmodule
```

xycoord_interface.v

```
module xycoord_interface    (
                            clk,
                            reset_n,
                            read,
                            write,
                            chipselect,
                            address,
                            readdata,
                            writedata,
                        iX_COORD,
                        iY_COORD
                        ////////////////////
                        );


//=======================================================================
// PORT declarations
//=======================================================================
input       clk;     // system clock 50Mhz
input reset_n;// system reset
input       read;
input write;
input chipselect;
input [4:0]address;
output [15:0]readdata;
input [15:0]writedata;
input       [11:0]      iX_COORD;
input       [11:0]      iY_COORD;

//=======================================================================
// REG/WIRE declarations
//=======================================================================
reg         [11:0]      oX_COORD;
reg         [11:0]      oY_COORD;
reg [15:0] readdata_buff;
```

```
//=============================================================================
// Structural coding
//=============================================================================

assign readdata = readdata_buff;
//write the x y coordinates to the avalon bus
always@(posedge clk or negedge reset_n)
	begin
		if(!reset_n)
			readdata_buff <= 12'b0;
		else if (chipselect && read)
			begin
					if(address == 5'b00000)
						readdata_buff <= iX_COORD;
					else if (address == 5'b00001)
						readdata_buff <= iY_COORD;
			end
	end


endmodule
```

functions.h

```
#include <stdio.h>
#include <system.h>
#include <io.h>
#include "background.h"
#include "letters.h"
#include "music.h"

//read x y coordinates, offset = 0 for x and offset = 1 for y
#define IORD_XY_DATA(base,offset) \
	IORD_16DIRECT(base,(offset)*2)
#define IOWR_SRAM_DATA(base,offset,data)\
	IOWR_16DIRECT(base,(offset)*2,data)
#define IORD_SRAM_DATA(base,offset)\
	IORD_16DIRECT(base,(offset)*2)

	// offset = 0 control panel 32bit
	// offset = 1 control mole 32bit
#define IOWR_CONTROL(base,offset,data) \
	IOWR_32DIRECT(base,(offset)*4,data)

//Initialization
void init()
{
	int base = 0;
	int i;
	int data = 0;

   for(i=0;i<32000;i++)
   {
	   data = background[i];
	   IOWR_SRAM_DATA(SRAM_MUX_0_BASE,i,data);
```

```
   } //shifted by 64000

  // printf("parameter control_panel_base = %d\n",base);
   for(i=0; i< 16000;i++)
   {
         data = control_panel[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+64000,i,data); //shift 32000 from the base

   }

  // printf("parameter mole_shape_base = %d\n",base);
   for(i=0; i< 14400;i++)
   {
         data = mole_shape[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+96000,i,data);  //shift  48000  16bit  from  the
base
   }

//writing 26 letters into SRAM
   for(i=0; i<1024;i++)
   {
         data = A[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+124800,i,data);  //shift  48000  16bit  from  the
base
   }

   for(i=0; i<1024;i++)
   {
         data = B[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+126848,i,data);  //shift  48000  16bit  from  the
base
   }

   for(i=0; i<1024;i++)
   {
         data = C[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+128896,i,data);  //shift  48000  16bit  from  the
base
         base = base +1;
   }
   for(i=0; i<1024;i++)
   {
         data = D[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+130944,i,data);  //shift  48000  16bit  from  the
base
   }
   for(i=0; i<1024;i++)
   {
         data = E[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+132992,i,data);  //shift  48000  16bit  from  the
base
   }
   for(i=0; i<1024;i++)
   {
         data = F[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+135040,i,data);  //shift  48000  16bit  from  the
base
   }
```

```
  for(i=0; i<1024;i++)
  {
        data = G[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+137088,i,data); //shift 48000 16bit from the
base
  }
  for(i=0; i<1024;i++)
  {
        data = H[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+139136,i,data); //shift 48000 16bit from the
base
  }
  for(i=0; i<1024;i++)
  {
        data = I[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+141184,i,data); //shift 48000 16bit from the
base
  }
  for(i=0; i<1024;i++)
  {
        data = J[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+143232,i,data); //shift 48000 16bit from the
base
  }
  for(i=0; i<1024;i++)
  {
        data = K[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+145280,i,data); //shift 48000 16bit from the
base
  }
  for(i=0; i<1024;i++)
  {
        data = L[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+147328,i,data); //shift 48000 16bit from the
base
  }
  for(i=0; i<1024;i++)
  {
        data = M[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+149376,i,data); //shift 48000 16bit from the
base
  }
  for(i=0; i<1024;i++)
  {
        data = N[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+151424,i,data); //shift 48000 16bit from the
base
  }
  for(i=0; i<1024;i++)
  {
        data = O[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+153472,i,data); //shift 48000 16bit from the
base
  }
  for(i=0; i<1024;i++)
  {
        data = P[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+155520,i,data); //shift 48000 16bit from the
```

```
base
   }
   for(i=0; i<1024;i++)
   {
         data = Q[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+157568,i,data); //shift 48000 16bit from the
base
   }
   for(i=0; i<1024;i++)
   {
         data = R[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+159616,i,data); //shift 48000 16bit from the
base
   }
   for(i=0; i<1024;i++)
   {
         data = S[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+161664,i,data); //shift 48000 16bit from the
base
   }
   for(i=0; i<1024;i++)
   {
         data = T[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+163712,i,data); //shift 48000 16bit from the
base
   }
   for(i=0; i<1024;i++)
   {
         data = U[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+165760,i,data); //shift 48000 16bit from the
base
   }
   for(i=0; i<1024;i++)
   {
         data = V[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+167808,i,data); //shift 48000 16bit from the
base
   }
   for(i=0; i<1024;i++)
   {
         data = W[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+169856,i,data); //shift 48000 16bit from the
base
   }
   for(i=0; i<1024;i++)
   {
         data = X[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+171904,i,data); //shift 48000 16bit from the
base
   }
   for(i=0; i<1024;i++)
   {
         data = Y[i];
         IOWR_SRAM_DATA(SRAM_MUX_0_BASE+173952,i,data); //shift 48000 16bit from the
base
   }
   for(i=0; i<1024;i++)
   {
```

```
        data = Z[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+176000,i,data); //shift 48000 16bit from the
base
    }
    //write black hole
    for(i=0; i<15;i++)
    {
        data = xcolor[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+178048,i,data); //shift 48000 16bit from the
base
    }

    for(i=0;i<3600;i++)
    {
        data = clock1[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+178078,i,data); //shift 48000 16bit from the
base
    }

    for(i=0;i<3600;i++)
    {
        data = heart[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+185278,i,data); //shift 48000 16bit from the
base
    }

    for(i=0;i<3600;i++)
    {
        data = coin[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+192478,i,data); //shift 48000 16bit from the
base
    }

    for(i=0;i<3600;i++)
    {
        data = indicator[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+199678,i,data);
    }

    for(i=0;i<14400;i++)
    {
        data = bottle1[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+206878,i,data);
    }

    for(i=0;i<14400;i++)
    {
        data = evil[i];
        IOWR_SRAM_DATA(SRAM_MUX_0_BASE+235678,i,data);
    }
}
```

main.c

```
#include <stdio.h>
#include <system.h>
#include <io.h>
#include "functions.h"
#include <stdlib.h>
#include <time.h>
#include <math.h>
#include <sys/alt_irq.h> // the irq functions
#include <sys/types.h>

#define random(x) (rand()%x)

int i=0;
int j;
int m;
int n;
int time_interval=0;
unsigned data_temp;
int state = 0;
int score0 = 0;
int score1 = 0;
int score2 = 0;
int game_time=0;
int life = 3;
int moleP=0;
int showtime=0;
int counter = 0;
int counter_previous = 0;
int random_number=0;
long int panel_command=0;
long int mole_command=0;
int mole_status=0;
int level_mode = 0;
int mole_command1=0;
int mole_command2=0;
int mole_command3=0;
int item=0;
int animal2=0;
int whichmole;
clock_t start_t;
clock_t end_t;
clock_t total_t;




int touch(int state_in){
	int x;
	int y;
	x = IORD_XY_DATA(XYCOORD_INTERFACE_0_BASE,0);
	y = IORD_XY_DATA(XYCOORD_INTERFACE_0_BASE,1);
	if(state_in == 0x4 || state_in == 0x5 || state_in == 0x6 || state_in == 0x7 )
	{
		if(x>0xA10 && x< 0xED0 && y> 0x430 && y< 0x7F0)
			return 0;//mole0
		else if(x>0xA10 && x< 0xED0 && y>0x7F1 && y< 0xBB0)
```

```
                return 1;
        else if(x>0xA10 && x< 0xED0 && y>0xBB0 && y< 0xF40)
                return 2;
        else if(x>0x530 && x< 0xA10 && y> 0x430 && y< 0x7F0)
                return 3;
        else if(x>0x530 && x< 0xA10 && y>0x7F1 && y< 0xBB0)
                return 4;
        else if(x>0x530 && x< 0xA10 && y>0xBB0 && y< 0xF40)
                return 5;
        else if(x>0x0C0 && x< 0x530 && y> 0x430 && y< 0x7F0)
                return 6;
        else if(x>0x0C0 && x< 0x530 && y>0x7F1 && y< 0xBB0)
                return 7;
        else if(x>0x0C0 && x< 0x530 && y>0xBB0 && y< 0xF40)
                return 8;//mole8
        else if(x>0x530 && x<0x790 && y>0x0 && y<0x430)
                return 9; //start key
        else if(x>0x2F0 && x< 0x530 && y>0x0 && y<0x430)
                return 0xA;//pause key
        else if(x>0x0 && x< 0x2F0 && y>0x0 && y<0x430)
                return 0xB; //quit key
        else
                return 0xC;
    }

    else if(state_in == 0x0 || state_in == 0x1 || state_in == 0x2 || state_in == 0x3)
    {
        if(x>0x810 && x< 0xA90 && y> 0x580 && y< 0xA10)
                return 0;// easy
        else if(x>0x610 && x< 0x810 && y> 0x580 && y< 0xA10)
                return 1; // normal
        else if(x>0x370 && x< 0x610 && y> 0x580 && y< 0xA10)
                return 2; // hard
        else if(x>0x0 && x< 0x350 && y> 0xCD0 && y< 0xF98){
                music = 1;
                return 3;} //go
        else
                return 4;
    }
}



int mole_position(int num,int status){

    switch(num%3){
        case 0: item=0;    // mole
                break;
        case 1: item=1;    //bomb
                break;
        case 2: item=2; //bottle
                break;
    }

    while (num%3!=0){
        num--;
    }
    int i=num/3;
```

```
      whichmole = i;
    mole_command = item*pow(8,i)+status*pow(8,i)*4;
    return mole_command;
}



//Music interrupt function
short audio_to_play;
short *music_to_play;
short music_to_play_temp;
short sound_to_play_temp;
short *remember_music_to_play;
short *sound_to_play;
int music = 0;
int remember_music;
int remember_musiclength;
int music_length;
int sound = 0;
int sound_length;
int a,b,c,d,e;
int aa,bb,cc,dd,ee,ff;
int pause = 0;
int pre_pause = 0;

static void standbymusic(){
//    switch(music){
//    case 0: music_length = 368139; break;
//    case 1:    music_length = 78912;    break;
//    case 2:    music_length = 368140; break;
//    case 3:    music_length = 80640;   break;
//    case 4:    music_length = 87552;   break;
//    default:   break;
//    }
      if (b != 1 && d != 1 && e != 1){
      switch(music){
                  case 0: music_length = 368139; if(a==0){i=0;} a=1; b=0 ;c=0;d=0;e = 0;
                                                              music_to_play       =       standby;
break;
                  case 1:    music_length = 78912;    if(b==0){i=0;} b=1; a=0;c=0;d=0;e = 0;
                                                              music_to_play       =       lady_go;
break;
                  case 2:    music_length = 368140; if(c==0){i=0;} c=1; a=0;b=0;d=0;e = 0;
                                                             music_to_play = background_music;
break;
                  case 3:    music_length = 67026;    if(d==0){i=0;} d=1; a=0;b=0;c=0;e = 0;
                                                              music_to_play = victory;       break;
                  case 4:    music_length = 63295;    if(e==0){i=0;} e=1; a=0;b=0;c=0;d = 0;
                                                              music_to_play       =       defeat;
break;
//                          case 5: music_length = 5790;    if(aa==0) m=1; aa=1; bb=0; dd=0;
ee=0; ff = 0;
//
music_to_play = hit;        break;
//                          case 6:    music_length    =    14008;        if(bb==0){m=1;}    bb=1;
aa=0;cc=0;dd=0;ee=0;ff = 0;
//
music_to_play = gold;       break;
```

```
//                              case 7:   music_length    =    13540;    if(cc==0){m=1;}    cc=1;
aa=0;bb=0;dd=0;ee=0;ff = 0;
//
music_to_play = explo;     break;
//                              case 8:   music_length    =    6571;     if(dd==0){m=1;}    dd=1;
aa=0;bb=0;cc=0;ee=0;ff = 0;
//
music_to_play = miss;      break;
//                              case 9:   music_length    =    1961;     if(ee==0){m=1;}    ee=1;
aa=0;bb=0;cc=0;dd=0;ff = 0;
//
music_to_play = button_chose; break;
//                              case 10:  music_length    =    1128;      if(ff==0){m=1;}    ff=1;
aa=0;bb=0;cc=0;dd=0;ee = 0;
//
music_to_play = button_wood;   break;
                        default:   break;
                        }
      }
                              switch(sound){
                                          case 0: sound_length = 5790;
                                                      if(aa==0) m=0;
                                                      aa=1;
                                                      bb=0;
                                                      cc=0;
                                                      dd=0;
                                                      ee=0;
                                                      ff = 0;
                                                      sound_to_play = hit;
                                                      break;
                                          case 1:    sound_length = 14008;    if(bb==0){m=0;} bb=1;
aa=0;cc=0;dd=0;ee=0;ff = 0;
                                                                                  sound_to_play
= gold;       break;
                                          case 2:    sound_length  =  13540;  if(cc==0){m=0;}  cc=1;
aa=0;bb=0;dd=0;ee=0;ff = 0;
                                                                                  sound_to_play
= explo;      break;
                                          case 3:    sound_length  =  6571;   if(dd==0){m=0;}  dd=1;
aa=0;bb=0;cc=0;ee=0;ff = 0;
                                                                                  sound_to_play
= miss;       break;
                                          case 4:    sound_length  =  1961;   if(ee==0){m=0;}  ee=1;
aa=0;bb=0;cc=0;dd=0;ff = 0;
                                                                                  sound_to_play
= button_chose; break;
                                          case 5:    sound_length  =  1128;    if(ff==0){m=0;}  ff=1;
aa=0;bb=0;cc=0;dd=0;ee = 0;
                                                                                  sound_to_play
= button_wood;    break;
                                          default: aa=0;bb=0;cc=0;dd=0;ee=0;ff = 0; m = 0;    break;
                                          }



      for(j=0;j<2048;j++)
```

```
            {

              if (pause == 1){audio_to_play=0;}
//              else if (m!=0){audio_to_play = music_to_play[m];}
//              else audio_to_play = music_to_play[i];
              else if (sound !=6) {
                    music_to_play_temp = music_to_play[i];
                    sound_to_play_temp = sound_to_play[m];
                    audio_to_play = (music_to_play_temp >> 2) + ((sound_to_play_temp>>2)*3);
              }
              else audio_to_play = music_to_play[i];

              IOWR_16DIRECT(MUSICCONTROLLER_0_BASE,j*2,audio_to_play);
                              i++;
                              m++;

              if(i == music_length){ i = 0;
                 if (music == 1) {music = 2; b = 0;}
                 else if (music == 3 || music == 4) {state = 0;d = 0; e = 0;music=0;}

              }
                 //       if(i == 368139){ i = 0;}
              if(m == sound_length){
                    if (pre_pause == 1){pause = 1;}
                    m = 0; sound = 6;}
            }

}


void check_mole(){


      if (random_number==0 || random_number==1 || random_number==2){
            moleP=0;
      }else if (random_number==3 || random_number==4 || random_number==5){
            moleP=1;
      }else if (random_number==6 || random_number==7 || random_number==8){
            moleP=2;
      }else if (random_number==9 || random_number==10 || random_number==11){
            moleP=3;
      }else if (random_number==12 || random_number==13 || random_number==14){
            moleP=4;
      }else if (random_number==15 || random_number==16 || random_number==17){
            moleP=5;
      }else if (random_number==18 || random_number==19 || random_number==20){
            moleP=6;
      }else if (random_number==21 || random_number==22 || random_number==23){
            moleP=7;
      }else if (random_number==24 || random_number==25 || random_number==26){
            moleP=8;
      }
}

void state_sel(int state_in)
{
     check_mole();
     switch(state_in)
```

```
{
        //Welcome-Easy
    case 0x0:
        if(touch(state_in) != 4)
        {
            if(touch(state_in)== 0)
            {
                state = 0x0; //easy
                sound = 4;
            }
            else if(touch(state_in) == 1)
            {
                state = 0x1; // normal
               music = 0;
                sound = 4;
            }
            else if(touch(state_in) == 2)
            {
                state = 0x2; // hard
              music = 0;
                sound = 4;
            }
            else if(touch(state_in)==3){
                state = 0x4;
                level_mode=0;
                music = 2;
                sound = 4;
            }
        }

        break;
        //WELCOME-NORMAL
    case 0x1:
        if(touch(state_in) != 4)
        {
            if(touch(state_in)== 0)
            {
                state = 0;
                music = 0;
                sound = 4;
            }
            else if(touch(state_in) == 1)
            {
                state = 0x1;
                music =0;
                sound = 4;
            }
            else if(touch(state_in) == 2)
            {
                state = 0x2;
                music = 0;
                sound = 4;
            }
            else if(touch(state_in)==3){
                state = 0x4;
                level_mode=1;
                music = 2;
                sound = 4;
```

```
            }
        }
        break;
        //WELCOME-HARD
    case 0x2:
        if(touch(state_in) != 4)
        {
            if(touch(state_in)== 0)
            {
                state = 0;
                music = 0;
                sound = 4;
            }
            else if(touch(state_in) == 1)
            {
                state = 0x1;
                music = 0;
                sound = 4;
            }
            else if(touch(state_in) == 2)
            {
                state = 0x2;
                music = 0;
                sound = 4;
            }
            else if(touch(state_in)==3){
                state = 0x4;
                level_mode=2;
                music = 2;
                sound = 4;
            }
        }
        break;
        //unused state
    case 0x3:
        break;

        //PLAY-INIT
    case 0x4:
        if(touch(state_in) == 0xB)
        {
            state = 0x0;
            music = 0;
            sound = 5;
        }
        else if(touch(state_in) == 0x9)
        {
            state = 0x5;
            music = 2;
            sound =5;

        }
        break;

        //PLAY- ONGOING
    case 0x5:
        if(touch(state_in) == 0xB)
        {
```

```
            state = 0x0;
            sound =5;
            music =0;
        }
        else if(touch(state_in) == 0xA)
        {
            state = 0x6;
            sound =5;
            music = 5;
            pause = 1;
        }
        else if(touch(state_in) == moleP){
            mole_status = 0;
            if(item == 0)
                sound = 0;
            else if(item == 1)
                sound = 2;
            else
                sound = 1;
        }
        else
            sound = 3;
        break;

        //PLAY- PAUSE
    case 0x6:
        if(touch(state_in) == 0xB)
        {
            state = 0x0;
            sound =5;
            pause = 0;
            music = 2;
        }
        else if(touch(state_in) == 0x9)
        {
            state = 0x5;
            sound =5;
            music = 0;
        }
        break;

    case 0x7:
        break;
    case 0x8:
        music = 4;
        break;
    case 0x9:
        break;
    case 0xA:
        break;
    case 0xB:
        break;
    case 0xC:
        music = 3;
        break;
    case 0xD:
        break;
    case 0xE:
```

```
                break;
        case 0xF:
                break;
    }
}

typedef enum {True, False} bool;

static void statedetect()
{
    state_sel(state);
    panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;
    IOWR_CONTROL(INTERRUPT_0_BASE,0,0);
    IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
}


int main (int argc, const char * argv[])
{



    //Music interrupt
    alt_irq_register(MUSICCONTROLLER_0_IRQ, NULL,(void*)standbymusic);
    //touch interrupt
    alt_irq_register(INTERRUPT_0_IRQ, NULL,(void*)statedetect);

    init();

    // initialization
    IOWR_CONTROL(COMMAND_0_BASE,0,0x30);
    IOWR_CONTROL(COMMAND_0_BASE,1,0);

    while (1){
    LOOP: if (state==0x0 || state==0x1 || state==0x2){
        life=3;
        score0=0;
        score1=0;
        score2=0;
        panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;
        IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
        IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
    }

    if (state==0x4){
        if (level_mode==0)
        {
            while(state == 0x4 || state == 0x5 || state ==0x6)
            {
            if (state==0x5)
            {
//              start_t=clock();
//              printf("start time: %d \n", start_t/CLOCKS_PER_SEC);
                while(1 && game_time <= 10000000 ){
                    random_number = rand()%27;
```

```
                mole_status=1;
                mole_command = mole_position( random_number,mole_status);
                panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;



                IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);


                while (mole_status==1 && counter<100000 ){
                    counter++;
                    game_time++;

                    //pause
                    if (state==6){
                    while (state==6){
                        panel_command = state+ life*16 + score0*16*16 +
score1*16*16*16 + score2*16*16*16*16;
                        IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                        IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                    }

                    }
                    else if (state==0x0){

                        IOWR_CONTROL(COMMAND_0_BASE,1,0);
                        IOWR_CONTROL(COMMAND_0_BASE,0,0);
                        goto LOOP;

                    }
                }

                //end_t=clock();
                //printf("end time: %d \n", end_t/CLOCKS_PER_SEC);

            //  total_t = (double)(end_t - start_t) / CLOCKS_PER_SEC;
                //printf("time interval: %f\n",total_t);
                //12000000

                if (counter==100000 ){
                    if (item==0){
                    life--;
                    }
                     if (life<=0){
                        state=0xC;
                        music = 4;
                        panel_command = state+ life*16 + score0*16*16 +
score1*16*16*16 + score2*16*16*16*16;
                        IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                        IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                        while (showtime<500000){
                            showtime++;
                        }
                        showtime=0;
                        state=0;
                        IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
```

```
                    IOWR_CONTROL(COMMAND_0_BASE,0,0x0);
                    goto LOOP;

                }else{
                    mole_status=0;
                    panel_command = state+ life*16 + score0*16*16 +
score1*16*16*16 + score2*16*16*16*16;
                    mole_command =
mole_position(random_number,mole_status);
                    IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                    IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                }
            }else{
                if(item == 0){
                    if(score0 == 0){
                        score0= score0+5;
                    }else if(score1 < 9 ){
                                score0 =0;
                                score1++;
                            }else{
                                    score2++;
                                    score1 = 0;
                                    score0 = 0;
                                }
                    panel_command = state+ life*16 + score0*16*16 +
score1*16*16*16 + score2*16*16*16*16;
                    mole_command = mole_position(random_number, mole_status);
                    IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                    IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                    item=0;

                }else if(item == 2) {
                                    if (life!=3){
                                        life = life +1;//life limit
                                    }

                }else if(item == 1){

                    if(life>0){
                        life = life -1;
                    }else{
                        state=0xC;
                        music = 4;
                        panel_command = state+ life*16 + score0*16*16 +
score1*16*16*16 + score2*16*16*16*16;
                        IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                        IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                        while (showtime<500000){
                            showtime++;
                        }
                        showtime=0;
                        state=0;
                        IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                        IOWR_CONTROL(COMMAND_0_BASE,0,0x0);
                        goto LOOP;
                    }
                }
                 panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
```

```
score2*16*16*16*16;
                        mole_command = mole_position(random_number, mole_status);
                        IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                        IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                        item=0;

                    }

                counter = 0;

                }
                 state=8;
                 music = 3;
                 game_time=0;
                 panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;
                 IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                 IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                 while (showtime<500000){
                       showtime++;
                 }
                 showtime=0;
                 state=0;
                 IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                 IOWR_CONTROL(COMMAND_0_BASE,0,0x0);
                 goto LOOP;
          }
     }

     }
     else if (level_mode==1)        {
          while(state == 0x4 || state == 0x5 || state ==0x6)
          {
          if (state==0x5)
          {
//              start_t=clock();
//              printf("start time: %d \n", start_t/CLOCKS_PER_SEC);
          while(1 && game_time <= 10000000 ){
               random_number = rand()%27;

               mole_status=1;
               mole_command = mole_position( random_number,mole_status);
               panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;



               IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
               IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);


               while (mole_status==1 && counter<70000 ){
                    counter++;
                    game_time++;

                    //pause
                    if (state==6){
                    while (state==6){
```

```
                panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;
                IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
            }

            }
            else if (state==0x0){

                IOWR_CONTROL(COMMAND_0_BASE,1,0);
                IOWR_CONTROL(COMMAND_0_BASE,0,0);
                goto LOOP;

            }
        }


        if (counter==70000 ){
            if (item==0){
            life--;
            }
              if (life<=0){
                  state=0xC;
                  music = 4;
                  panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;
                  IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                  IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                  while (showtime<500000){
                      showtime++;
                  }
                  showtime=0;
                  state=0;
                  IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                  IOWR_CONTROL(COMMAND_0_BASE,0,0x0);
                  goto LOOP;

                    }else{
                      mole_status=0;
                      panel_command = state+ life*16 + score0*16*16 +
score1*16*16*16 + score2*16*16*16*16;
                      mole_command = mole_position(random_number,mole_status);
                      IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                      IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                  }
        }else{
            if(item == 0){
                if(score0 == 0){
                    score0= score0+5;
                }else if(score1 < 9 ){
                                score0 =0;
                                score1++;
                            }else{
                                    score2++;
                                    score1 = 0;
                                    score0 = 0;
                                }
                panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
```

```
score2*16*16*16*16;
                        mole_command = mole_position(random_number, mole_status);
                        IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                        IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                        item=0;

                    }else if(item == 2) {
                                        if (life!=3){
                                            life = life +1;//life limit
                                        }

                    }else if(item == 1){

                        if(life>0){
                            life = life -1;
                        }else{
                            state=0xC;
                            music = 4;
                            panel_command = state+ life*16 + score0*16*16 +
score1*16*16*16 + score2*16*16*16*16;
                            IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                            IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                             while (showtime<500000){
                                  showtime++;
                             }
                             showtime=0;
                             state=0;
                             IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                             IOWR_CONTROL(COMMAND_0_BASE,0,0x0);
                             goto LOOP;
                        }
                    }
                     panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;
                     mole_command = mole_position(random_number, mole_status);
                     IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                     IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                     item=0;

                }

            counter = 0;

            }
             state=8;
             music = 3;
             game_time=0;
             panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;
             IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
             IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
             while (showtime<500000){
                  showtime++;
             }
             showtime=0;
             state=0;
             IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
             IOWR_CONTROL(COMMAND_0_BASE,0,0x0);
```

```
            goto LOOP;
      }
}


      }else if (level_mode==2)        {
            while(state == 0x4 || state == 0x5 || state ==0x6)
            {
            if (state==0x5)
            {

            while(1 && game_time <= 10000000 ){
                  random_number = rand()%27;

                  mole_status=1;
                  mole_command = mole_position( random_number,mole_status);
                  panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;



                  IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                  IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);


                  while (mole_status==1 && counter<40000 ){
                        counter++;
                        game_time++;

                        //pause
                        if (state==6){
                        while (state==6){
                              panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;
                              IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                              IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                        }

                        }
                        else if (state==0x0){

                              IOWR_CONTROL(COMMAND_0_BASE,1,0);
                              IOWR_CONTROL(COMMAND_0_BASE,0,0);
                              goto LOOP;

                        }
                  }


                  if (counter==40000 ){
                        if (item==0){
                        life--;
                        }
                         if (life<=0){
                               state=0xC;
                               music = 4;
                               panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;
```

```
                        IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                        IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                        while (showtime<500000){
                              showtime++;
                        }
                        showtime=0;
                        state=0;
                        IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                        IOWR_CONTROL(COMMAND_0_BASE,0,0x0);
                        goto LOOP;

                            }else{
                              mole_status=0;
                              panel_command = state+ life*16 + score0*16*16 +
score1*16*16*16 + score2*16*16*16*16;
                              mole_command = mole_position(random_number,mole_status);
                              IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                              IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                        }
                  }else{
                        if(item == 0){
                              if(score0 == 0){
                                    score0= score0+5;
                              }else if(score1 < 9 ){
                                          score0 =0;
                                          score1++;
                                    }else{
                                                score2++;
                                                score1 = 0;
                                                score0 = 0;
                                          }
                              panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;
                              mole_command = mole_position(random_number, mole_status);
                              IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                              IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                              item=0;

                        }else if(item == 2) {
                                          if (life!=3){
                                                life = life +1;//life limit
                                          }

                        }else if(item == 1){

                              if(life>0){
                                    life = life -1;
                              }else{
                                    state=0xC;
                                    music = 4;
                                    panel_command = state+ life*16 + score0*16*16 +
score1*16*16*16 + score2*16*16*16*16;
                                    IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                                    IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                                     while (showtime<500000){
                                          showtime++;
                                     }
                                     showtime=0;
```

```
                                state=0;
                                IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                                IOWR_CONTROL(COMMAND_0_BASE,0,0x0);
                                goto LOOP;
                            }
                        }
                         panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;
                         mole_command = mole_position(random_number, mole_status);
                         IOWR_CONTROL(COMMAND_0_BASE,1,mole_command);
                         IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                         item=0;

                    }

                counter = 0;

                }
                  state=8;
                  music = 3;
                  game_time=0;
                  panel_command = state+ life*16 + score0*16*16 + score1*16*16*16 +
score2*16*16*16*16;
                  IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                  IOWR_CONTROL(COMMAND_0_BASE,0,panel_command);
                  while (showtime<500000){
                        showtime++;
                  }
                  showtime=0;
                  state=0;
                  IOWR_CONTROL(COMMAND_0_BASE,1,0x0);
                  IOWR_CONTROL(COMMAND_0_BASE,0,0x0);
                  goto LOOP;
          }
}

          }
}
          }
          return 0;
}
```

background.h

```
const int background[]= {

      25832,38510,38510,30058,36397,25832,25800,34285,38543,27978,23752,23687,15299,19
493,27945,27978,36461,36461,27977,36462,30122,23751,30090,32235,32203,36429,21638,195
26,34349,32236,25897,19526,21606,25865,19525,25864,21638,23751,15299,15331,25864,2167
1,15332,23784,11106,19493,27945,19493,40623,23751,36396,38542,40622,34348,30122,34380
,34348,19557,36461,34380,17444,21702,25864,15331,36461,32235,21638,38542,13250,23815,
28009,32235,38541,25896,36493,30090,32235,25896,21670,38542,38542,23783,23751,23751,2
3816,32235,21670,13219,19557,23783,30090,25896,27977,25864,15299,13186,21670,23783,34
283,27977,40623,36429,21670,34315,44913,32235,38574,27976,40655,40654,40655,21637,216
70,21606,27977,25896,25864,23719,42768,32203,38574,25897,27977,21670,23783,30090,3220
3,27977,17412,40687,30121,25863,34347,28040,25927,25894,32266,25927,30186,38605,28040
```

,38605,36460,40686,25863,34316,34316,13218,30058,17445,34316,38606,32202,32235,30122,25896,25863,36461,34315,25863,36461,30122,30090,11073,30090,21670,25896,34315,36460,32235,32267,30122,30122,30122,25928,34348,32267,36493,23783,34348,30089,36428,27977,34316,15363,30121,25896,34315,25928,25895,28040,28040,36492,34347,25960,28008,34379,36460,40654,28008,

25865,30090,30091,32204,36430,23720,15300,30026,44817,30026,25833,32139,30091,36397,32204,30091,34316,40687,23751,32203,25864,34348,34348,30090,17412,27977,38542,38542,34316,30058,15300,34317,34316,23752,19558,27978,19526,25864,17412,30090,19525,30090,32236,36430,19558,13219,30090,40623,40655,21638,38510,25831,32202,25896,25928,30154,32235,28009,23783,34315,23783,38574,27944,27976,34315,28009,17444,34348,19525,30090,23815,32235,30154,19557,40687,28009,19589,25864,15331,30090,28009,19525,25864,19557,32235,30122,17444,25864,32203,36429,25864,32236,32236,30122,19525,11106,23751,38542,36396,44881,30090,42768,36461,17444,38574,19557,32235,30122,38542,36428,38542,15266,27944,42735,36429,28009,34316,30090,40688,34317,25897,32203,42768,28009,34316,38574,34348,27976,36461,34347,30154,23750,34347,32234,23782,19620,34346,38605,30185,38573,30121,36492,40686,25928,27976,28009,30122,30058,30058,30090,30090,40687,42768,32203,21637,27976,28009,38574,32202,27976,42800,30089,21638,25831,25896,36429,25896,25896,40654,36460,30089,36428,34348,23815,30155,32235,30155,28041,21702,32267,30122,32267,34316,32235,28009,38541,25863,27976,30121,30120,30121,25927,36492,34347,28040,23814,32266,23815,32266,23814,

36430,23751,32204,34284,32171,21639,38478,36333,32139,38446,32171,25832,32139,30059,19525,23752,34316,38575,25864,21671,21638,25864,25896,32235,15299,23750,36429,25897,17445,13219,21671,23719,25897,25832,30123,28010,27945,19558,30123,25897,36429,34349,34284,38542,25864,21639,25865,40623,21606,19525,17412,25864,38509,30122,25863,30154,32202,25896,25928,25863,25863,32235,40622,23751,23783,28009,17412,21638,21670,21670,23751,32235,23783,28009,34316,25864,19557,23783,21670,21702,23751,36429,32235,19557,30090,27977,32236,21638,32236,38542,25864,34316,34348,25896,13219,34348,32235,27977,34348,30090,21638,36396,42768,17412,42800,17412,23783,42800,40687,44880,40654,19525,34316,42768,32170,36396,25864,25864,34317,30090,21639,32236,42768,34348,38574,36493,36428,23783,44912,28009,30121,19556,36428,32234,32266,36492,40685,40685,36492,38637,28008,34379,36493,28008,30089,34316,30090,30058,25832,30090,23783,30154,34348,25864,30154,32235,25896,38541,32234,36460,36461,21670,34348,27976,30089,34283,32234,40687,34348,25863,23815,32202,36493,25928,34380,38607,28009,23783,28041,25928,36493,32202,38574,42735,28009,32235,32202,30121,28041,28008,32234,28008,25927,34347,38605,28008,32266,21669,34347,30121,

25865,23719,42736,32172,38543,19526,25833,29994,30026,36398,34284,42704,25865,34284,6848,13154,17380,36429,28010,19525,38542,21670,21670,32202,32202,30089,19525,23783,11105,11073,32204,25832,25897,23752,25865,34317,25865,30123,32268,34316,30123,28010,32236,34317,34317,19526,19493,30058,25864,15299,15299,23718,38541,21637,17476,30154,30122,28009,21670,30089,30090,25864,32203,44848,17379,30090,21638,27977,32236,21638,19589,38574,23815,34380,23783,25896,19557,17476,28009,25864,21670,38542,23815,23815,28041,32267,32203,19557,28009,38542,21638,23751,25864,30123,30123,28009,32171,30090,34284,27977,30058,40655,40655,11073,36461,23751,32203,38574,36428,38541,40687,36428,34316,30090,23751,42735,27977,32171,34349,38543,27945,30091,36429,32235,38574,32202,36460,34347,42831,23815,38573,15331,34380,38573,17475,38572,42831,23814,32266,23782,21701,40718,28008,23815,30122,28009,25832,23751,17412,30058,11073,23816,25896,25928,36461,40687,25896,36461,38574,23815,32170,27976,23751,23751,36428,30057,34283,32202,32234,25863,21637,28009,36494,23815,30122,30155,25928,25896,30154,30122,38574,32235,38510,44881,23751,34315,34347,23782,25927,30121,21701,32233,25927,23814,30153,21669,30154,21702,38572,40653,

27945,32203,32204,23752,30091,15235,19494,27881,34252,25800,19493,32204,36430,38543,17412,21639,21638,34284,25897,21671,32203,25896,30089,25928,32235,38574,8992,21670,13218,23783,30090,32236,8993,13187,23752,38510,28010,38543,23784,34316,21639,34349,28010,34349,36462,21671,19525,34316,27977,8960,23718,34315,36428,25863,23783,15363,21

702,21669,25928,19589,32235,40655,30090,30089,30057,34316,15331,27977,19557,19525,280
09,36428,36428,28041,19557,32235,34380,21702,32267,30122,23783,32235,32267,32235,3223
5,28009,32203,25864,32236,42768,30090,32203,40655,40623,38542,30090,32235,25832,27945
,36429,27977,36429,40687,11105,21670,30122,38542,38541,32202,27976,36461,28009,42832,
17412,30089,36461,30058,30122,30091,40656,34349,25864,36461,36461,25928,34380,25895,3
4379,32267,30154,38606,23783,32203,34380,21669,40718,38573,28040,23782,25927,17443,34
379,15362,17476,36461,25863,32203,36429,21606,30090,23751,25896,28009,28041,36461,322
35,30089,40654,40687,30089,40654,34283,19525,23783,36428,42735,34283,32235,30121,2586
3,25896,21637,19589,17476,21670,19589,28041,34348,25928,32235,34348,28009,32235,30090
,27977,34283,23783,25895,25895,23814,36492,36460,30121,25895,34347,23782,34379,28008,
36460,40718,

30091,30090,23687,25832,21606,6848,27913,32139,19462,23655,27978,23752,30058,385
75,23751,19525,32236,30090,17412,21638,17412,32203,30122,32202,21670,32267,21670,3012
2,23815,40687,28010,23784,13186,25864,23784,38510,23752,21606,25833,21639,21639,32171
,25865,40623,25832,17412,17412,42768,25896,15331,32203,32235,30122,34348,21670,23750,
19524,36461,28041,23783,25864,34348,32203,21670,27977,28009,38574,32235,17444,25896,3
4315,42767,38606,23750,32235,36525,28073,30186,30155,32235,38574,30154,23784,28009,23
784,38542,30090,32236,28009,38542,44848,32171,40622,44849,30090,36397,23751,25865,195
26,34349,27945,38542,42800,17412,34315,23815,32202,40687,25863,32267,32202,25928,2592
8,19557,28009,30090,34315,23751,27977,36397,32171,17412,30090,32202,17444,32267,23783
,28009,36461,34380,28009,30090,17444,34348,30154,32234,32202,34380,21637,36460,17475,
23814,15297,32202,32234,34315,34380,38574,27977,23783,30122,34316,36461,32235,38541,2
5896,34316,36461,28009,34315,36461,30122,32202,25896,28008,38541,36461,34380,25895,25
895,32267,15363,15330,21702,23783,25928,38574,32267,28009,32267,34381,27977,27976,321
70,30089,25863,21637,23750,32202,17411,34380,36460,28041,32266,32234,30121,28073,1962
1,34379,40751,

36397,30090,34317,25832,27946,36398,36398,19494,21542,17348,25865,21639,23751,13
187,17412,21671,34316,34348,11041,23783,30090,23751,30090,21637,21670,23815,28009,237
83,32235,36493,21638,34316,34284,32203,19526,23752,17381,23752,30059,30058,25865,2372
0,25865,23719,13186,8960,27945,34284,23751,23751,36461,17412,30089,27977,32235,34380,
28009,30154,38541,25928,25928,28041,23783,13186,23783,32235,32203,38542,17444,25896,2
7976,30089,25896,25863,34380,25961,21702,23815,40719,34380,28042,25896,32235,27977,34
317,25897,25897,30123,27945,38574,38510,30057,46962,38510,34284,30090,21574,17413,343
16,28010,21638,34316,30090,34315,40687,30089,30122,36493,34347,34347,28041,21702,2589
5,32235,30122,21702,27976,30154,21638,36429,34316,15299,23783,19557,21670,32203,30090
,30122,27976,36429,36429,42800,27977,32235,21670,32235,34315,28008,13217,36428,19524,
21669,25862,42766,36460,42799,36460,36461,25863,21670,25864,38542,36429,34348,36461,3
0122,36461,25864,17444,34348,34315,34315,40654,30089,32235,30154,25928,32267,23782,30
154,32267,30121,17476,30121,34347,30121,32267,25928,30154,25928,32235,17476,27976,406
22,34315,23718,32202,30057,36460,13218,36428,36460,23782,25928,28008,36460,23814,2589
5,28073,40718,

27978,34284,36430,23720,17381,36398,38511,32139,30059,15268,30058,13187,4736,153
00,25897,25897,30090,40687,21606,30058,23719,19492,38574,17444,21702,23783,30122,3009
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};
```

edge_calculation.py

```
import csv



ins=open('clock_white.txt','r')
temp = csv.reader(ins)
f=open('clock_white_result.txt','w')
count = 0
for line in temp:
      for element in line:
            if element =='0':
                  res = 'clock_white_result[ '+str(count)+' ]<=0;\n';
                  f.write(res)
                  count = count +1
            elif element =='1':
                  res = 'clock_white_result[ '+str(count)+' ]<=1;\n';
                  f.write(res)
                  count = count +1


f.close()
```

edge_cal_2.py

```
#!/user/bin/env python
f = open("evil.txt","r")
lines = f.readlines()
r = open("resEvil.txt","w")
counter = 0
Cnt =-1
```

```
lineCnt = -1
flag = "0"
outStr = ""
for line in lines:
    lineCnt = lineCnt +1
    print lineCnt
    x = line.split(",")
    Cnt =-1
    flag = "0"
    outStr = ""
    for y in x:
        Cnt = Cnt +1
        if(y=="65535" and flag =="0"):
            counter = counter +1
            flag ="1"
        elif(flag == "1" and y!="65535"):
#             print lineCnt
#             print "-firstone-"
#             print Cnt
            flag = "2"
            outStr = outStr + str(lineCnt)+", start: ," + str(Cnt) +","
        elif(flag == "2" and y=="65535"):
#             print lineCnt
#             print "-secondone-"
#             print Cnt
            flag = "0"
            outStr = outStr + str(lineCnt)+", end: ," + str(Cnt) +","
    outStr = outStr + "\n"
    r.write(outStr)
f.close()
```

image_convert.m

```
%Jian LU 16bit color map conversion

X = imread('oops','jpg');

height = 50;

width = 100;

[Y,map] = rgb2ind(X,65536);

R = X(:,:,1);

G = X(:,:,2);

B = X(:,:,3);



R1 = bitshift(R,-3);

G1 = bitshift(G,-2);
```

```
B1 = bitshift(B,-3);


% NEW(:,:,1)= R1;
% NEW(:,:,2)= G1;
% NEW(:,:,3)= B1;
%
% image(NEW);




OUTPUT = uint16(R1)*2^11 + uint16(G1)*2^5 + uint16(B1);


dlmwrite('oops.txt',OUTPUT);


R2 = reshape(uint8(bitshift(bitshift(OUTPUT,0),-11)),height,width);
G2 = reshape(uint8(bitshift(bitshift(OUTPUT,5),-10)),height,width);
B2 = reshape(uint8(bitshift(bitshift(OUTPUT,11),-11)),height,width);


NEW(:,:,1)= bitshift(R2,3);
NEW(:,:,2)= bitshift(G2,2);
NEW(:,:,3)= bitshift(B2,3);


image(NEW);
%
% R1 = bitand(R,hex2dec('1f'));
% G1 = bitand(G,hex2dec('3f'));
% B1 = bitand(B,hex2dec('1f'));
%
% NEW(:,:,1)= R1;
```

```
% NEW(:,:,2)= G1;

% NEW(:,:,3)= B1;

%

% image(NEW);
```