# CSEE W3827

## Fundamentals of Computer Systems

## Homework Assignment 6

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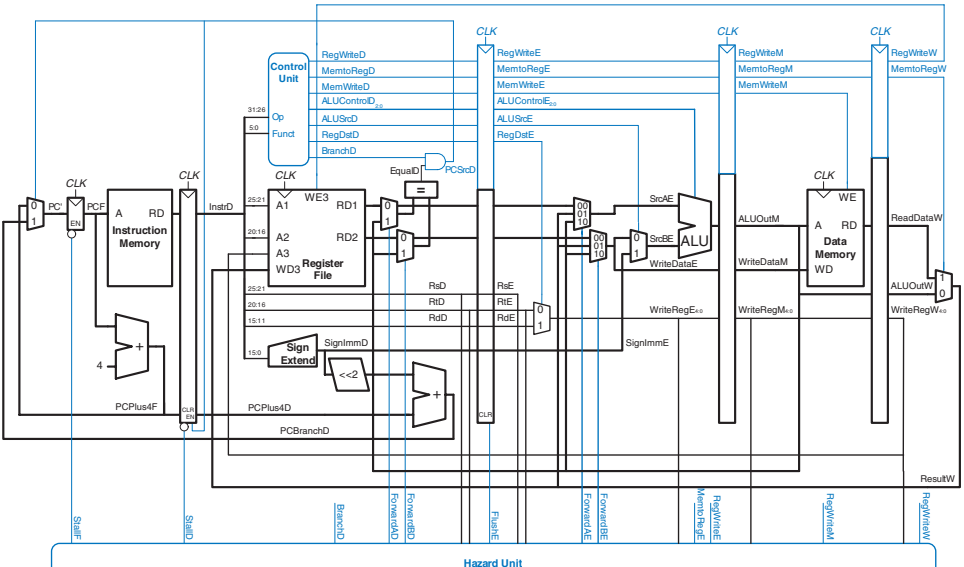
Columbia University

Due December 6th, 2011 at 10:35 AM

Show your work for each problem; we are more interested in how you get your answer than whether you get the right answer.

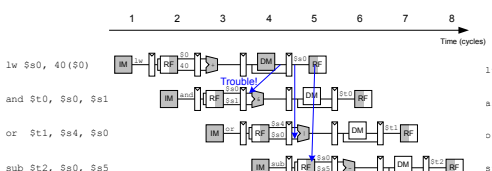



The fully bypassed five-stage (F, D, E, M, W) MIPS pipeline with stall logic

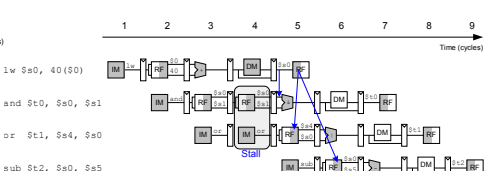
1. (30 pts.) For the five-stage MIPS pipeline with full bypass and stall logic discussed in class, in the book, and included in this assignment, explain the hazard, if any, in each sequence of code below and explain how the processor will resolve it, e.g., “stall two cycles,” “bypass W to E,” “bypass M to D.” The stages are abbreviated F, D, E, M, and W (Fetch, Decode, Execute, Memory, and Writeback). For one example from the slides,

```
lw  $s0, 40($0)
and $t0, $s0, $s1
or  $t1, $s4, $s0
sub $t2, $s0, $s5
```

The *and* must stall a cycle then use a W-to-E bypass to get $s0.
The *or* is already in the pipeline when the *and* stalls, so it, too, must stall.




Hazard Illustrated




Resolution of Hazard

```
   lw  $t1, 42($t1)
(a) add $t2, $t1, $t3
   sub $t4, $t1, $t3


   lw  $t1, 42($t1)
(b) add $t4, $t2, $t3
   sub $t5, $t2, $t3


   add $t1, $t2, $t3
(c) add $t1, $t1, $t4
   add $t1, $t1, $t5


   lw  $t1, 42($t1)
(d) add $t3, $t2, $t3
   sub $t4, $t1, $t3
```

2. (30 pts.) Consider the following fragment of MIPS code:

```
        li    $t0, 64
loop:   lw    $t1, 0($t2)
        sw    $t1, 0($t3)
        addiu $t2, $t2, 4
        addiu $t3, $t3, 4
        subu  $t0, $t0, 1
        bnez  $t0, loop
```

(a) When this code fragment is run, how many instructions will be executed total?

(b) How many cycles will it take to execute on the fully bypassed MIPS processor?

Now, consider this fragment of code:

```
        li    $t0, 64
loop:   subu  $t0, $t0, 1
        lw    $t1, 0($t2)
        addiu $t2, $t2, 4
        sw    $t1, ($t3)
        addiu $t3, $t3, 4
        bnez  $t0, loop
```

(c) When this code fragment is run, how many instructions will be executed total?

(d) How many cycles will it take to execute on the fully bypassed MIPS processor?

3. (25 pts.) Consider a computer with a *direct mapped* cache of 64 16-byte blocks backed by $2^{24}$ bytes of main memory.

   (a) How many blocks does main memory contain?

   (b) How are memory addresses interpreted, i.e., how many bits each are the tag, set, and byte offset fields?

   (c) To which cache set will the address `0xDECADE` map?

(d) Assuming the cache starts empty, what sequence of events would be produced by reading bytes in the following sequences of addresses? Classify each event as a compulsory miss, a conflict miss, a spatial locality hit, or a temporal locality hit.

| Address | Event |
|---|---|
| 0xDECADE | |
| 0xDECAD8 | |
| 0xDECAE8 | |
| 0xBECADE | |
| 0xDECADE | |

4. (15 pts.) Consider a computer with a *fully associative* cache of 32 64-byte blocks backed by $2^{16}$ bytes of main memory.

   (a) How many blocks does main memory contain?

   (b) How are memory addresses interpreted, i.e., how many bits each are the tag, set, and byte offset fields?

   (c) To which cache set will the address `0xF00D` map?