# Fundamentals of Computer Systems Boolean Logic

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#### **Boolean Logic**

AN INVESTIGATION

OF

#### THE LAWS OF THOUGHT,

ON WHICH ARE FOUNDED

THE MATHEMATICAL THEORIES OF LOGIC AND PROBABILITIES.

BY

GEORGE BOOLE, LL.D.



George Boole 1815–1864

LONDON:

WALTON AND MABERLY,

#### UPPEE GOWER-STREET, AND IVY-LANE, PATERNOSTER-ROW.

CAMBRIDGE: MACMILLAN AND CO.

# Boole's Intuition Behind Boolean Logic

Variables x, y, ... represent classes of things No imprecision: A thing either is or is not in a class

If x is "sheep" and y is "white things," xy are all white sheep,

xy = yx

and

If x is "men" and y is "women," x + y is "both men and women,"

x + y = y + x

and

XX = X.

z(x+y)=zx+zy.

X + X = X.

If x is "men," y is "women," and z is "European," z(x+y) is "European men and women" and

# The Axioms of (Any) Boolean Algebra

A Boolean Algebra consists of

A set of values A An "and" operator ∧ An "or" operator ∨ A "not" operator ¬

- A "false" value  $0 \in A$
- A "true" value  $1 \in A$

# The Axioms of (Any) Boolean Algebra

A Boolean Algebra consists of	F
A set of values $A$ An "and" operator $\land$ An "or" operator $\lor$	A "not" operator $\neg$ A "false" value $0 \in A$ A "true" value $1 \in A$
Axi	oms
$a \lor b = b \lor a$	$a \wedge b = b \wedge a$
$a \lor (b \lor c) = (a \lor b) \lor c$	$a \land (b \land c) = (a \land b) \land c$
$a \lor (a \land b) = a$	$a \land (a \lor b) = a$
$a \land (b \lor c) = (a \land b) \lor (a \land c)$	$a \lor (b \land c) = (a \lor b) \land (a \lor c)$
$a \lor \neg a = 1$	$a \wedge \neg a = 0$

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We will use the first non-trivial Boolean Algebra:  $A = \{0, 1\}$ . This adds the law of excluded middle: if  $a \neq 0$  then a = 1 and if  $a \neq 1$  then a = 0.

"You are a New Yorker if you were born in New York or were not born in New York and lived here ten years."

Axioms
$a \lor b = b \lor a$
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$a \land (a \lor b) = a$
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$a \lor (b \land c) = (a \lor b) \land (a \lor c)$
$a \vee \neg a = 1$
$a \wedge \neg a = 0$

$$x \wedge 1 = x \wedge (x \vee \neg x)$$
  
=  $x \wedge (x \vee y)$  if  $y = \neg x$   
=  $x$ 

$$x \lor ((\neg x) \land y)$$

х

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	$a \land (b \land c) = (a \land b) \land c$
$V\left( (-\mathbf{x}) \wedge V \right)$	$a \lor (a \land b) = a$
$\mathbf{v} \left( \left( \mathbf{x} \right) \times \mathbf{y} \right)$	$a \land (a \lor b) = a$
$-(\mathbf{x}\mathbf{y}(-\mathbf{x})) \wedge (\mathbf{x}\mathbf{y}\mathbf{y})$	$a \land (b \lor c) = (a \land b) \lor (a \land c)$
$= (x \circ (x)) \land (x \circ y)$	$a \lor (b \land c) = (a \lor b) \land (a \lor c)$
	$a \lor \neg a = 1$
	<i>a</i> ∧ ¬ <i>a</i> = 0

$$x \wedge 1 = x \wedge (x \vee \neg x)$$
  
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	$a \land (b \land c) = (a \land b) \land c$
$\mathbf{x} \vee ((\neg \mathbf{x}) \wedge \mathbf{y})$	$a \lor (a \land b) = a$
	$a \land (a \lor b) = a$
$-(\mathbf{x} \vee (\neg \mathbf{x})) \wedge (\mathbf{x} \vee \mathbf{x})$	$a \land (b \lor c) = (a \land b) \lor (a \land c)$
$= \left( \mathbf{x} \cdot (\mathbf{x}) \right) \times (\mathbf{x} \cdot \mathbf{y})$	$a \lor (b \land c) = (a \lor b) \land (a \lor c)$
$= 1 \wedge (x \vee y)$	$a \lor \neg a = 1$
	<i>a</i> ∧ ¬ <i>a</i> = 0

$$x \wedge 1 = x \wedge (x \vee \neg x)$$
  
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$$x \wedge 1 = x \wedge (x \vee \neg x)$$
  
=  $x \wedge (x \vee y)$  if  $y = \neg x$   
=  $x$ 

### What Does This Have To Do With Logic Circuits?

A SYMBOLIC ANALYSIS OF RELAY AND SWITCHING CIRCUITS

ЪУ

Claude Elwood Shannon B.S., University of Michigan 1956

Submitten in Partial Fulfillment of the Requirements for the Degree of MASTER OF SOLENCE from the Massachusetts Institute of Technology 1940

Signature of Author

Department of Electrical Engineering, August 10, 1937

Signature of Professor in Charge of Research\_\_\_\_\_

Signature of Chairman of Department Committee on Graduate Students\_\_\_\_\_



Claude Shannon 1916–2001

# Shannon's MS Thesis

"We shall limit our treatment to circuits containing only relay contacts and switches, and therefore at any given time the circuit between any two terminals must be either open (infinite impedance) or closed (zero impedance).





### Shannon's MS Thesis



"It is evident that with the above definitions the following postulates hold.

$0 \cdot 0 = 0$	A closed circuit in parallel with a closed circuit is a closed circuit.
1 + 1 = 1	An open circuit in series with an open circuit is an open circuit.
1 + 0 = 0 + 1 = 1	An open circuit in series with a closed circuit in either order is an open circuit.
$0 \cdot 1 = 1 \cdot 0 = 0$	A closed circuit in parallel with an open circuit in either order is an closed circuit.
0 + 0 = 0	A closed circuit in series with a closed circuit is a closed circuit.
$1 \cdot 1 = 1$	An open circuit in parallel with an open circuit is an open circuit.
	At any give time either $X = 0$ or $X = 1$

# Alternate Notations for Boolean Logic

Operator	Math	Engineer	Schematic
Сору	x	X	$x-$ or $x- \longrightarrow x$
Complement	¬ <i>x</i>	$\overline{X}$	x
AND	<i>x</i> ∧ <i>y</i>	$XY$ or $X \cdot Y$	
OR	<i>x</i> ∨ <i>y</i>	X + Y	

# Definitions

*Literal*: a Boolean variable or its complement

E.g., 
$$X \quad \overline{X} \quad Y \quad \overline{Y}$$

Implicant: A product of literals

E.g., X XY 
$$X\overline{Y}Z$$

Minterm: An implicant with each variable once

E.g.,  $X\overline{Y}Z$  XYZ  $\overline{X}\overline{Y}Z$ 

Maxterm: A sum of literals with each variable once

E.g.,  $X + \overline{Y} + Z$  X + Y + Z  $\overline{X} + \overline{Y} + Z$ 

#### Be Careful with Bars

#### $\overline{X}\overline{Y} \neq \overline{XY}$

Let's check all the combinations of X and Y:

X	Y	$\overline{X}$	Ŷ	$\overline{X} \cdot \overline{Y}$	XY	XΥ
0	0	1	1	1	0	1
0	1	1	0	0	0	1
1	0	0	1	0	0	1
1	1	0	0	0	1	0

# **Truth Tables**

A *truth table* is a canonical representation of a Boolean function

X	Y	Minterm	Maxterm	$\overline{X}$	XY	$\overline{XY}$	X + Y	$\overline{X+Y}$
0	0	$\overline{X}\overline{Y}$	X + Y	1	0	1	0	1
0	1	XΥ	$X+\overline{Y}$	1	0	1	1	0
1	0	XY	$\overline{X} + Y$	0	0	1	1	0
1	1	XY	$\overline{X} + \overline{Y}$	0	1	0	1	0

Each row has a unique minterm and maxterm

The  $\begin{array}{c} \mbox{minterm is 1} \\ \mbox{maxterm is 0} \end{array}$  for only its row

# Sum-of-minterms and Product-of-maxterms

Two mechanical ways to translate a function's truth table into an expression:

X	Y	Minterm	Maxterm	F
0	0	$\overline{X}\overline{Y}$	X + Y	0
0	1	ΧY	$X + \overline{Y}$	1
1	0	XY	$\overline{X} + Y$	1
1	1	XY	$\overline{X} + \overline{Y}$	0

The sum of the minterms where the function is 1:

$$F = \overline{X}Y + X\overline{Y}$$

The product of the maxterms where the function is 0:

$$F = (X + Y)(\overline{X} + \overline{Y})$$

$$F = \overline{X}Y + X\overline{Y}$$



$$F = \overline{X}Y + X\overline{Y}$$



$$F = \overline{X}Y + X\overline{Y}$$



$$F = \overline{X}Y + X\overline{Y}$$



$$F = \overline{X}Y + X\overline{Y}$$



$$F = \overline{X}Y + X\overline{Y} = (X + Y)(\overline{X} + \overline{Y})$$



# Minterms and Maxterms: Another Example

The minterm and maxterm representation of functions may look very different:

X	Y	Minterm	Maxterm	F
0	0	$\overline{X}\overline{Y}$	X + Y	0
0	1	ΧY	$X + \overline{Y}$	1
1	0	XY	$\overline{X} + Y$	1
1	1	XY	$\overline{X} + \overline{Y}$	1

The sum of the minterms where the function is 1:

$$F = \overline{X}Y + X\overline{Y} + XY$$

The product of the maxterms where the function is 0:

$$F = X + Y$$

$$F = \overline{X}Y + X\overline{Y} + XY = X + Y$$



# The Menagerie of Gates





# De Morgan's Theorem

$$\neg (a \lor b) = (\neg a) \land (\neg b)$$
  $\neg (a \land b) = (\neg a) \lor (\neg b)$ 

Proof by Truth Table:

а	b	$a \lor b$	$(\neg a) \land (\neg b)$	a∧b	$(\neg a) \lor (\neg b)$
0	0	0	1	0	1
0	1	1	0	0	1
1	0	1	0	0	1
1	1	1	0	1	0

# De Morgan's Theorem in Gates



$$\overline{A+B} = \overline{A} \cdot \overline{B}$$



# **Bubble Pushing**



Apply De Morgan's Theorem:

Transform NAND into OR with inverted inputs

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Two bubbles on a wire cancel

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Apply De Morgan's Theorem:

Transform NAND into OR with inverted inputs

Two bubbles on a wire cancel

# PONG





#### PONG, Atari 1973

Built from TTL logic gates; no computer, no software

Launched the video arcade game revolution

М	L	R	Α	В
0	0	0	Х	Х
0	0	1	0	1
0	1	0	0	1
0	1	1	Х	Х
1	0	0	Х	Х
1	0	1	1	0
1	1	0	1	1
1	1	1	Х	Х

The ball moves either left or right.

Part of the control circuit has three inputs: *M* ("move"), *L* ("left"), and *R* ("right").

It produces two outputs A and B.

Here, "X" means "I don't care what the output is; I never expect this input combination to occur."

L	R	Α	В
0	0	0	0
0	1	0	1
1	0	0	1
1	1	0	0
0	0	0	0
0	1	1	0
1	0	1	1
1	1	0	0
	L 0 1 1 0 0 1 1 1	L R   0 0   1 0   1 1   0 0   0 1   1 0   1 1   0 1   1 0   1 1   1 1	L R A   0 0 0   0 1 0   1 0 0   1 1 0   0 0 0   0 1 1   1 0 1   1 0 1   1 1 0

- E.g., assume all the X's are 0's and use Minterms:
- $A = M\overline{L}R + ML\overline{R}$

$$B = \overline{M}\,\overline{L}R + \overline{M}\,L\overline{R} + ML\overline{R}$$

3 inv + 4 AND3 + 1 OR2 + 1 OR3

М	L	R	Α	В
0	0	0	1	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	1	1

Assume all the X's are 1's and use Maxterms:

$$A = (M + L + \overline{R})(M + \overline{L} + R)$$

$$B=\overline{M}+L+\overline{R}$$

М	L	R	Α	В
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	1	0

Choosing better values for the X's and being much more clever:

$$A = M$$

$$B = \overline{MR}$$

1 NAND2 (!)

Basic trick: put "similar" variable values near each other so simple functions are obvious

М	L	R	Α	В
0	0	0	Х	Х
0	0	1	0	1
0	1	0	0	1
0	1	1	Х	Х
1	0	0	Х	Х
1	0	1	1	0
1	1	0	1	1
1	1	1	Х	Х

The *M*'s are already arranged nicely

М	L	R		Α	В	
0	0	0		Х	Х	Let's rearrange the
0	0	1		0	1	L's by permuting two
0	1	0		0	1	pairs of rows
0	1	1		Х	Х	
1	0	0		Х	Х	
1	0	1		1	0	
			1	1	0	1 1
			1	1	1	X X

М	L	R	Α	В								
0	0	0	Х	Х	-	Let	's re	earran	ge the			
0	0	1	0	1		L's by permuting two pairs of rows						
0	1	0	0	1								
0	1	1	Х	Х								
1	0	0	Х	Х								
1	0	1	1	0								
					1	1	0	1	1			
					1	1	1	Х	Х			

М	L	R	Α	В						
0	0	0	Х	Х	Let	c's re	earran	ge the		
0	0	1	0	1	L's by permuting two pairs of rows					
0	1	0	0	1						
0	1	1	Х	Х						
1 1	0 0	0 1	X 1	X 0 1 1	. 1	0 1	1 X	1 X		

М	L	R	А	В						
0	0	0	Х	Х	Let	c's re	earran	ge th	e	
0	0	1	0	1	L's	by j	bermu	ting t	wo	
0	1	0	0	1	pairs of rows					
0	1	1	Х	Х						
1 1	0 0	0 1	X 1	x 1 0	1 1	0 1	1 X	1 X		

М	L	R	Α	В	_					
0	0	0	Х	Х	-	Let	's re	earran	ge the	е
0	0	1	0	1		L's	by j	permu	ting t	wo
0	1	0	0	1		pai	rs o	f rows		
0	1	1	Х	Х						
					1	1	0	1	1	
					1	1	1	Х	Х	
1	0	0	Х	Х						
1	0	1	1	0						

М	L	R	Α	В	_					
0	0	0	Х	Х	-	Let's ı	rearr	ange the		
0	0	1	0	1		L's by permuting two				
0	1	0	0	1	pairs of rows					
0	1	1	Х	Х						
			1	1	0	1	1			
			1	1	1	Х	Х			
1	0	0	Х	Х						
1	0	1	1	0						

М	L	R		Α	В	
0	0	0		Х	Х	Let's rearrange the
0	0	1		0	1	L's by permuting two
0	1	0		0	1	pairs of rows
0	1	1		Х	Х	
		1	1	0	1	1
		1	1	1	Х	Х
1	0	0		Х	Х	
1	0	1		1	0	

Basic trick: put "similar" variable values near each other so simple functions are obvious

М	L	R	Α	В
0	0	0	Х	Х
0	0	1	0	1
0	1	0	0	1
0	1	1	Х	Х
1	1	0	1	1
1	1	1	Х	Х
1	0	0	Х	Х
1	0	1	1	0

Let's rearrange the L's by permuting two pairs of rows

Basic trick: put "similar" variable values near each other so simple functions are obvious

М	L	R	Α	В
0	0	0	Х	Х
0	0	1	0	1
0	1	0	0	1
0	1	1	Х	Х
1	1	0	1	1
1	1	1	Х	Х
1	0	0	Х	Х
1	0	1	1	0

The *R*'s are really crazy; let's use the second dimension

Basic trick: put "similar" variable values near each other so simple functions are obvious



The *R*'s are really crazy; let's use the second dimension

М	L	R	Α	В	
00	00	01	X0	X1	The <i>R</i> 's are really
00	11	01	0 X	1 X	second dimension
11	11	01	1X	1 X	
11	00	01	X1	X0	



# Maurice Karnaugh's Maps The Map Method for Synthesis of Combinational Logic Circuits

#### M. KARNAUGH

NONMEMBER AIEE

THE SEARCH for simple abstract techniques to be applied to the design of switching systems is still, despite some recent advances, in its early stages. The problem in this area which has been attacked most energetically is that of the synthesis of efficient combinational that is, nonsequential, logic circuits. be convenient to describe other methods in terms of Boolean algebra. Whenever the term "algebra" is used in this paper, it will refer to Boolean algebra, where addition corresponds to the logical connective "or," while multiplication corresponds to "and."

The minimizing chart,2 developed at



Transactions of the AIEE, 1953

# The Seven-Segment Decoder Example









W	Х	Y	Ζ	а
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	Х
1	0	1	1	Х
1	1	0	0	Х
1	1	0	1	Х
1	1	1	0	Х
1	1	1	1	0

1011  $x \begin{cases} 0 & 1 & 1 & 1 \\ x & x & 0 & x \\ 1 & 1 & x & x \end{cases} w$ 

#### The Karnaugh Map Sum-of-Products Challenge

Cover all the 1's and none of the 0's using as few literals (gate inputs) as possible.

Few, large rectangles are good.

Covering X's is optional.

W	Х	Y	Ζ	а
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	Х
1	0	1	1	Х
1	1	0	0	Х
1	1	0	1	Х
1	1	1	0	Х
1	1	1	1	0



The minterm solution: cover each 1 with a single implicant.

$$a = \overline{W}\overline{X}\overline{Y}\overline{Z} + \overline{W}\overline{X}YZ + \overline{W}\overline{X}Y\overline{Z} + \overline{W}X\overline{Y}Z + \overline{W}XYZ + \overline{W}XY\overline{Z} + W\overline{X}\overline{Y}Z + W\overline{X}\overline{Y}Z$$

 $8 \times 4 = 32$  literals

4 inv + 8 AND4 + 1 OR8

W	Х	Y	Ζ	а
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	Х
1	0	1	1	Х
1	1	0	0	Х
1	1	0	1	Х
1	1	1	0	Х
1	1	1	1	0



Merging implicants helps Recall the distributive law: AB + AC = A(B + C)

$$a = \overline{W}\overline{X}\overline{Y}\overline{Z} + \overline{W}Y + \overline{W}XZ + W\overline{X}\overline{Y}$$

4 + 2 + 3 + 3 = 12 literals

4 inv + 1 AND4 + 2 AND3 + 1 AND2 + 1 OR4

W	Х	Y	Ζ	а
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	Х
1	0	1	1	Х
1	1	0	0	Х
1	1	0	1	Х
1	1	1	0	Х
1	1	1	1	0



Missed one: Remember this is actually a torus.

$$a = \overline{X}\overline{Y}\overline{Z} + \overline{W}Y + \overline{W}XZ + W\overline{X}\overline{Y}$$

3 + 2 + 3 + 3 = 11 literals

4 inv + 3 AND3 + 1 AND2 + 1 OR4

W	X	Y	Ζ	а
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	Х
1	0	1	1	Х
1	1	0	0	Х
1	1	0	1	Х
1	1	1	0	Х
1	1	1	1	0



Taking don't-cares into account, we can enlarge two implicants:

$$a = \overline{X}\overline{Z} + \overline{W}Y + \overline{W}XZ + W\overline{X}$$

2 + 2 + 3 + 2 = 9 literals

3 inv + 1 AND3 + 3 AND2 + 1 OR4

W	X	Y	Ζ	а
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	Х
1	0	1	1	Х
1	1	0	0	Х
1	1	0	1	Х
1	1	1	0	Х
1	1	1	1	0

W

Can also compute the complement of the function and invert the result.

Covering the 0's instead of the 1's:

$$\overline{a} = \overline{W}\overline{X}\overline{Y}Z + X\overline{Y}\overline{Z} + WY$$

 $\mathbf{4}+\mathbf{3}+\mathbf{2}=\mathbf{9} \text{ literals}$ 

5 inv + 1 AND4 + 1 AND3 + 1 AND2 + 1 OR3



7 1 Х Х 0 W

To display the score, PONG used a TTL chip with this solution in it:





 $WX\overline{Y}\overline{Z} + \overline{W}X\overline{Y}\overline{Z} + WX\overline{Y}\overline{Z} + WXY\overline{Z} + WXY\overline{Z} + WXYZ + WXYZ + WXYZ + WX\overline{Y}Z + WX\overline{Y}Z$ 

Factor out the W's



$$(W + \overline{W}) X \overline{Y} \overline{Z} + (W + \overline{W}) X Y \overline{Z} + (W + \overline{W}) X Y \overline{Z} + (W + \overline{W}) X \overline{Y} Z$$

Use the identities

$$W + \overline{W} = 1$$

and

$$1X = X.$$





#### Factor out the Y's



 $(\overline{Y} + Y) X \overline{Z} + (\overline{Y} + Y) X Z$ 

Apply the identities again







 $X(\overline{Z}+Z)$ 

Simplify





Done