

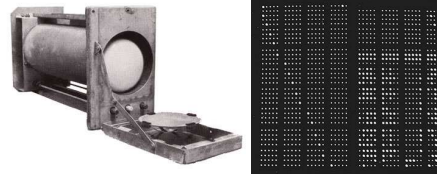
Memory

Prof. Stephen A. Edwards
sedwards@cs.columbia.edu

Columbia University
Spring 2006

Memory - p. 17

Early Memories



Williams Tube CRT-based random access memory, 1946. Used on the Manchester Mark I. 2048 bits.

Memory - p. 27

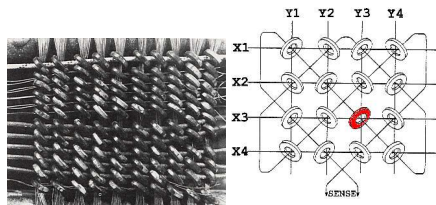
Early Memories



Mercury acoustic delay line. Used in the EDASC, 1947. 32×17 bits

Memory - p. 37

Early Memories



Magnetic core memory, 1952. IBM.

Memory - p. 47

Early Memories



Magnetic drum memory. 1950s & 60s. Secondary storage.

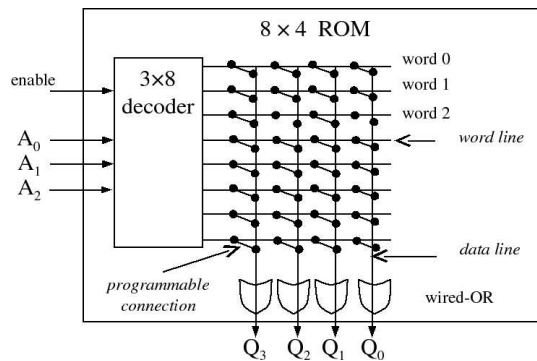
Memory - p. 57

Modern Memory Choices

Family	Programmed	Persistence
Mask ROM	at fabrication	∞
PROM	once	∞
EPROM	1000s, UV	10 years
FLASH	1000s, block	10 years
EEPROM	1000s, byte	10 years
NVRAM	∞	5 years
SRAM	∞	while powered
DRAM	∞	64 ms

Memory - p. 67

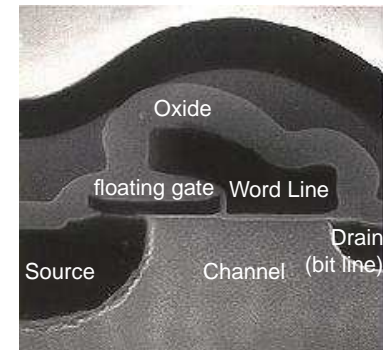
ROMs



EPROMs



EEPROM and FLASH



Slow write

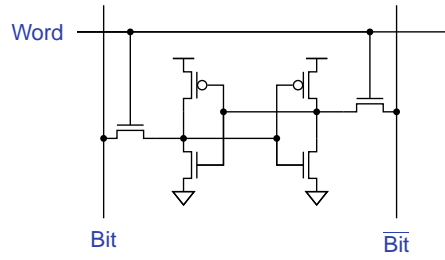
Fowler-Nordheim Tunneling

EEPROM: bit at a time

FLASH: block at a time

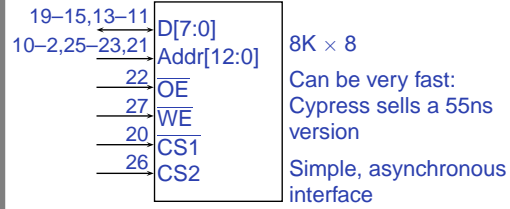
Source: SST

Static RAM Cell



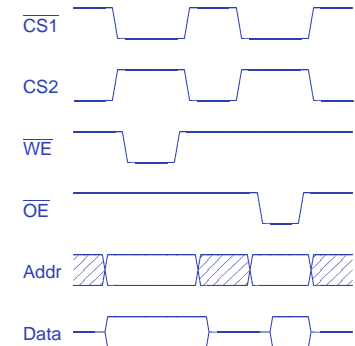
Memory - p.107

Standard SRAM: 6264



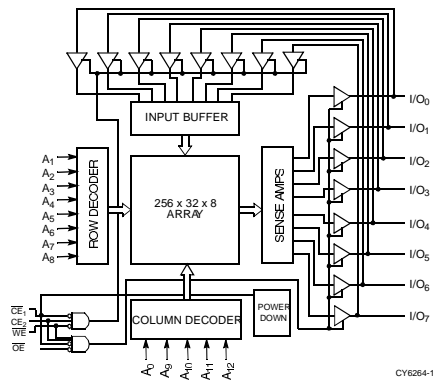
Memory - p.117

Standard SRAM: 6264



Memory - p.127

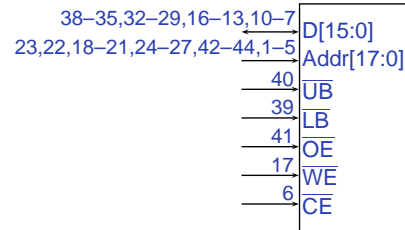
Standard SRAM: 6264



CY6264-1

Memory - p.137

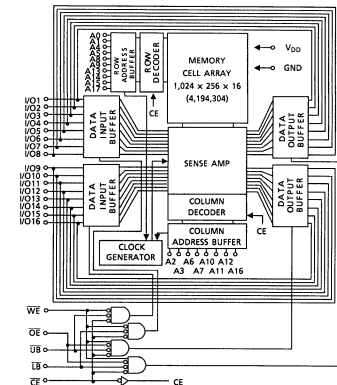
Toshiba TC55V16256J 256K x 16



12 or 15 ns access time
Asynchronous interface
UB, LB select bytes

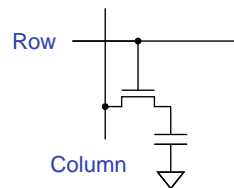
Memory - p.147

Toshiba TC55V16256J 256K x 16



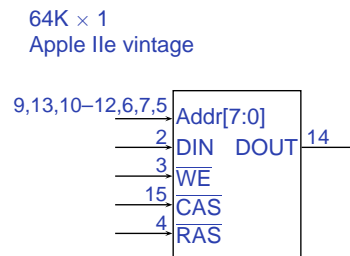
Memory - p.157

Dynamic RAM Cell

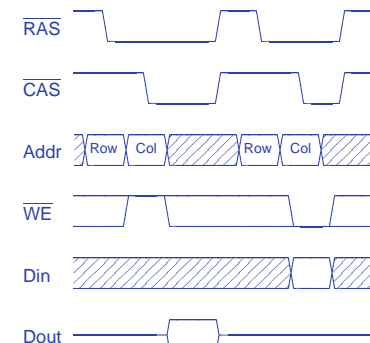


Basic problem: Leakage
Solution: Refresh

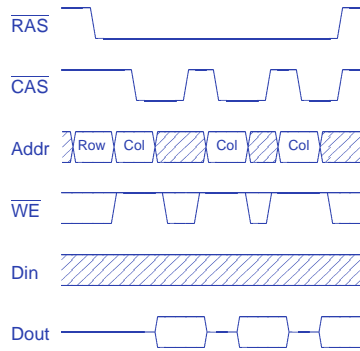
Ancient DRAM: 4164



Basic DRAM read and write cycles

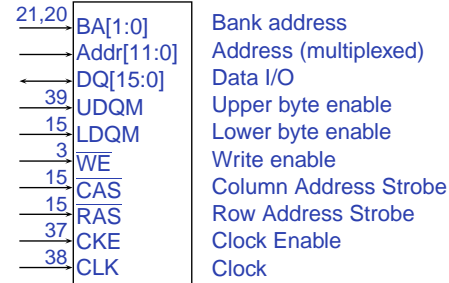


Page mode read cycle



Memory - p.197

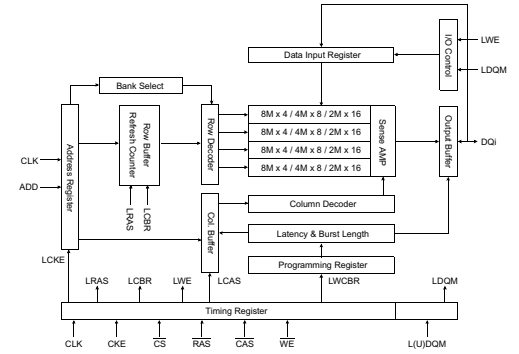
Samsung 8M × 16 SDRAM



Synchronous interface
Designed for burst-mode operation
Four separate banks; pipelined operation

Memory - p.207

Samsung 8M × 16 SDRAM



Memory - p.217

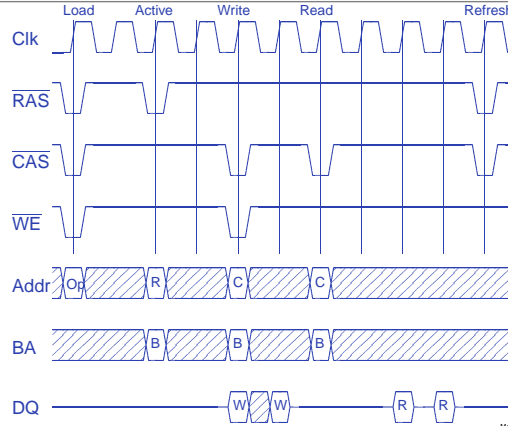
SDRAM: Control Signals

RAS	CAS	WE	action
1	1	1	NOP
0	0	0	Load mode register
0	1	1	Active (select row)
1	0	1	Read (select column, start burst)
1	0	0	Write (select column, start burst)
1	1	0	Terminate Burst
0	1	0	Precharge (deselect row)
0	0	1	Auto Refresh

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write

Memory - p.227

SDRAM: Timing with 2-word bursts



Memory - p.237