

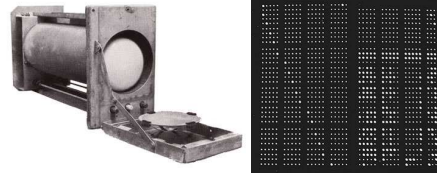
Memory

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NCTU, Summer 2005

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Early Memories



Williams Tube CRT-based random access memory, 1946. Used on the Manchester Mark I. 2048 bits.

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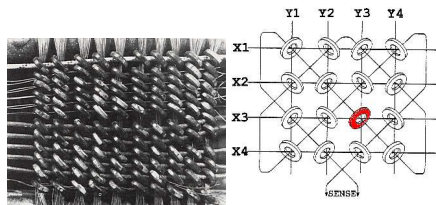
Early Memories



Mercury acoustic delay line. Used in the EDASC, 1947. 32 x 17 bits

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Early Memories



Magnetic core memory, 1952. IBM.

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Early Memories



Magnetic drum memory. 1950s & 60s. Secondary storage.

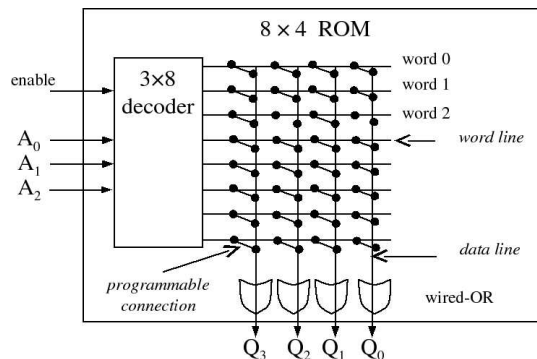
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Modern Memory Choices

Family	Programmed	Persistence
Mask ROM	at fabrication	∞
PROM	once	∞
EPROM	1000s, UV	10 years
FLASH	1000s, block	10 years
EEPROM	1000s, byte	10 years
NVRAM	∞	5 years
SRAM	∞	while powered
DRAM	∞	64 ms

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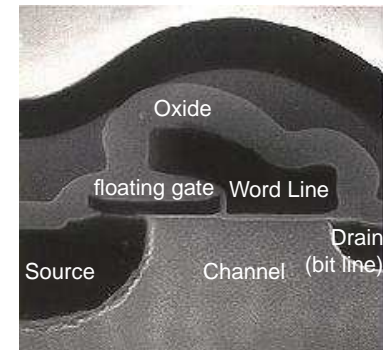
ROMs



EPROMs



EEPROM and FLASH



Slow write

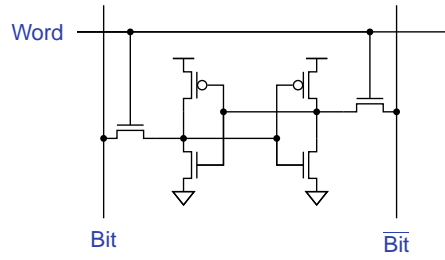
Fowler-Nordheim Tunneling

EEPROM: bit at a time

FLASH: block at a time

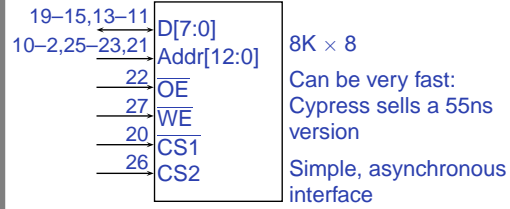
Source: SST

Static RAM Cell



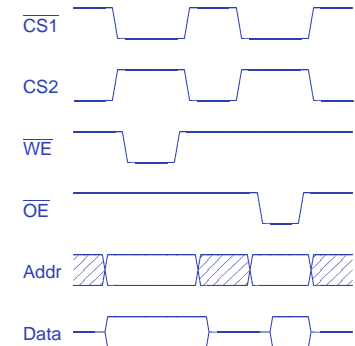
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Standard SRAM: 6264



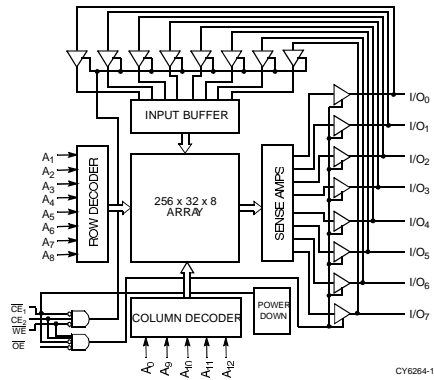
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Standard SRAM: 6264



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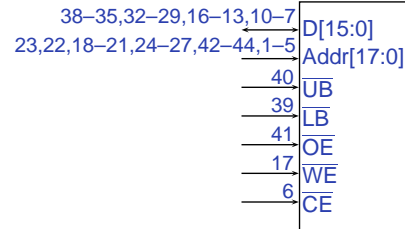
Standard SRAM: 6264



CY6264-1

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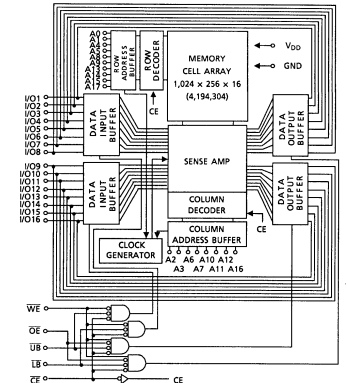
Toshiba TC55V16256J 256K x 16



12 or 15 ns access time
Asynchronous interface
UB, LB select bytes

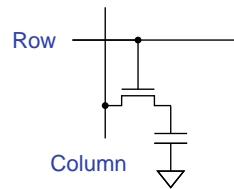
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Toshiba TC55V16256J 256K x 16



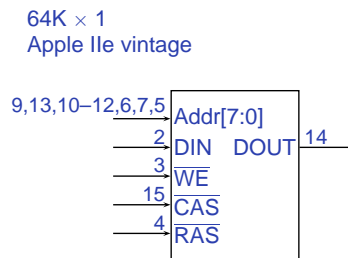
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Dynamic RAM Cell

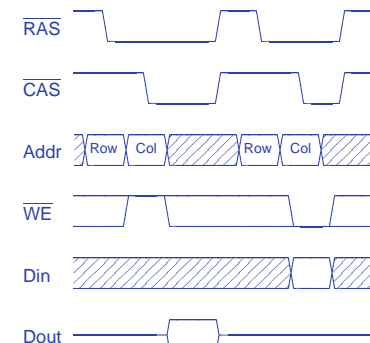


Basic problem: Leakage
Solution: Refresh

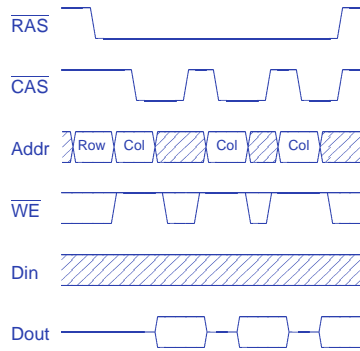
Ancient DRAM: 4164



Basic DRAM read and write cycles

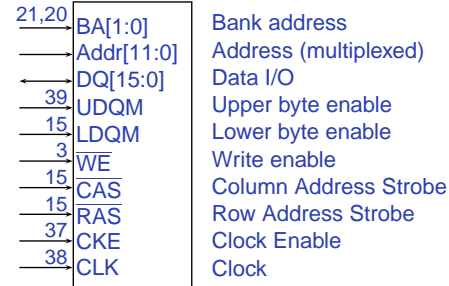


Page mode read cycle



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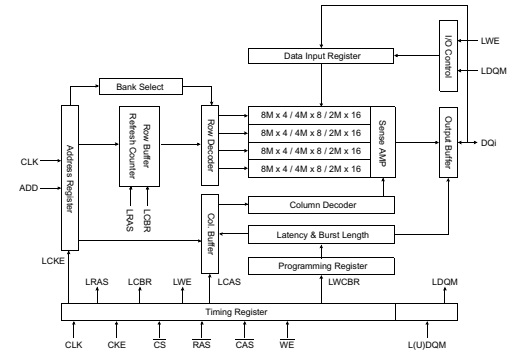
Samsung 8M × 16 SDRAM



Synchronous interface
Designed for burst-mode operation
Four separate banks; pipelined operation

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Samsung 8M × 16 SDRAM



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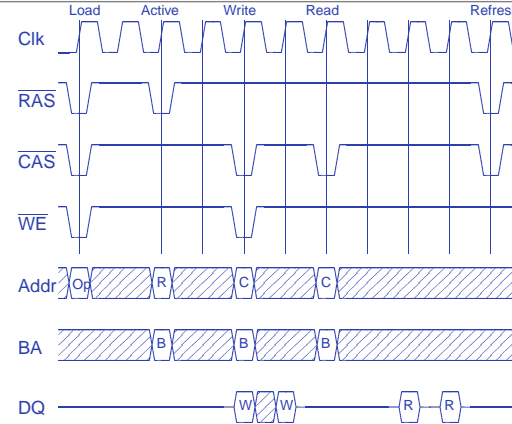
SDRAM: Control Signals

RAS	CAS	WE	action
1	1	1	NOP
0	0	0	Load mode register
0	1	1	Active (select row)
1	0	1	Read (select column, start burst)
1	0	0	Write (select column, start burst)
1	1	0	Terminate Burst
0	1	0	Precharge (deselect row)
0	0	1	Auto Refresh

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write

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SDRAM: Timing with 2-word bursts



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