CSEE W3827: Fundamentals of Computer Systems

Homework Assignment 2. Stephen Edwards. Columbia University

Due Sunday, May 23rd at 11:59 PM EDT via Courseworks

Put your answers in the dashed boxes provided and upload a PDF file to Courseworks. E.g., by editing it in Inkscape (`https://inkscape.org`) or printing and scanning. This assignment also requires you to use Digital, a logic simulator available at `https://github.com/hneemann/Digital`.

Name: Uni:

1. (25 pts.)

   A sequential circuit with two D flip-flops S_0 and S_1 and two inputs U and D behaves according to these equations:

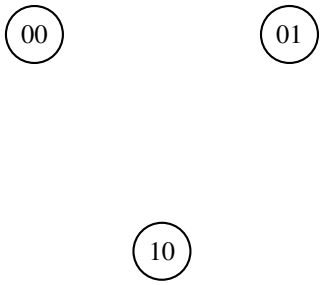
   $$S_0' = \overline{D}U\overline{S}_1\overline{S}_0 + \overline{D}\,\overline{U}S_0 + DS_1 \quad S_1' = D\overline{S}_1\overline{S}_0 + \overline{D}US_0 + \overline{D}\,\overline{U}S_1$$

   (a) Create this circuit in Digital by editing hw2-1.dig.

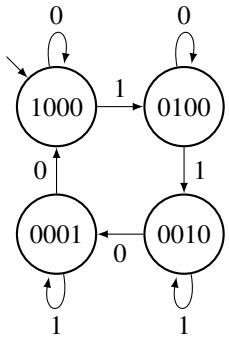
   (b) Complete its state table

DU	S_1S_0	S_1'	S_0'
00	00		
01	00		
10	00		
11	00		
00	01		
01	01		
10	01		
11	01		
00	10		
01	10		
10	10		
11	10		

   (c) Complete its bubble-and-arc diagram.

2. (20 pts.) Complete the circuit in hw2-2.dig to implement the following Moore state machine by just connecting wires. Do not add any other components.

3. (20 pts.) Use the PLA provided in hw2-3.dig to implement a decoder for the ''e'' and ''f'' segments of a seven-segment display by completing the Karnaugh maps below and connecting the appropriate wires to the inputs of all of the AND gates. Do not add or remove gates or change their number of inputs.

   e

X \ Z	1	0	0	1
0	0	0	0	1
X	X	X	0	X
1	0	0	X	X

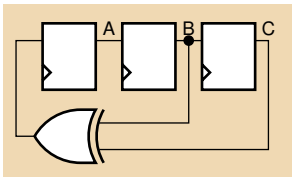
   W; Y

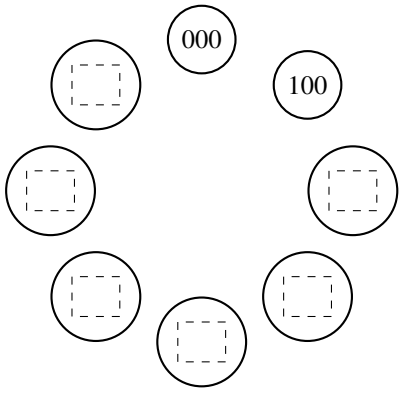
   f

X \ Z	1	0	0	0
1	1	1	0	1
X	X	X	0	X
1	1	1	X	X

   W; Y

4. (10 pts.) The circuit below is called a linear-feedback shift register. Fill in the bubble-and-arc diagram representing its behavior. Start from both the $ABC = 000$ and $ABC = 100$ states.

5. (25 pts.) Using MOSFET transistors (in Digital, N- and P-channel FETs under ''Switches''), build a static CMOS logic gate that computes $Y = AB + C$. Use only P-channel transistors in the pull-up network and only N-channel transistors in the pull-down network. Start from the skeleton in hw2-5.dig, which you may modify. We gave you an inverter to get started.