Fundamentals of Computer Systems

Review for the Final

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Summer 2021

The Final

48 hours: 12:00 AM EDT June 17 – 11:59 PM EDT June 18

Much like homework assignments, but with a range of simple to hard problems.

Open book, open notes, open Internet, closed classmates

Do the simple problems first, then work on the hard problems.

I want the average on this test to be low so I can curve it.

Download the .pdf file from Gradescope, edit it, and upload.

- Number Representation
  - Binary, Octal, Hex
  - One's, Two's Comp.
  - Fixed-point, BCD
- Boolean Logic
  - Axioms, Simplification
  - Implicants, Minterms
  - De Morgan's Theorem
  - Karnaugh Maps
- Combinational Logic
  - Decoders
  - Multiplexers
  - Timing and Glitches
  - Adders
- Sequential Logic
  - Bistables; SR, D Latches
  - D Flip-Flops
  - Synchronous Logic
  - Shift Registers
  - Counters
- Finite State Machines
  - Moore and Mealy Machines
  - The Snail Example
  - The TLC: One-Hot Encoding
- CMOS Logic Gates
  - The Inverter
  - The CMOS NAND Gate
  - The CMOS NOR Gate
  - A CMOS AND-OR-INVERT Gate
  - General Static CMOS Gates
- Memories
  - ROMs, EPROMs, FLASH
  - The SRAM Cell
  - Dynamic RAM Cell
  - PLAs

- MIPS Architecture/Assembly programming
  - Computational, Load/Store, & Control-flow Instrs.
  - Instruction Encoding
  - Pseudoinstructions
  - Calling Conventions
  - Higher-level constructs; subroutines and recursion
- MIPS Microarchitecture/Datapaths
  - Single-Cycle
    - The datapath for lw, sw, R-type, and branch
    - The controller: instruction decoding
    - Processor Performance
  - Pipelined
    - Basic pipelined datapath and control
    - Hazards: forwarding, stalling, and flushing
    - Performance Analysis

- The Memory Hierarchy: Caches
  - Memory hierarchy to make it fast & cheap
  - Temporal and Spatial Locality
  - Memory performance; hit rate
  - Direct-mapped caches
  - *n*-way set associative caches
  - Fully associative caches