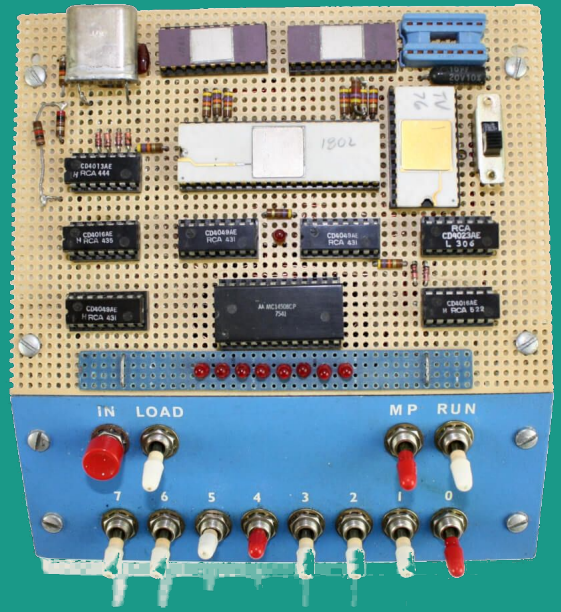

CDP1802 COSMAC Microprocessor

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Overview

- 1802 ISA, Memory, CPU
- Timing Diagrams
- Hardware-Software interface
- Testing & Debugging

ISA

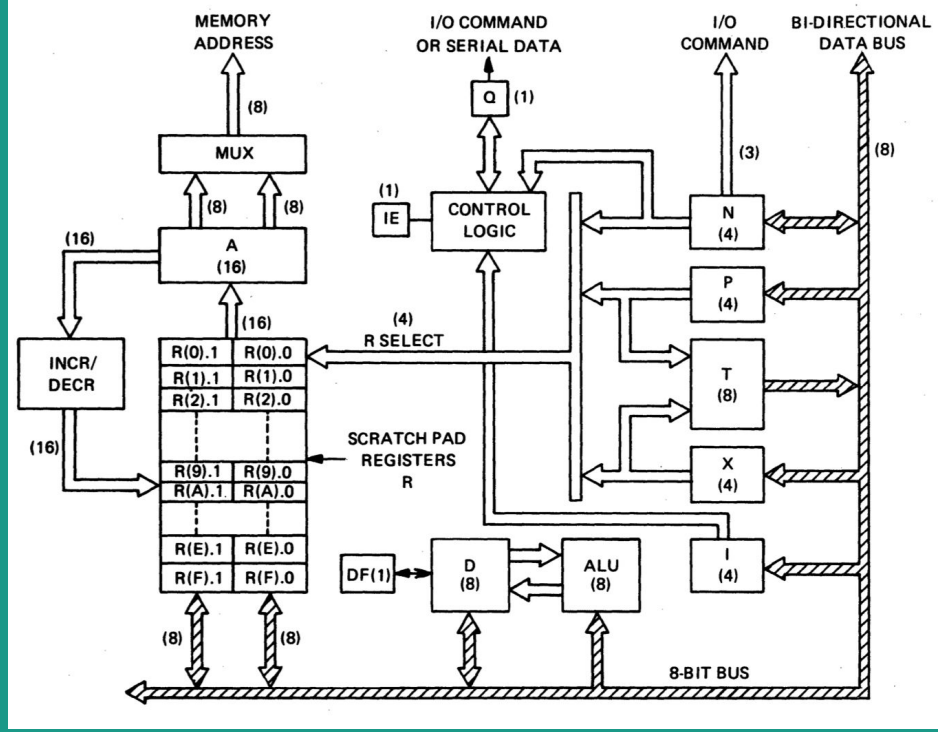
- Memory reference
- Register operations
- Logic operations
- Arithmetic operations
- Control flow (branch, long branch, skip, long skip)
- (I/O byte transfer) -- not implemented

1802 INSTRUCTION MATRIX

I \ N	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	IDL	LOAD VIA RN (LDN)														
1	INCREMENT RN (INC)															
2	DECREMENT RN (DEC)															
3	BRANCH ON Q, Z, DF				BRANCH ON EF1-EF4				BRANCH NOT ON Q, Z, DF				BRANCH NOT ON EF2-EF4			
4	LOAD-ADVANCE RN (LDA)															
5	STORE VIA RN (STR)															
6	IRX	OUTPUT							X	INPUT						
7	CONTROL & MEMORY REF.				ARITHMETIC W/CARRY				CONTROL				ARITH. IMMEDIATE W/CARRY			
8	GET LOW BYTE OF RN (GLO)															
9	GET HIGH BYTE OF RN (GHI)															
A	SET LOW BYTE OF RN (PLO)															
B	SET HIGH BYTE OF RN (PHI)															
C	LONG BRANCH			NOP	LONG SKIP				LONG BRANCH				LONG SKIP			
D	SET P REGISTER (SEP)															
E	SET X REGISTER (SEX)															
F	LOGIC				ARITHMETIC				LOGIC IMMEDIATE				ARITHMETIC IMMEDIATE			

Memory

- Dual-port RAM (4KB)
  - using Altera Megawizard
  - Single clock
  - single-cycle access
  - new data on same-port read-during-write
- 32 16-bit all-purpose registers
- D, N, I, P, T, X, DF, ALU
- We used more flip-flops...



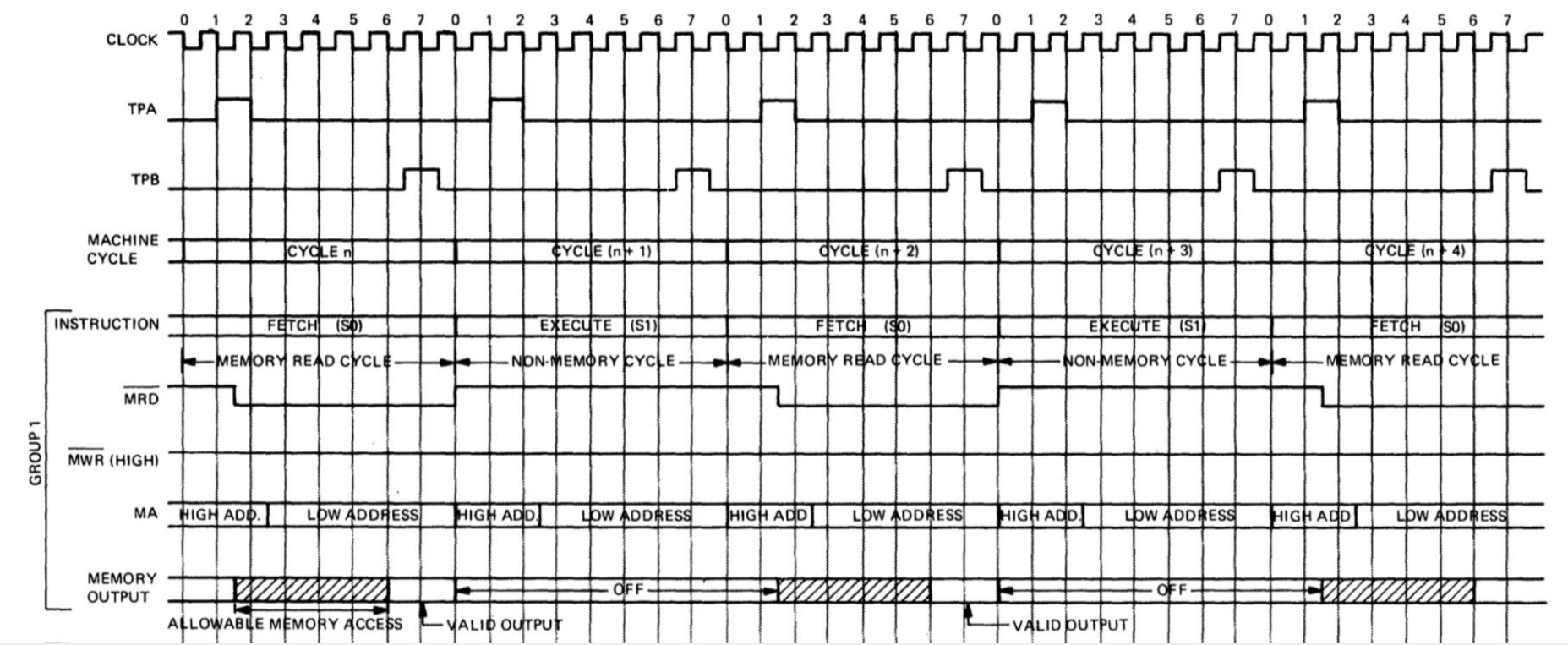
CPU design

- 4 clock cycles per machine cycle
- LOAD, RESET, RUN, PAUSE modes
  - In run mode: FETCH, EXECUTE, EXECUTE2 states

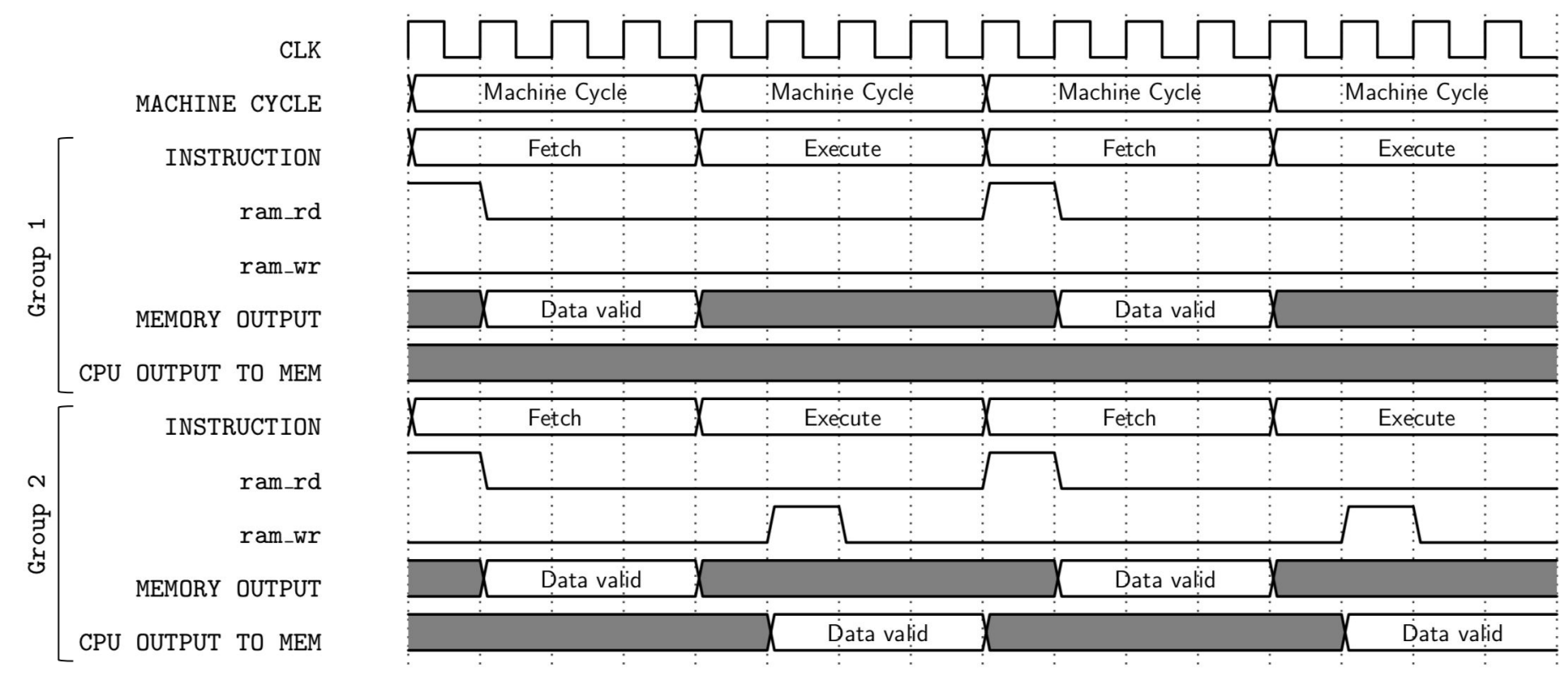
Graphics

- (incomplete)
- VGA displays 64x32 resolution
- Framebuffer implemented with Megawizard dual-port RAM
- Requires 1x2048-bit RAM
    - use only 1 bit for on/off, rather than 8-bit luminance

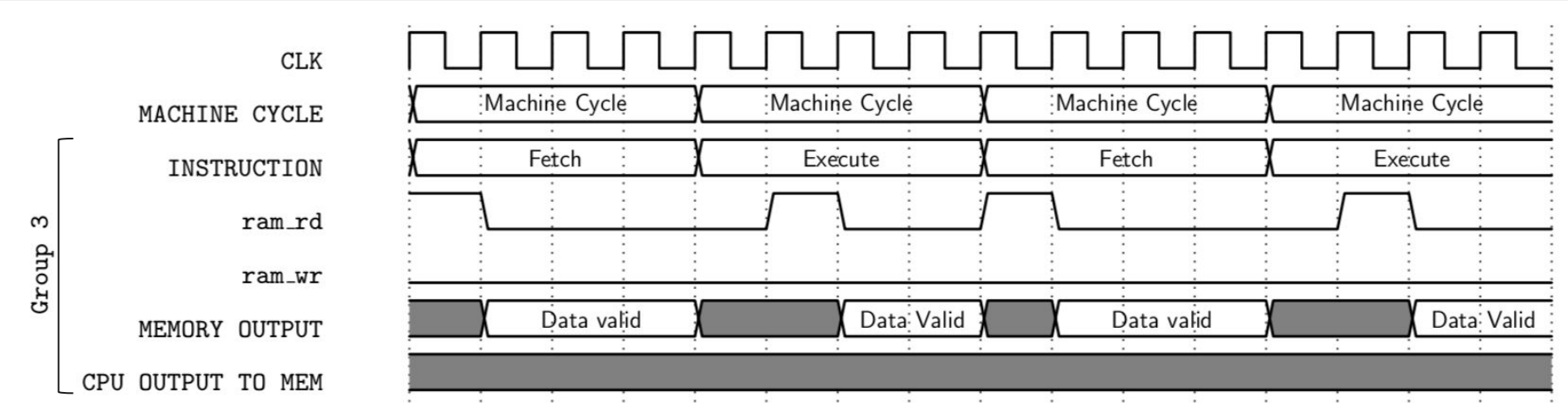
Timing diagrams



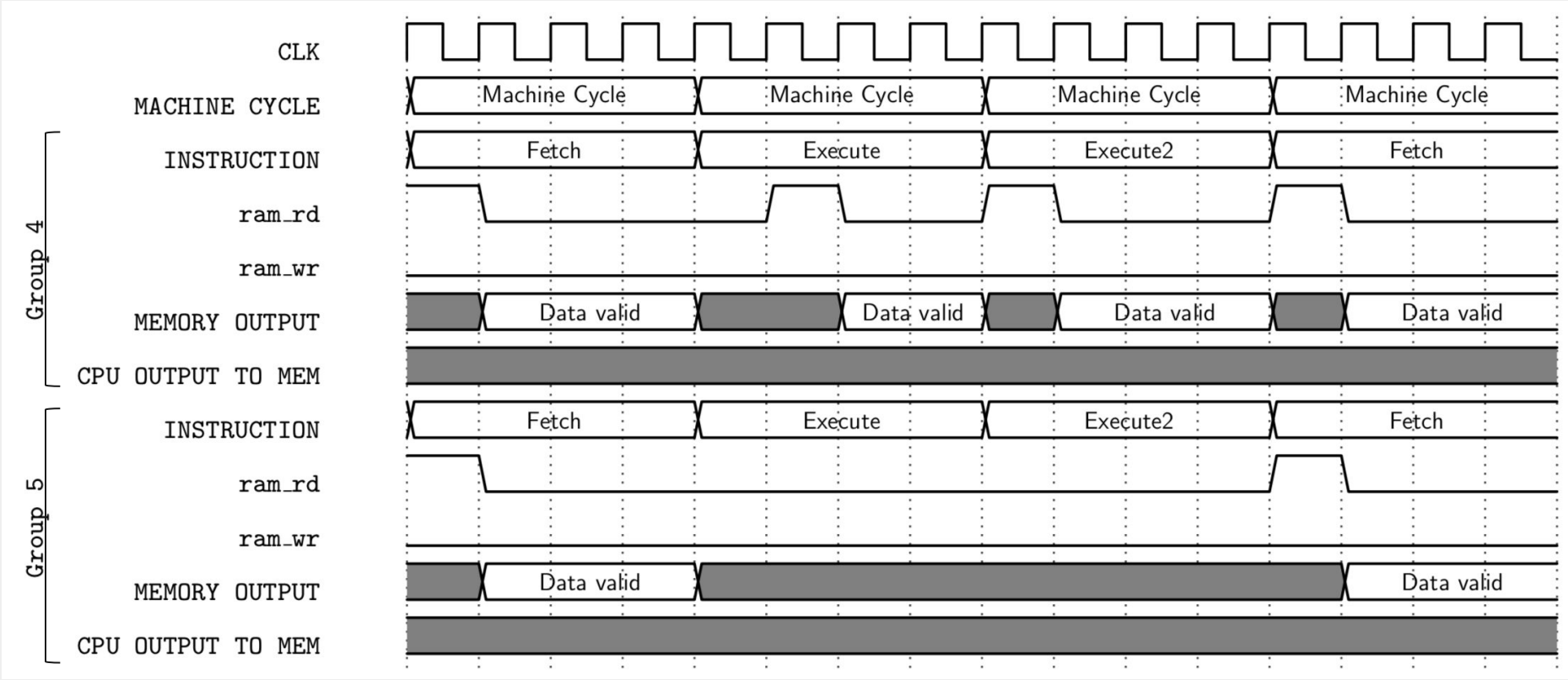
Original CDP1802 timing, Group 1 instructions



Instruction set timing: Group 1 Read/Non-memory, Group 2 Read/Read



Instruction set timing: Group 3 Read/Write

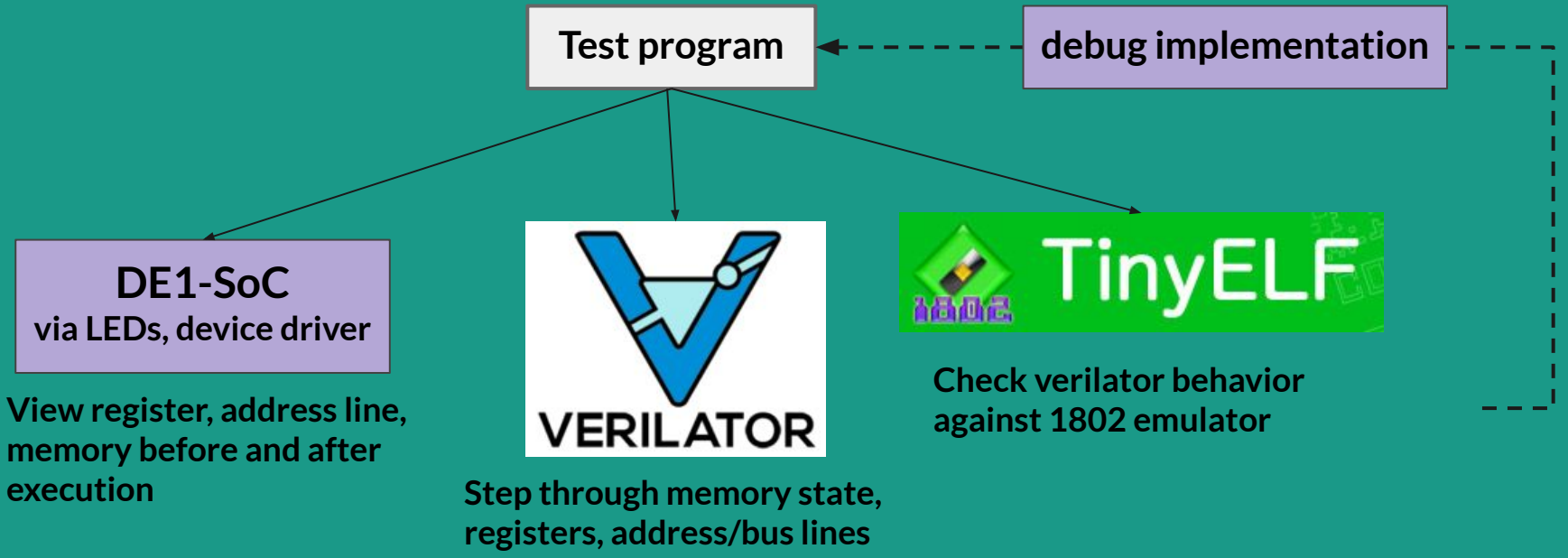


Instruction set timing: Group 4 Read/Read/Read, Group 2 Read/Non-memory/Non-memory

Hardware-software interface

- Avalon Memory-Mapped Port reads from/writes to RAM
- Linux Device driver
  - dtb specification generated from sopc file
  - ioctls for 8-bit read/write and burst 32-bit read/write
- User-space programs using device driver

Debugging & Testing



Demo

test_9N_BN

E4 :: x = 4

24 :: R(4) = FF

84 :: D = R(4).0 = FF

B3 :: R(3) = FF00

~~23 :: R(3) =~~ FEFF

93 :: D = R(3).1 = FE

test_5N

E0 : D = 0

1a : R(a) = 1

1a : R(a) = 2

8a : D = R(a) = 2

~~5a : M(2) =~~ 2