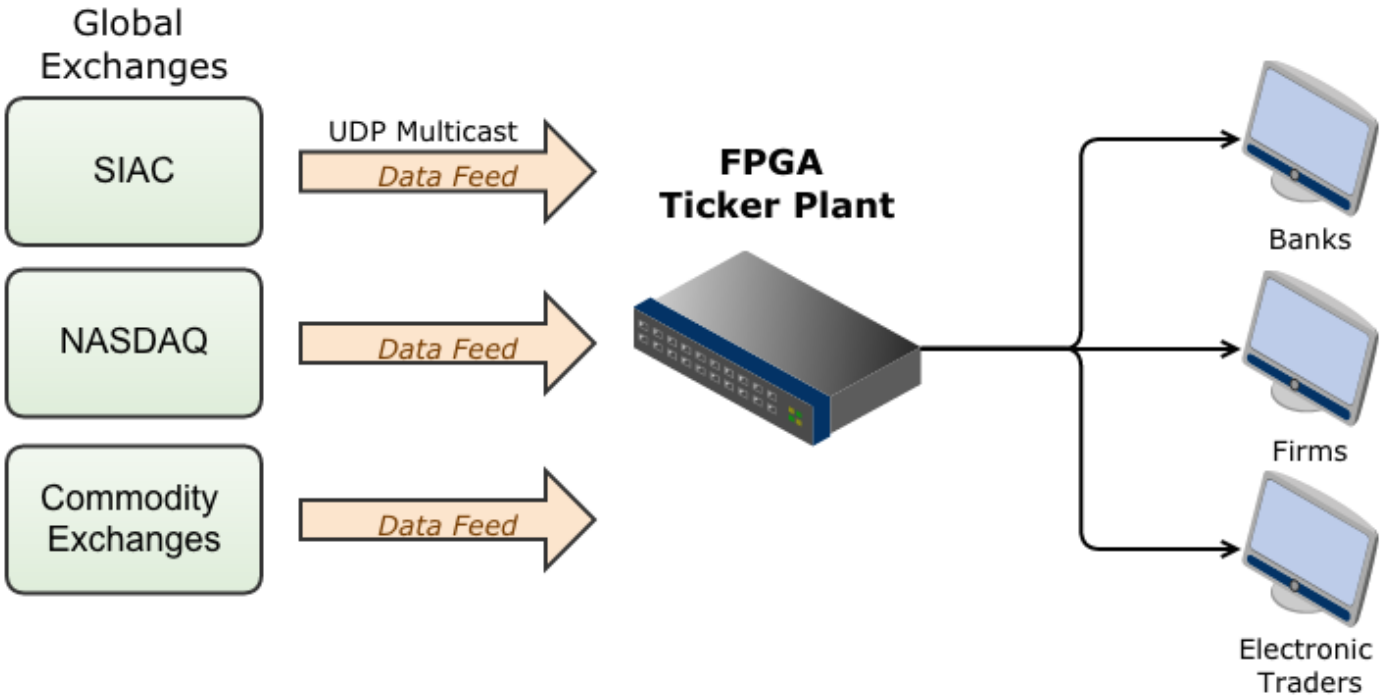
# Ticker Plant System Implemented in MaxCompiler

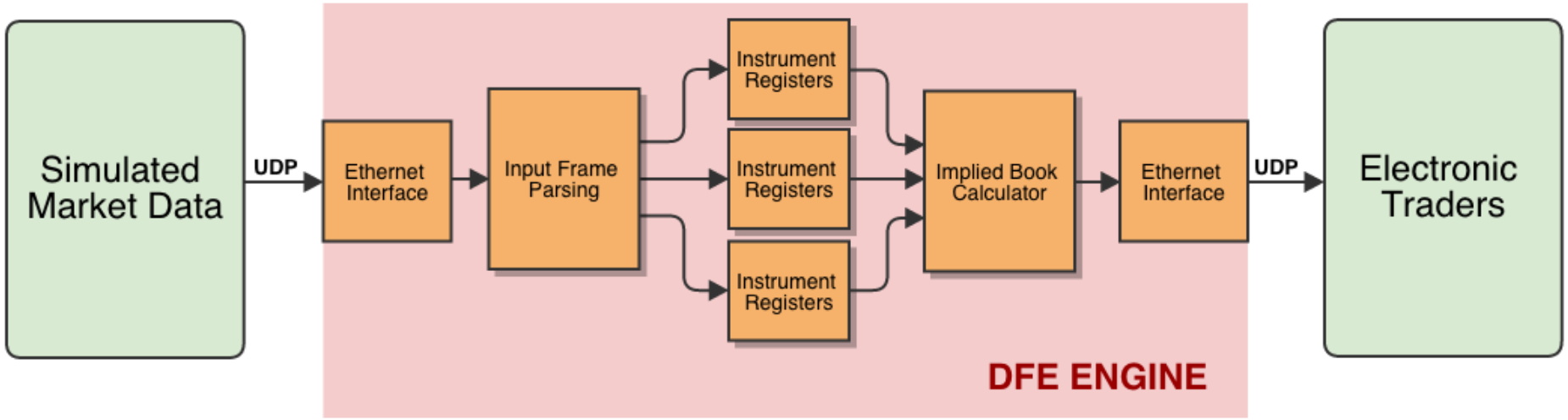
Gabriel Blanco (gab2135@columbia.edu)
Brian Bourn (bab2177@columbia.edu)
David Naveen Dhas Arthur (da2647@columbia.edu)
Suchith Vasudevan (sv2340@columbia.edu)

# Ticker Plant



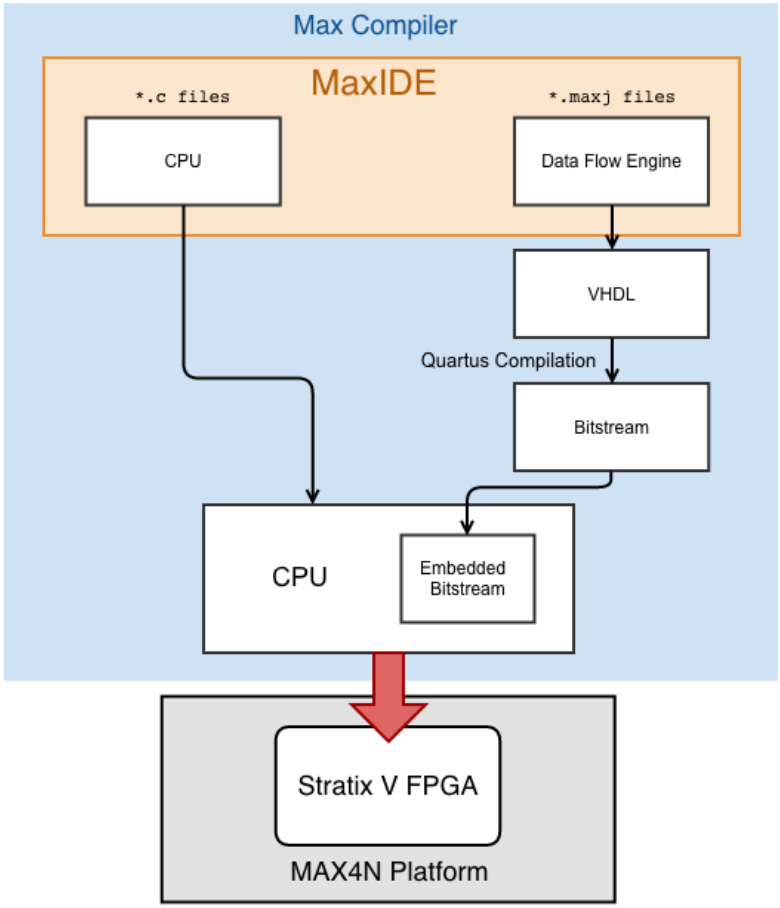

Receives data from the Exchange, calculates all possible implied values, then outputs them in a Machine Readable and sanitized format.

# Implementation



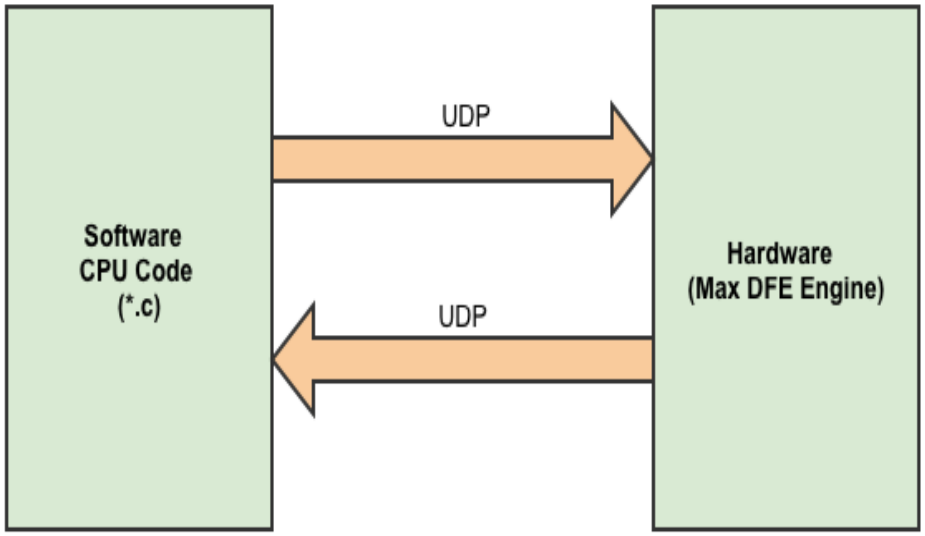

- Simulated market data is parsed CSV received through Ethernet (UDP)
- Kernel computes implied market data from real market data and stores them in respective registers
- Register data is transferred to order book through Ethernet (UDP)

# Max Compiler




- Development Environment for writing *optimized* hardware code
- Compiles the .maxj (DFE engine and manager) to VHDL
- The MaxCompiler uses an extension of Java and a proprietary version of the Eclipse IDE
- Compile -> Quartus Compile Run -> Hardware Implementation

# Software and Hardware Interface




- Communication between the CPU and the FPGA done with a networking approach rather than shared memory.
- UDP Streams sent through Ethernet

# Hardware: Platform

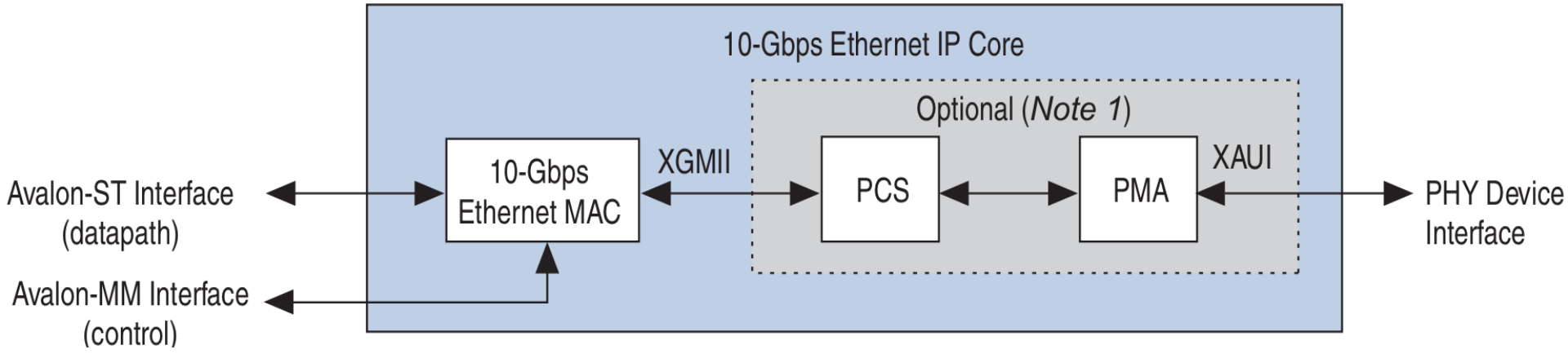
- Max4N FPGA platform
- PCIE express bus
- 24GB DDR3 offchip memory

# Hardware: FPGA

| FPGA | Altera Cyclone V 5CSXFC6D6F31C8ES | Altera Stratix V 5SGXMABN2F45C2 |
|---|---|---|
| Platform | SoCKit Board | Max4N Platform |
| ALMS | 41,910 | 359,200 |
| Block Memory Bits | 5,662,720 | 54,067,200 |
| DSP Blocks | 112 | 352 |

- Stratix V FPGA
- Higher count of ALMs
- On-Chip memory (M20k memory blocks)

# Hardware: Networking




- 2 QSFP Ports
- 4x10 Gbps Ethernet
- Avalon-ST 64-bit wide client interface
- Operating Frequency: 156.25 MHz with 10-Gbps full-duplex throughput rate (Fmax = 203.6 Mhz)

# Conclusion

- MaxCompiler used a simulation engine that executed in a significantly shorter amount of time than a normal Quartus compile.

- Documentation on the Maxeler IDE was sparse and heavily controlled by Maxeler, making it very hard to learn the language.


THANK$
$TE(pH)EN
and
DAVID!
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