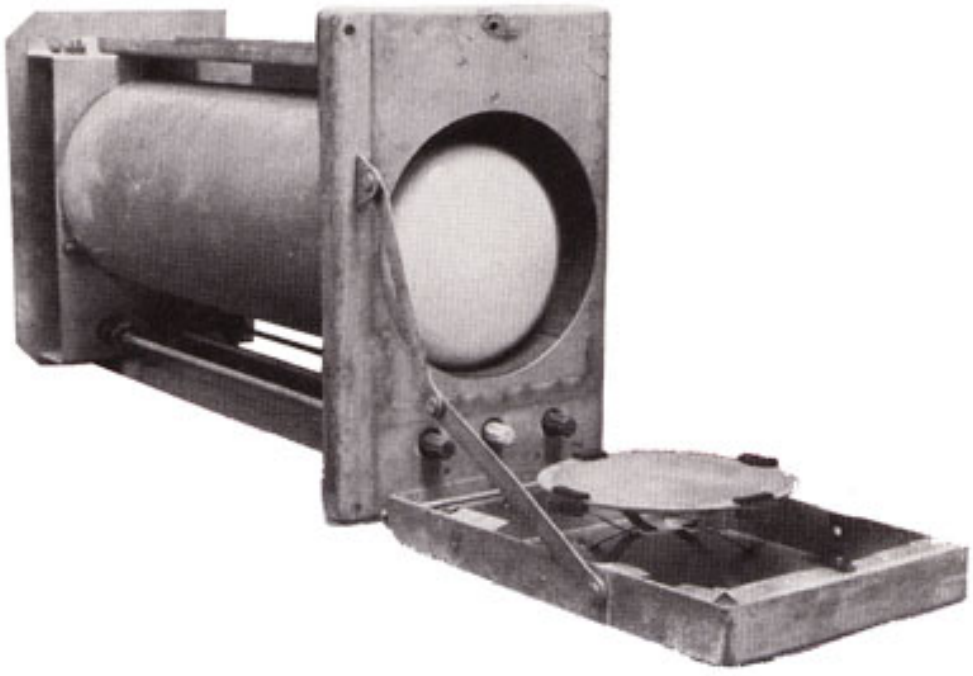
Memory

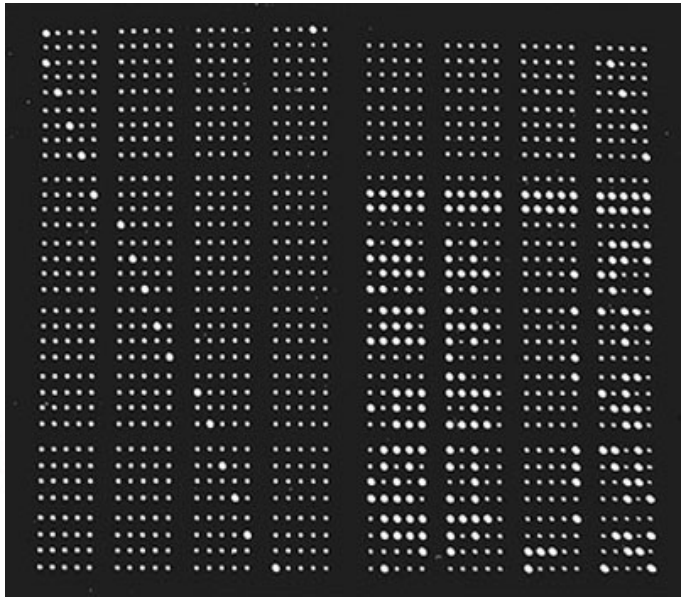
Stephen A. Edwards

Columbia University

Spring 2012

Early Memories





Williams Tube CRT-based random access memory, 1946. Used on the Manchester Mark I. 2048 bits.

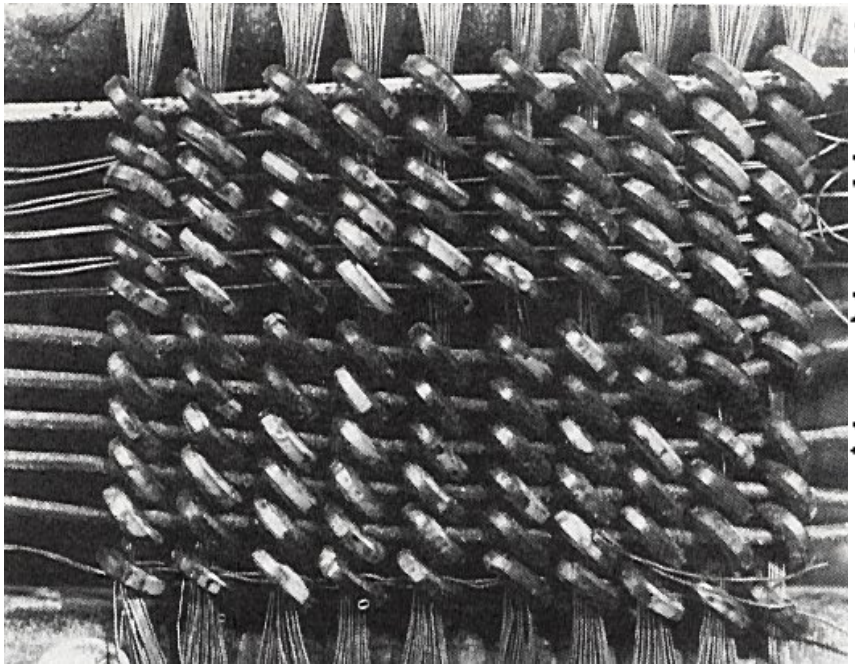
Early Memories

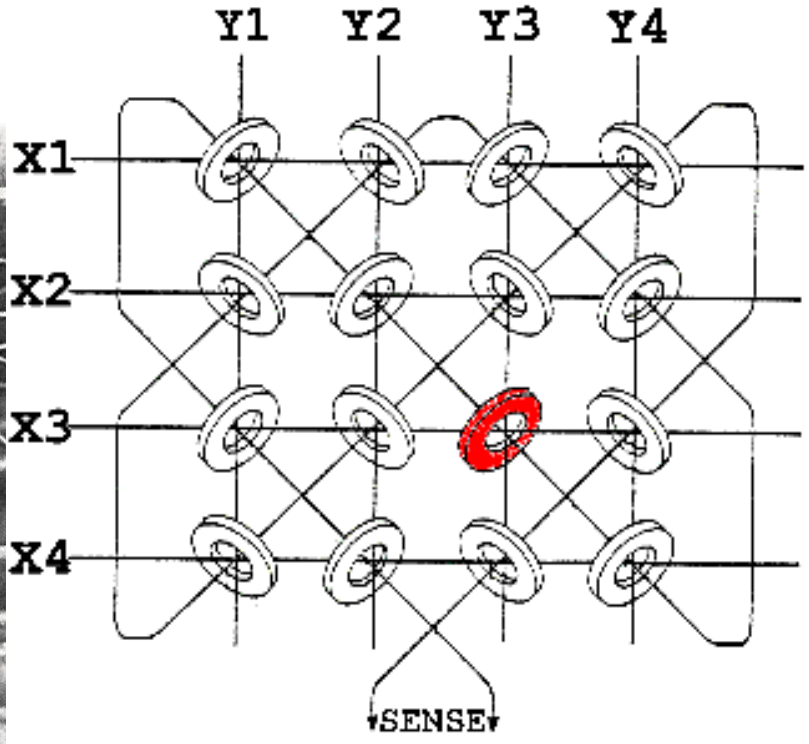
Mercury acoustic delay line.

Used in the EDASC, 1947.

32 × 17 bits

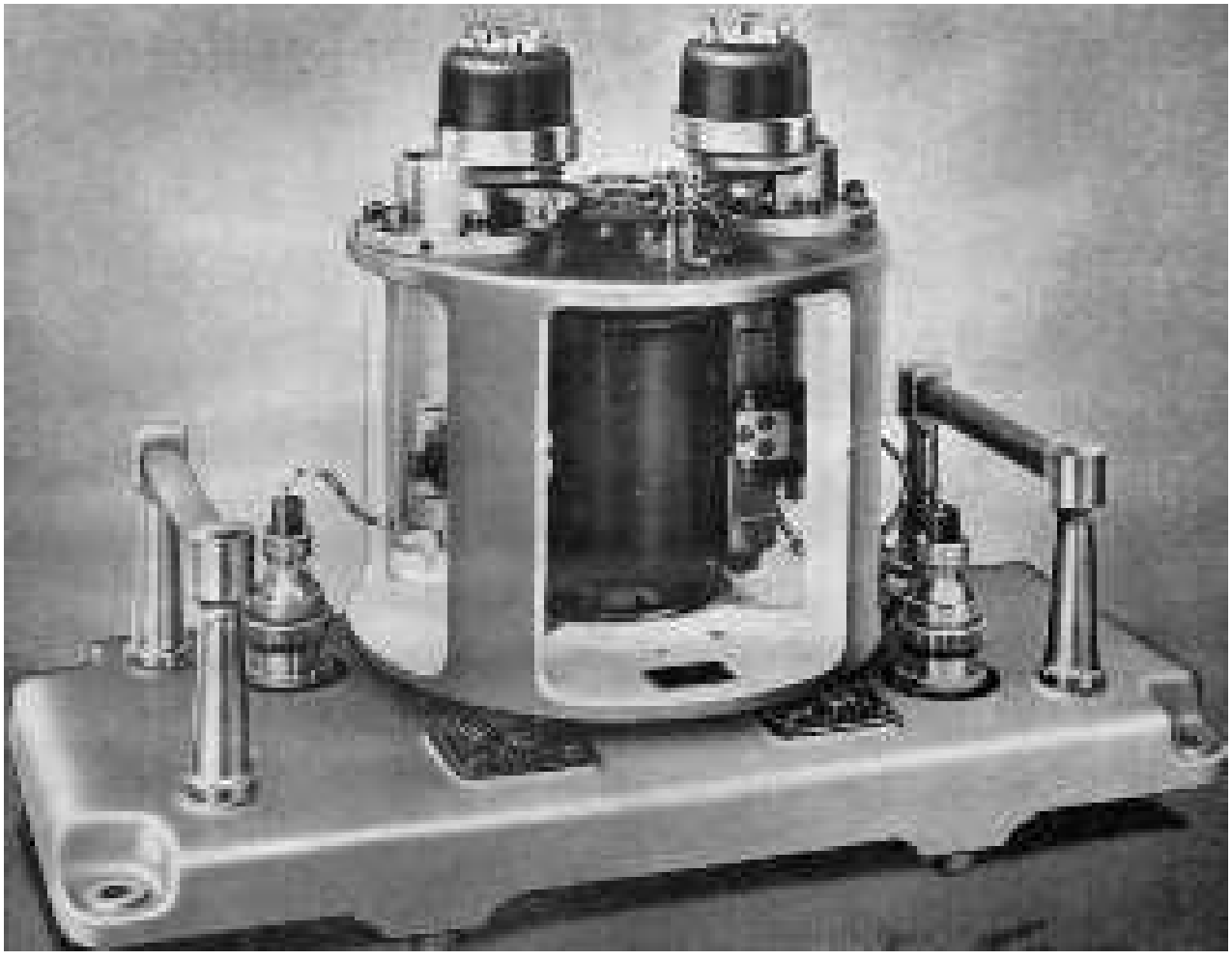
Early Memories





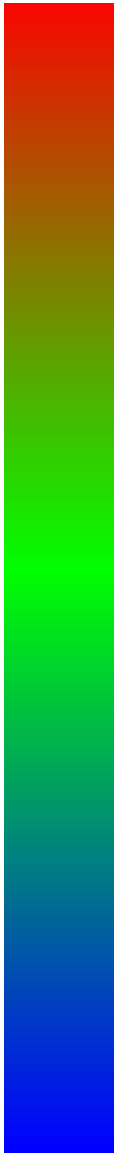
Magnetic core memory, 1952. IBM.

Early Memories



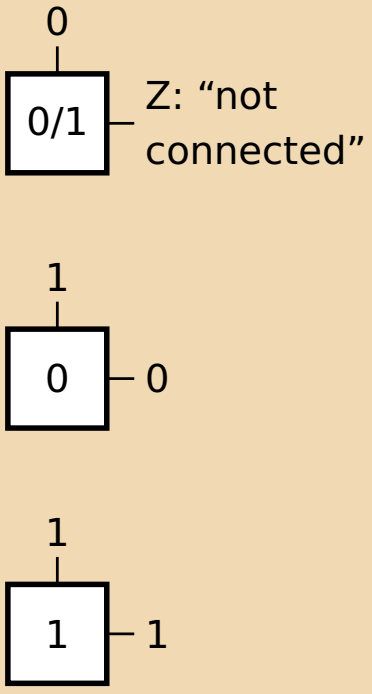
Magnetic drum memory. 1950s & 60s. Secondary storage.

Modern Memory Choices

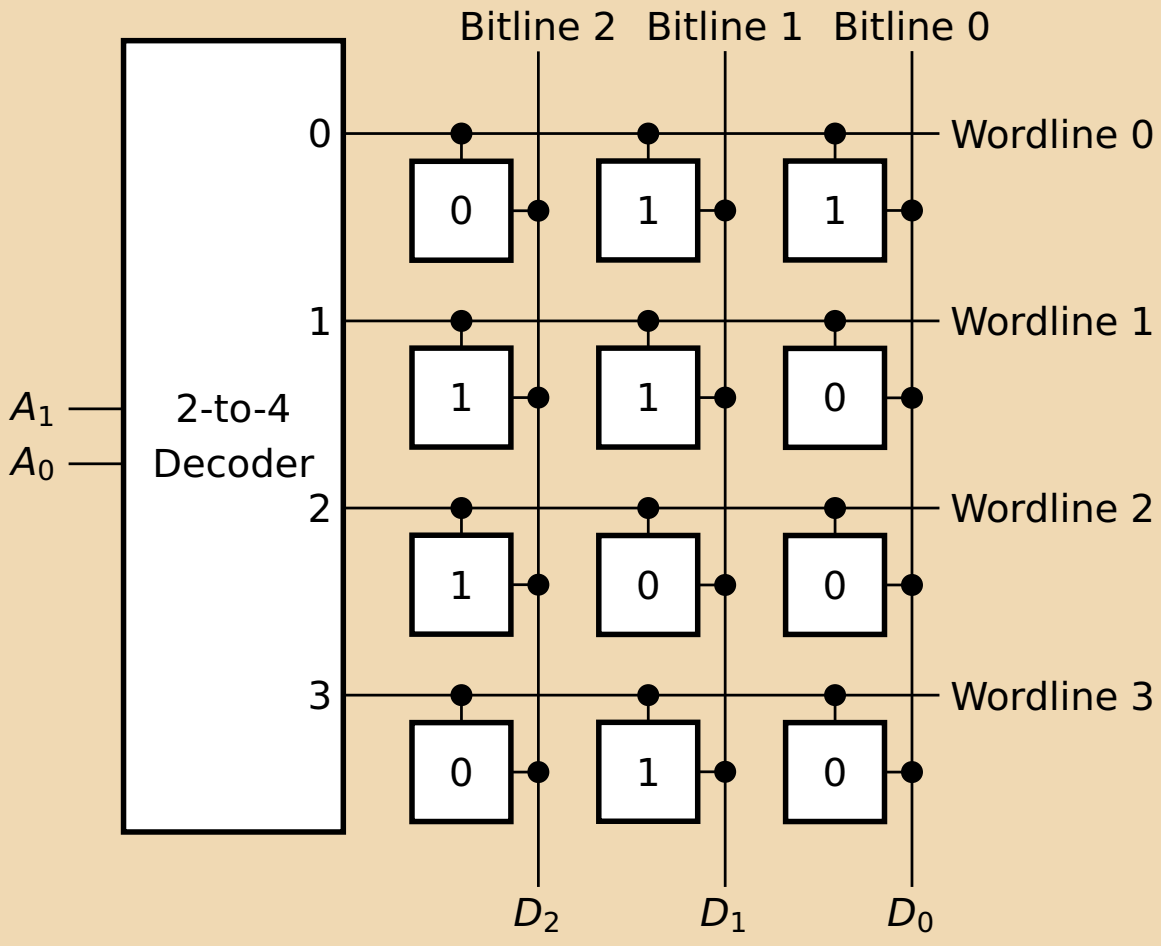


Family	Programmed	Persistence
Mask ROM	at fabrication	∞
PROM	once	∞
EPROM	1000s, UV	10 years
FLASH	1000s, block	10 years
EEPROM	1000s, byte	10 years
NVRAM	∞	5 years
SRAM	∞	while powered
DRAM	∞	64 ms

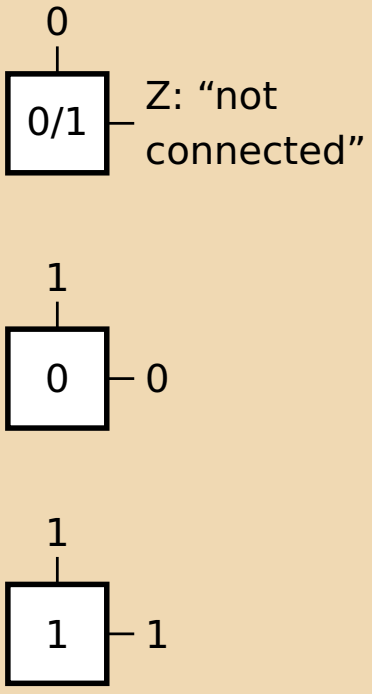
Implementing ROMs



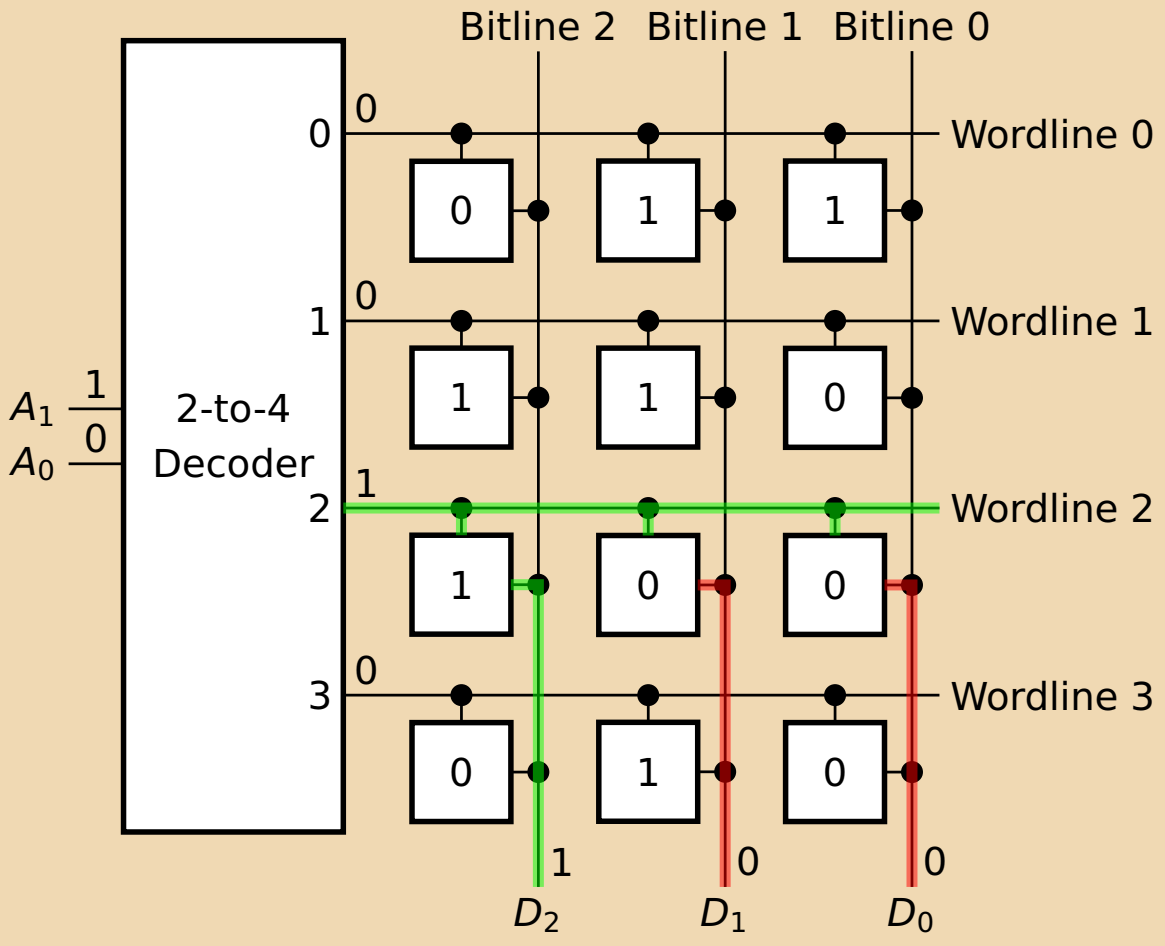
Add.	Data
00	011
01	110
10	100
11	010



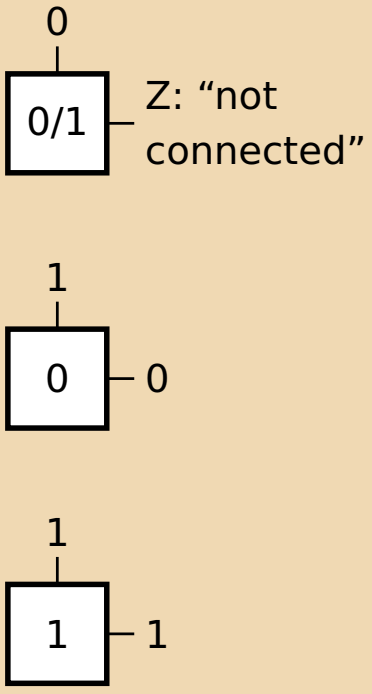
Implementing ROMs



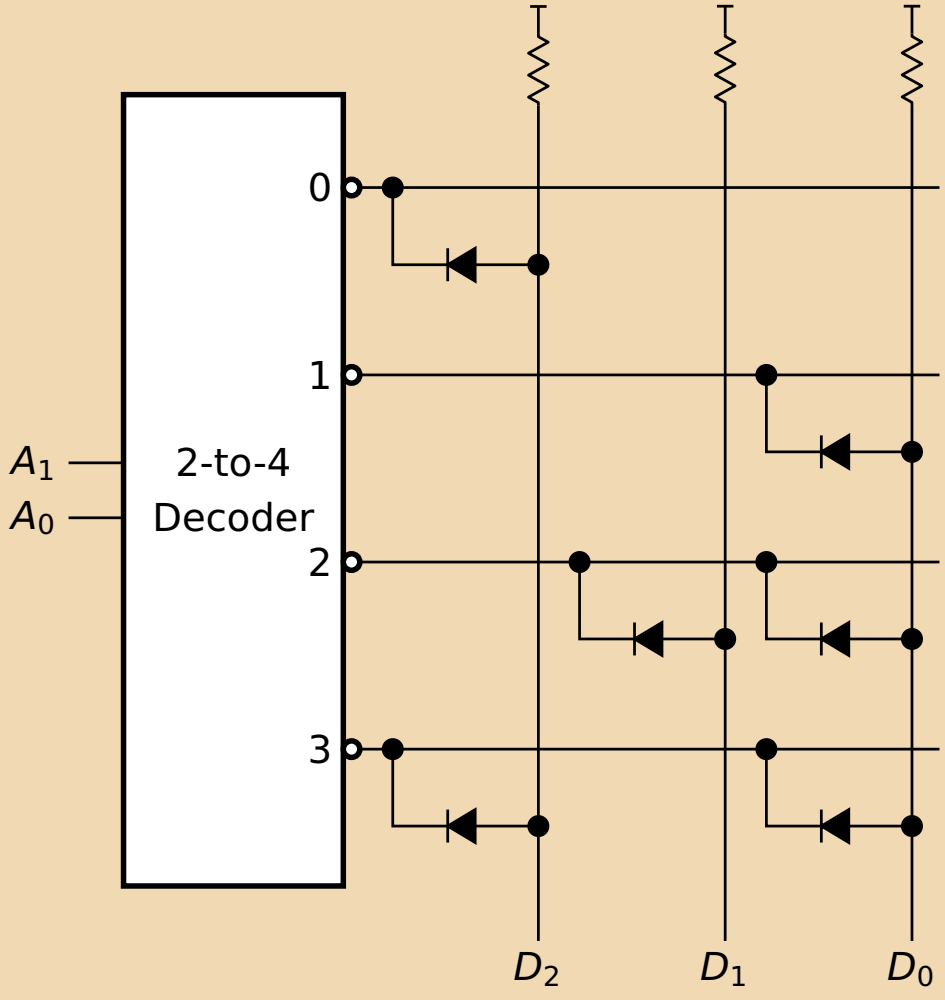
Add.	Data
00	011
01	110
10	100
11	010



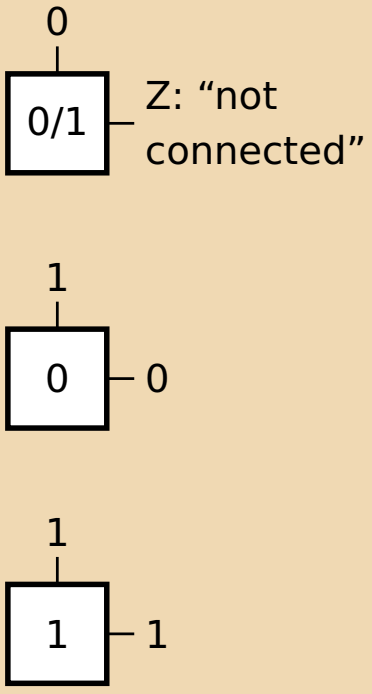
Implementing ROMs



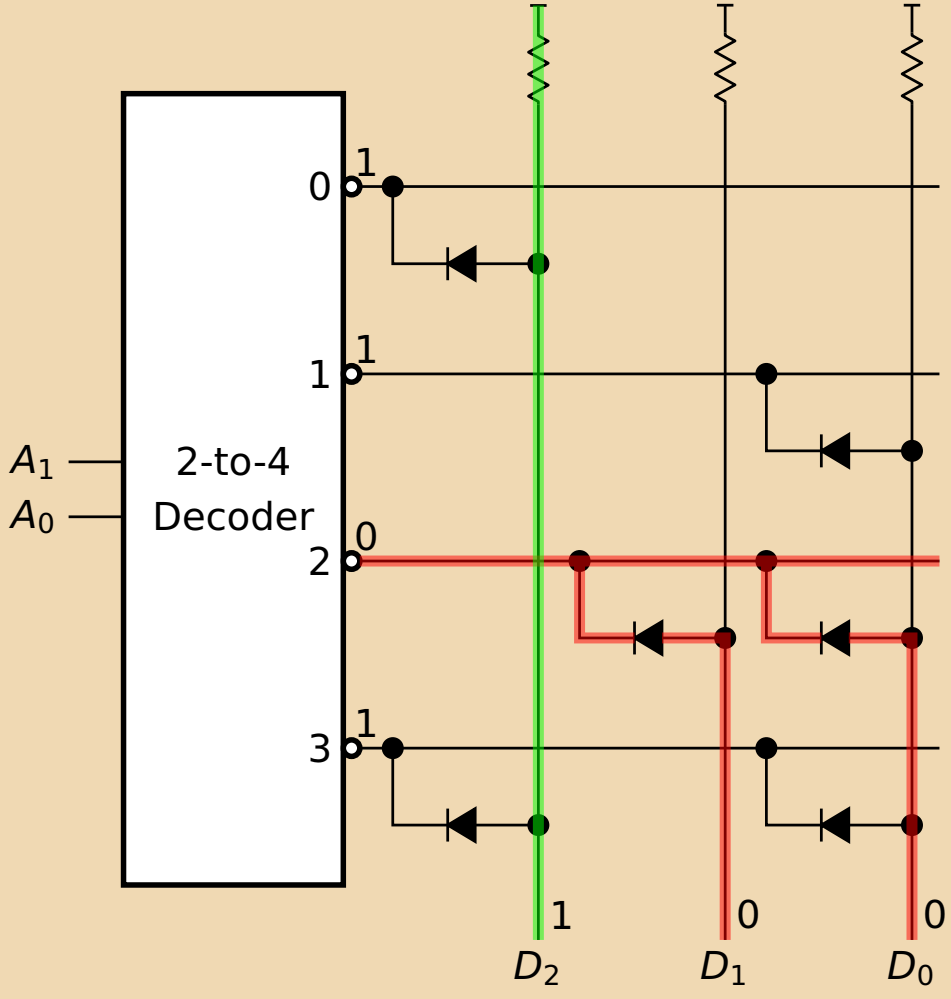
Add.	Data
00	011
01	110
10	100
11	010



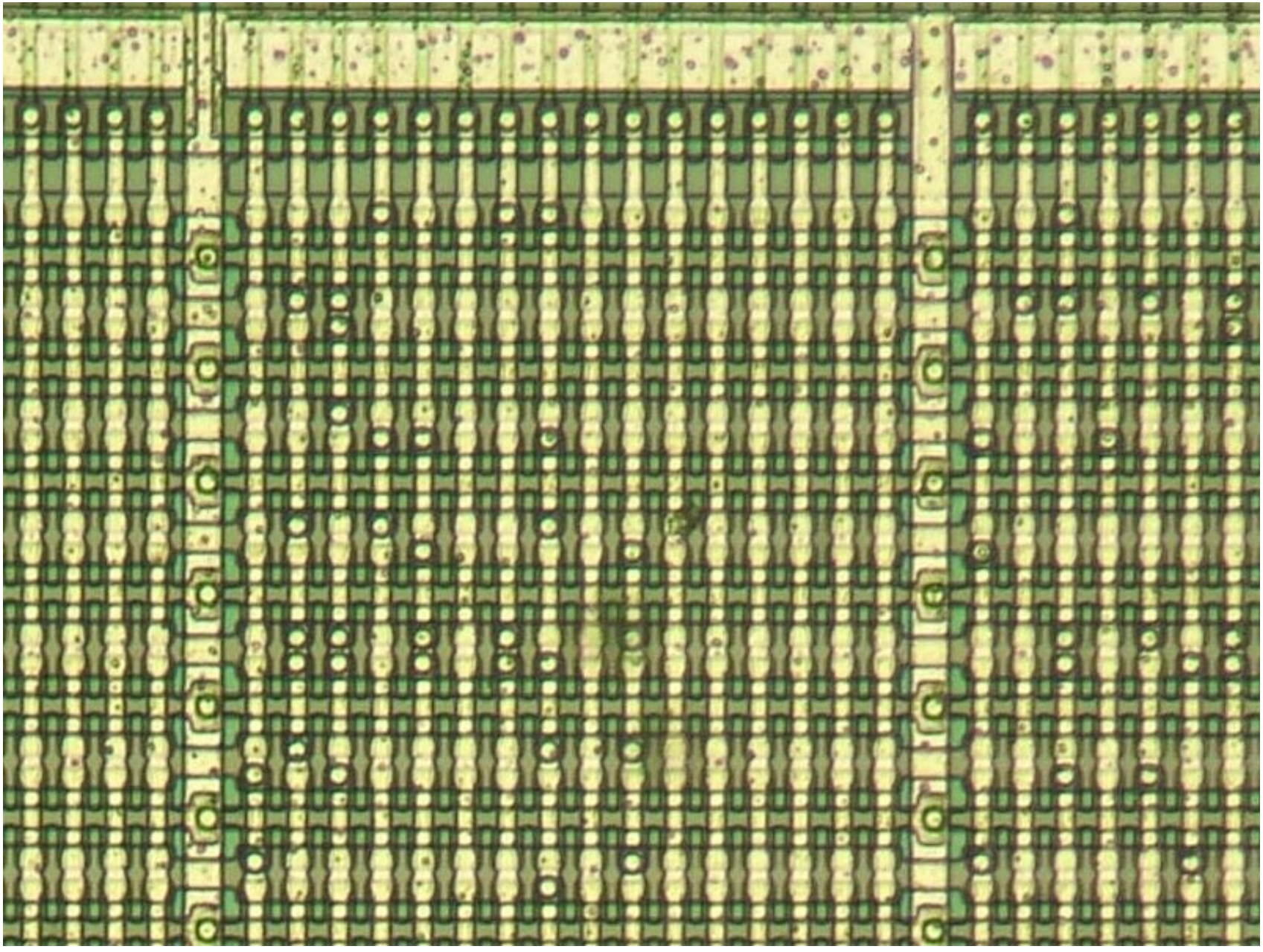
Implementing ROMs



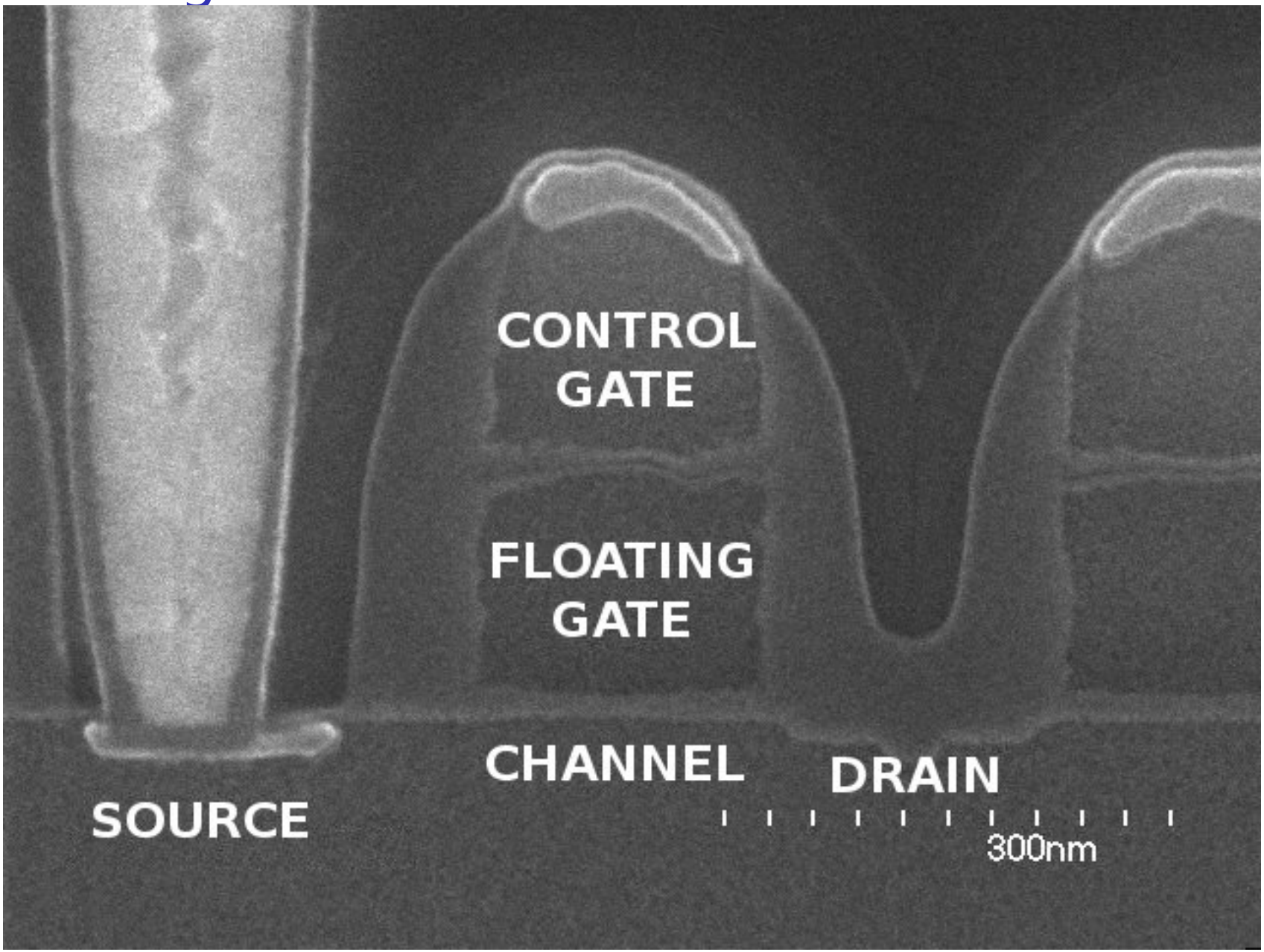
Add.	Data
00	011
01	110
10	100
11	010



Mask ROM Die Photo

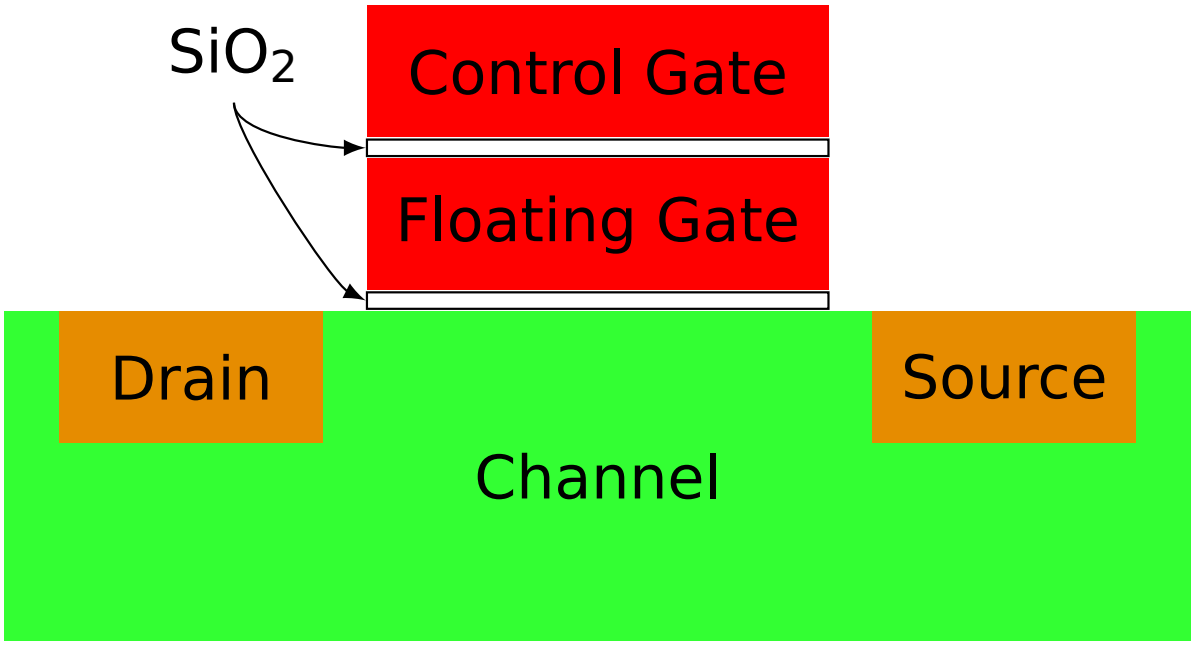


A Floating Gate MOSFET



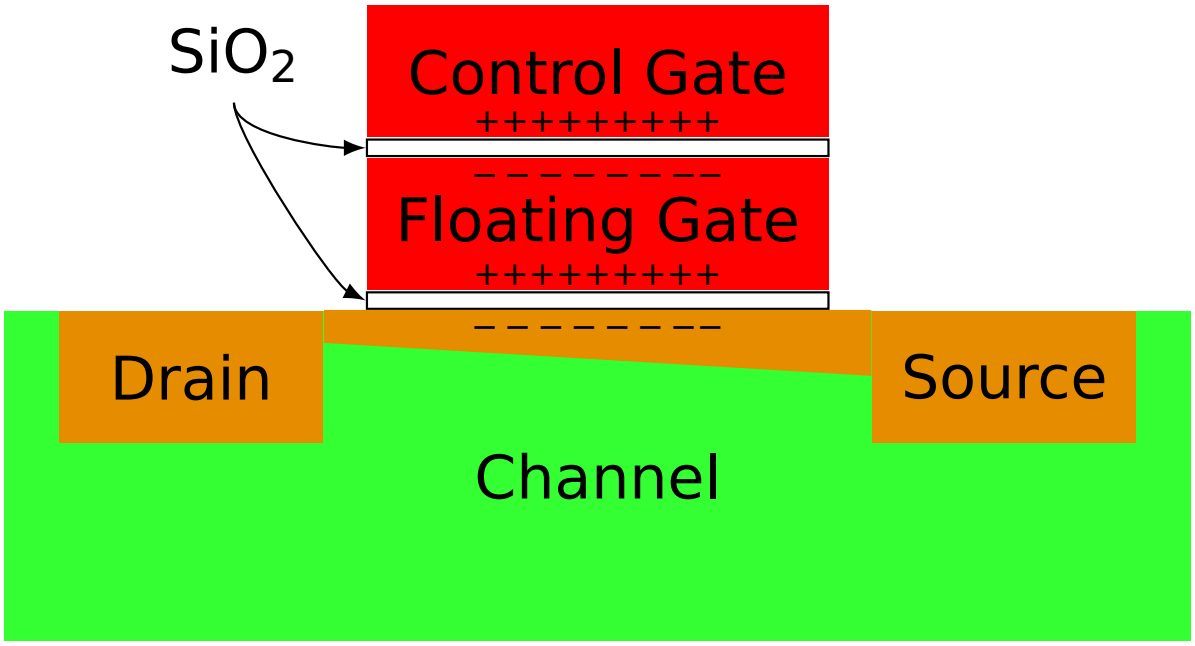
Cross section of a NOR FLASH transistor. Kawai et al., ISSCC 2008 (Renesas)

Floating Gate n-channel MOSFET



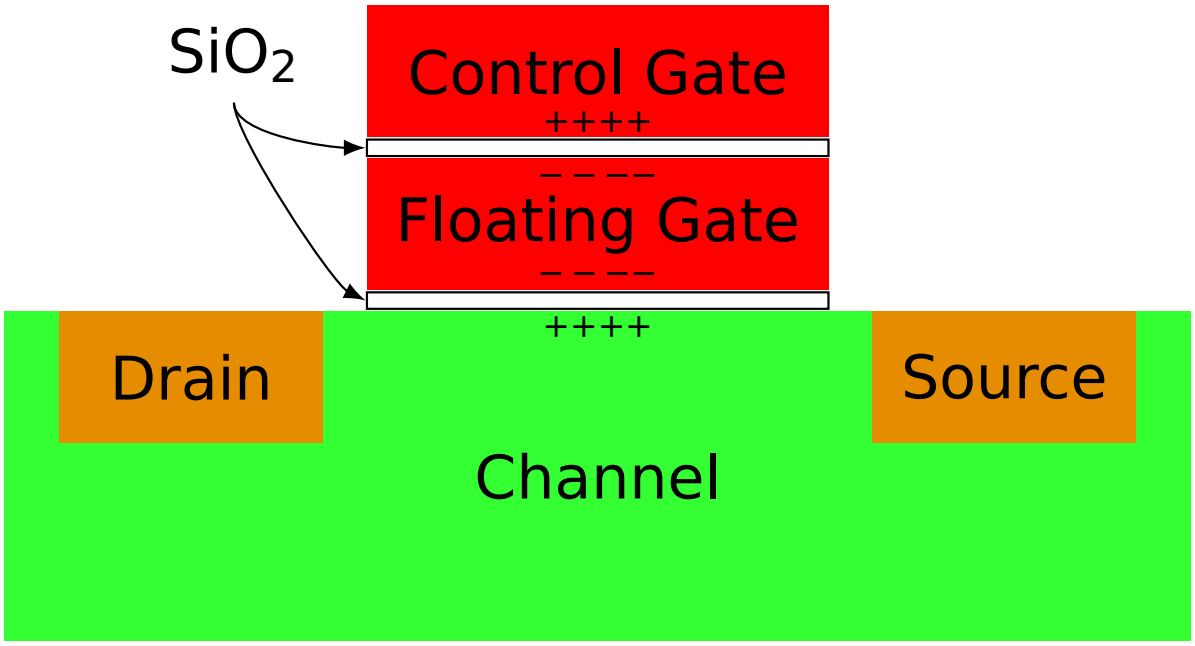
Floating gate uncharged; Control gate at 0V: Off

Floating Gate n-channel MOSFET



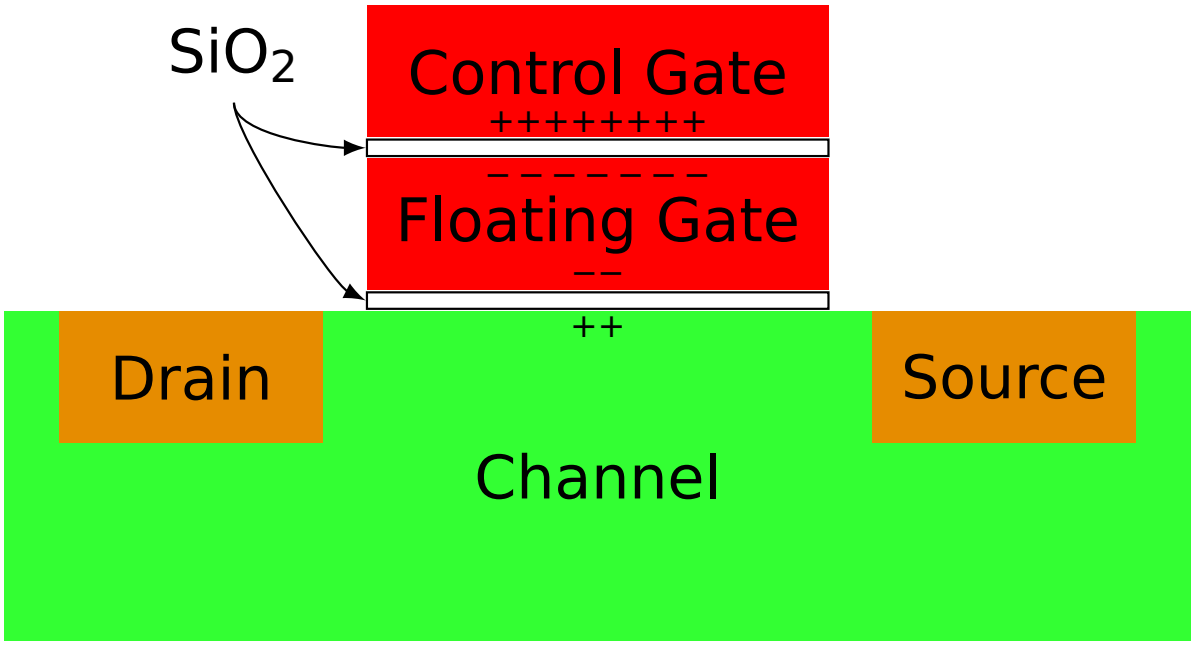
Floating gate uncharged; Control gate positive: On

Floating Gate n-channel MOSFET



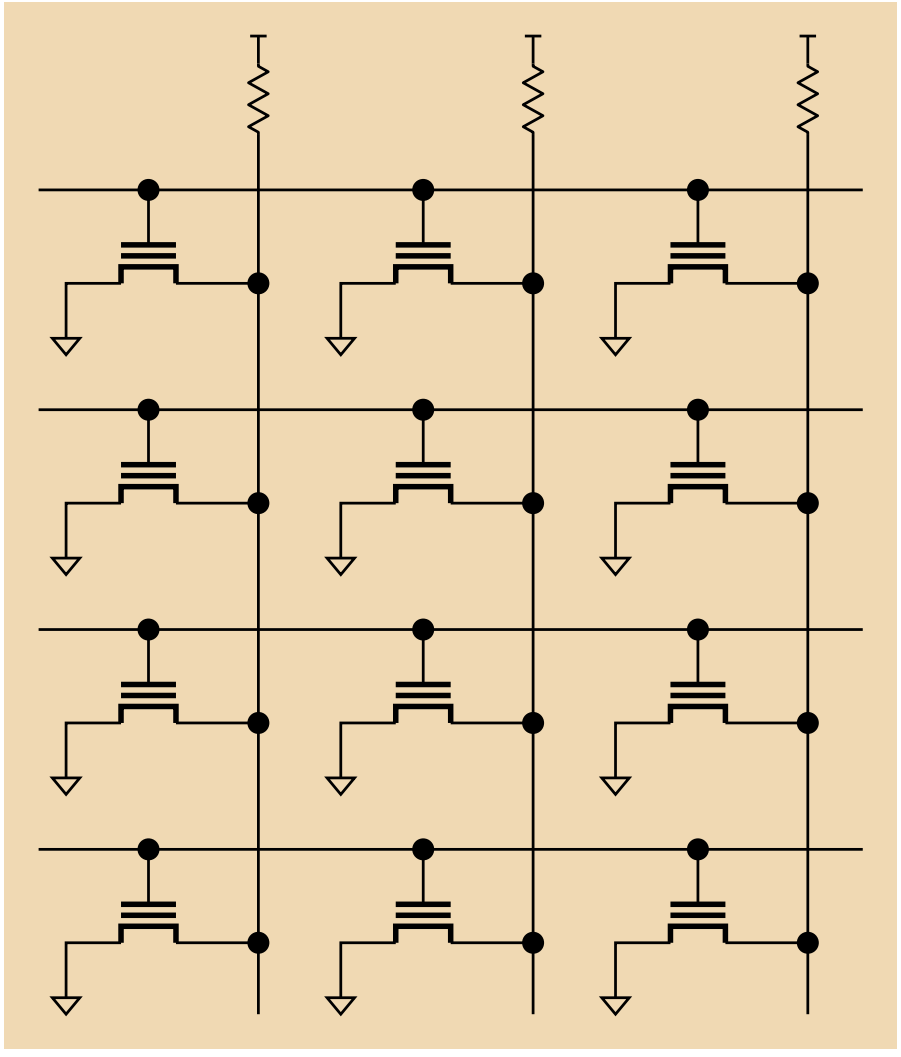
Floating gate negative; Control gate at 0V: Off

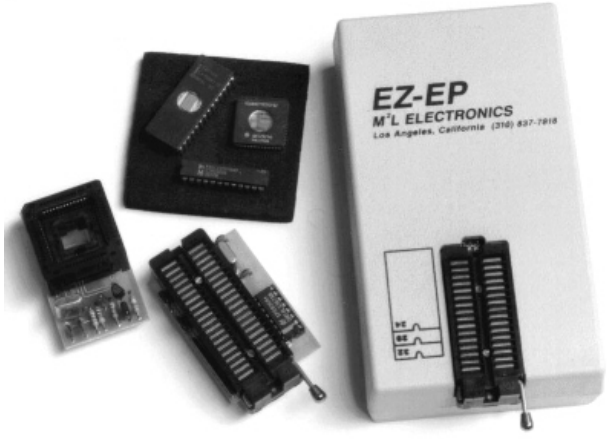
Floating Gate n-channel MOSFET



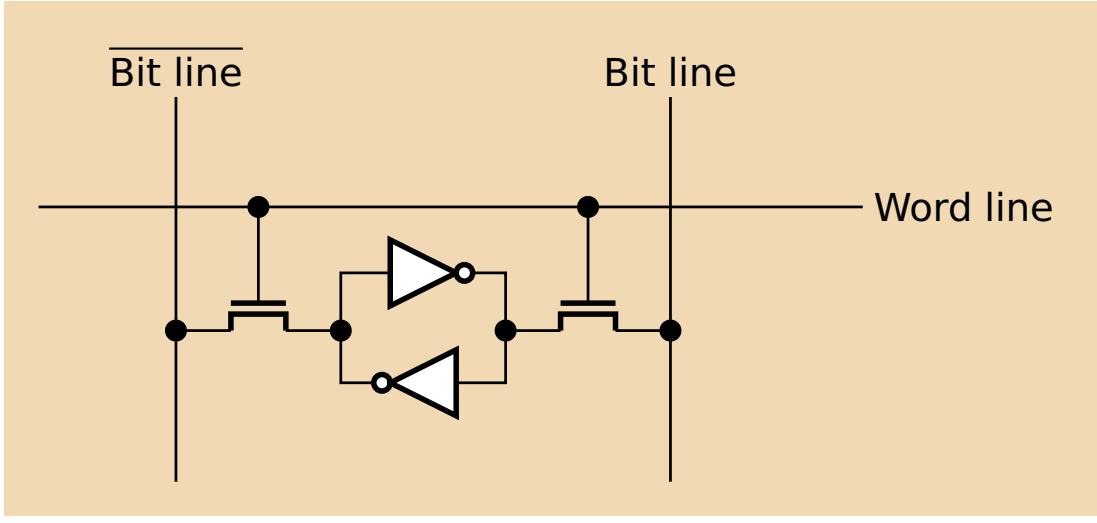
Floating gate negative; Control gate positive: Off

EPROMs and FLASH use Floating-Gate MOSFETs

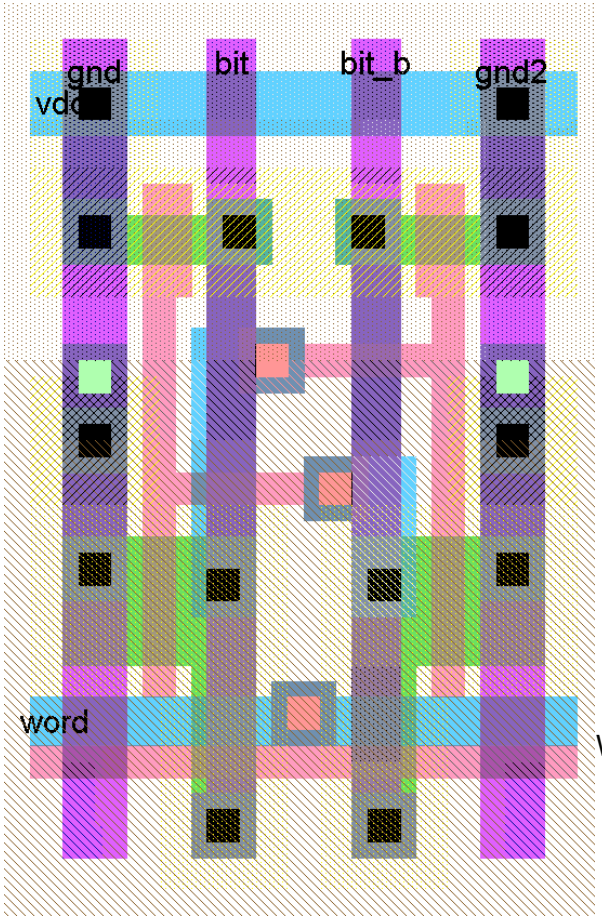


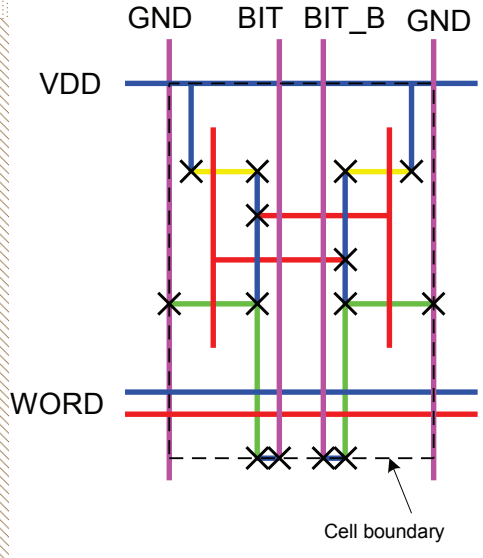


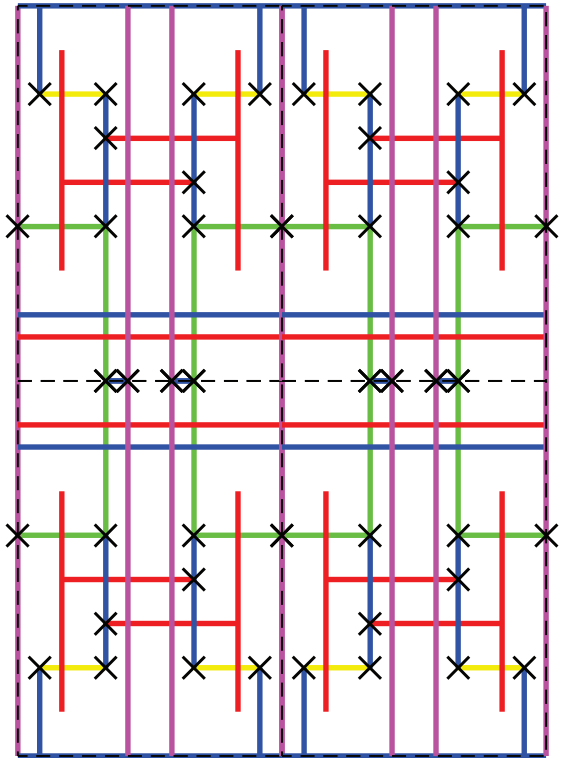
Static Random-Access Memory Cell



Layout of a 6T SRAM Cell

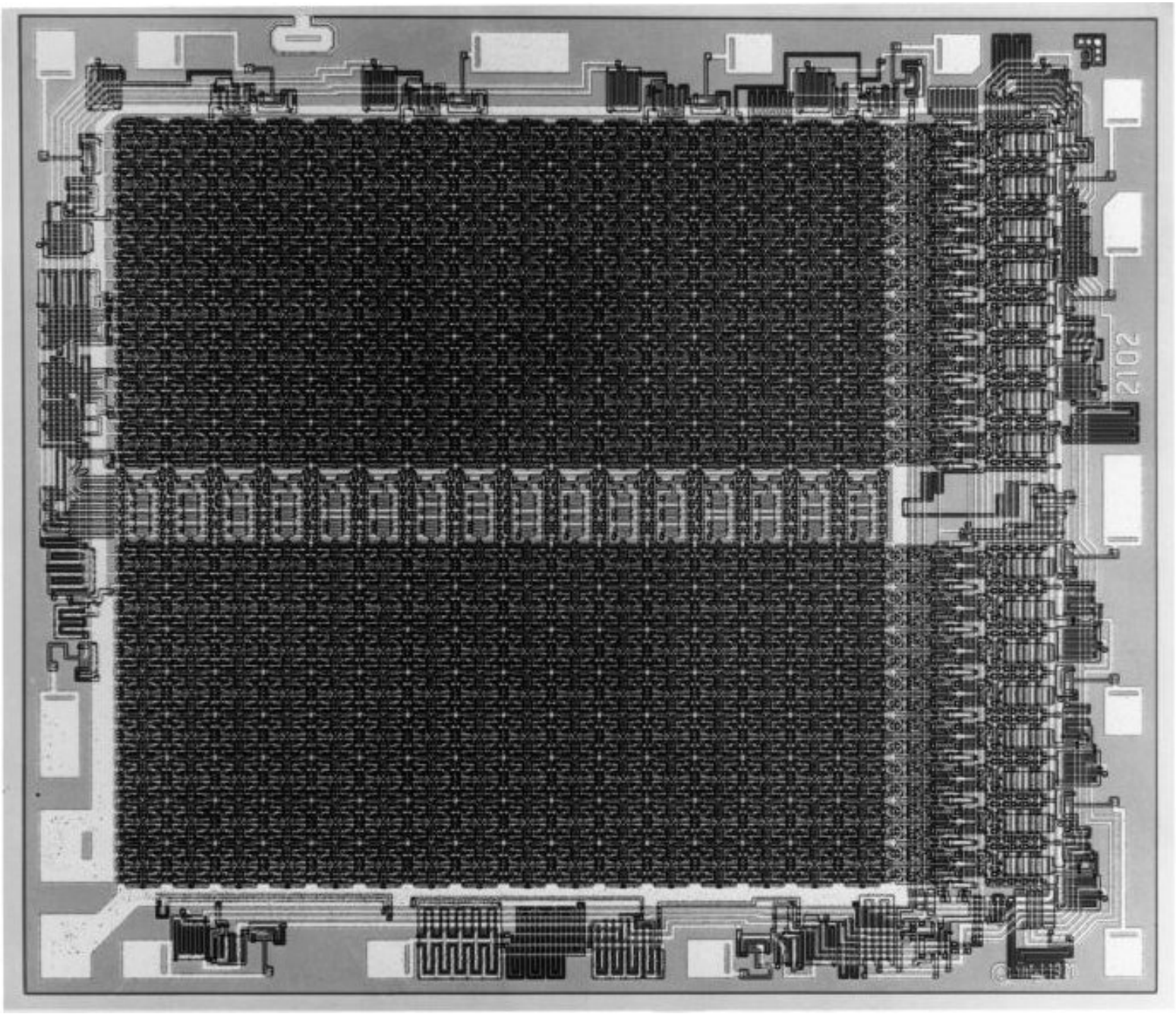




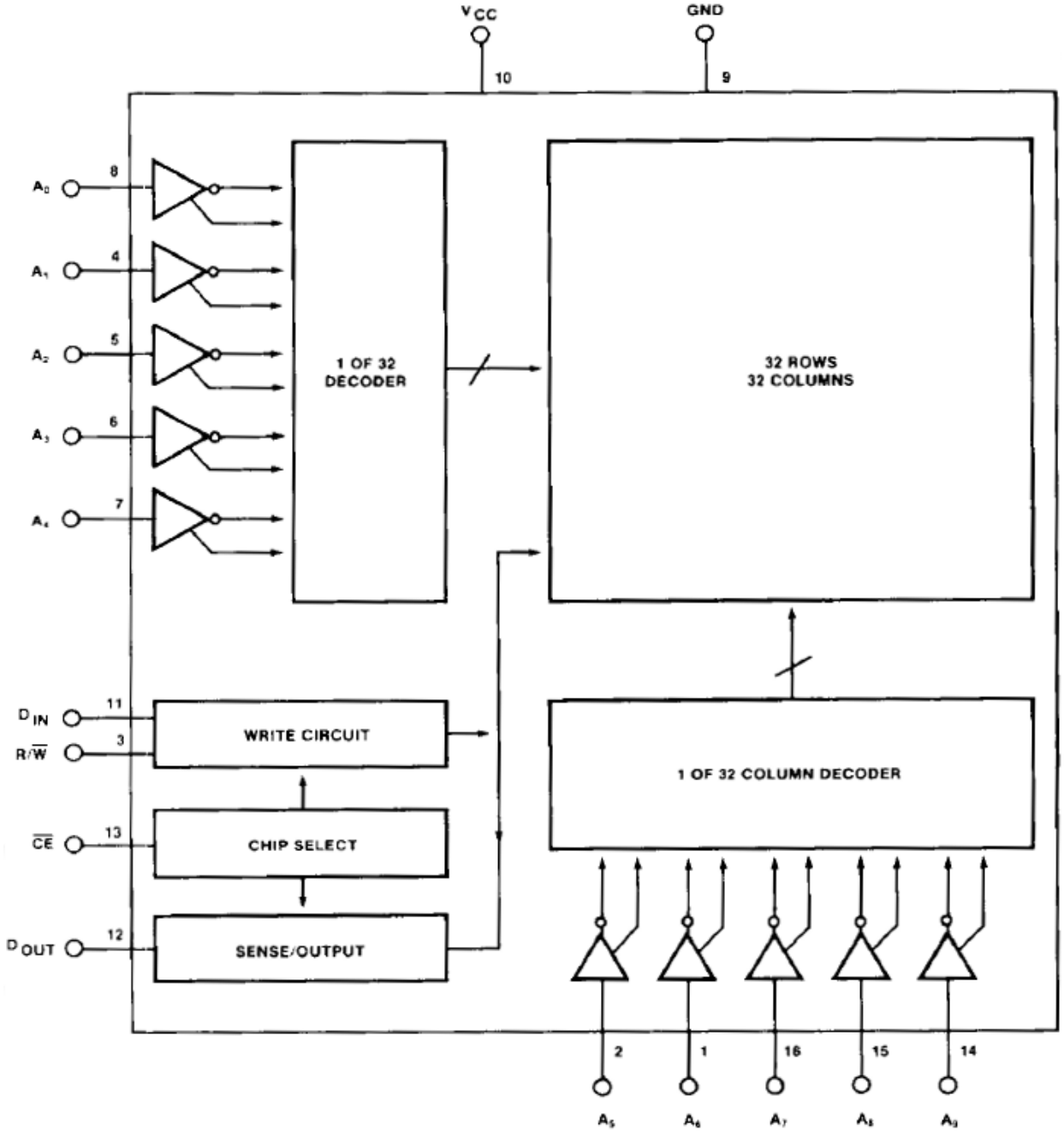


Weste and Harris. *Introduction to CMOS VLSI Design*. Addison-Wesley, 2010.

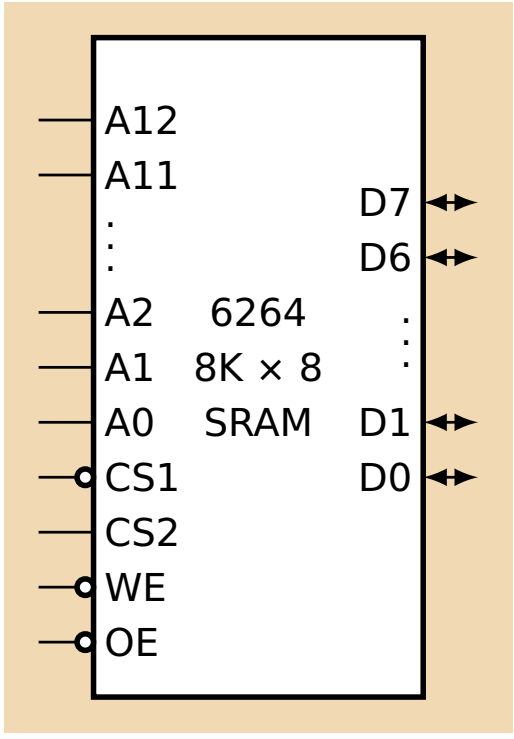
Intel’s 2102 SRAM, 1024 × 1 bit, 1972

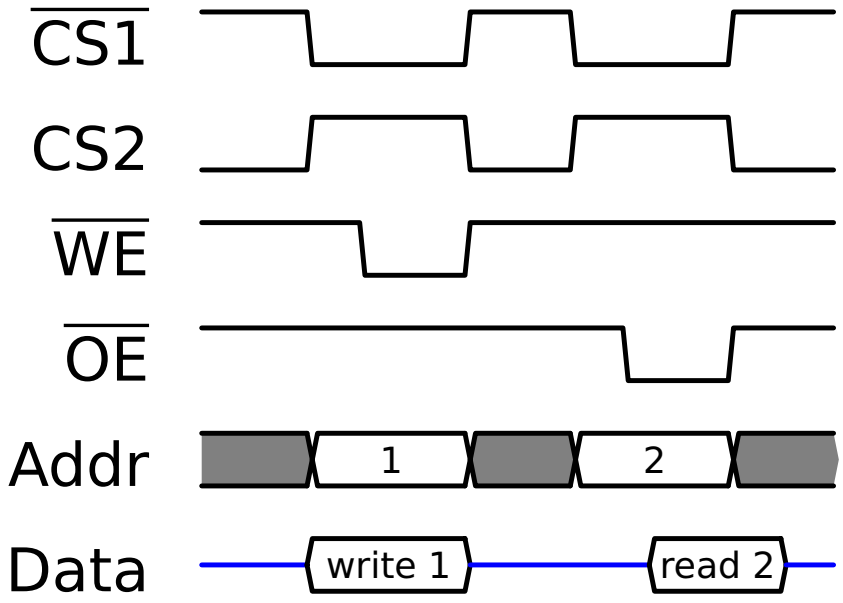


2102 Block Diagram

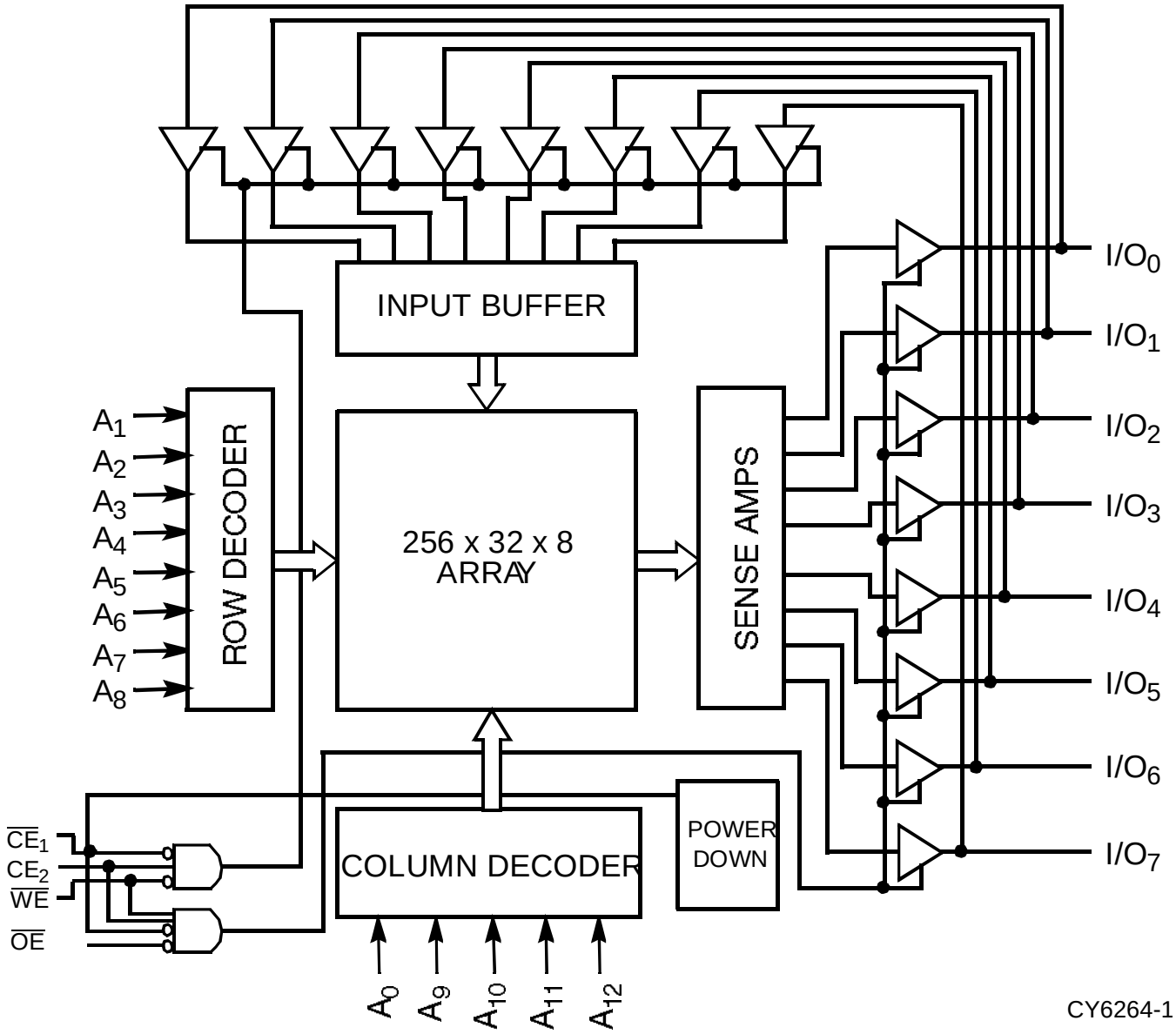


SRAM Timing

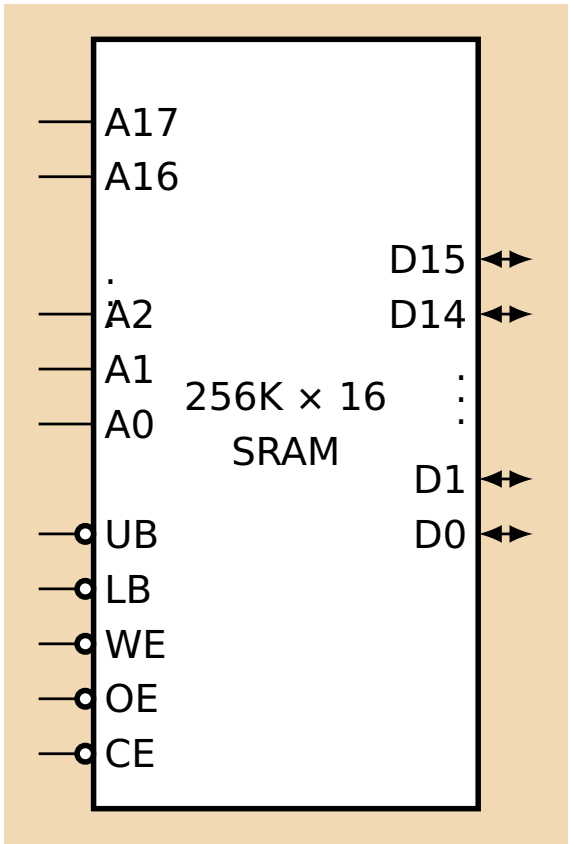

A12
A11
A2
A1
A0
CS1
CS2
WE
OE
6264
8K × 8
SRAM
D7
D6
D1
D0

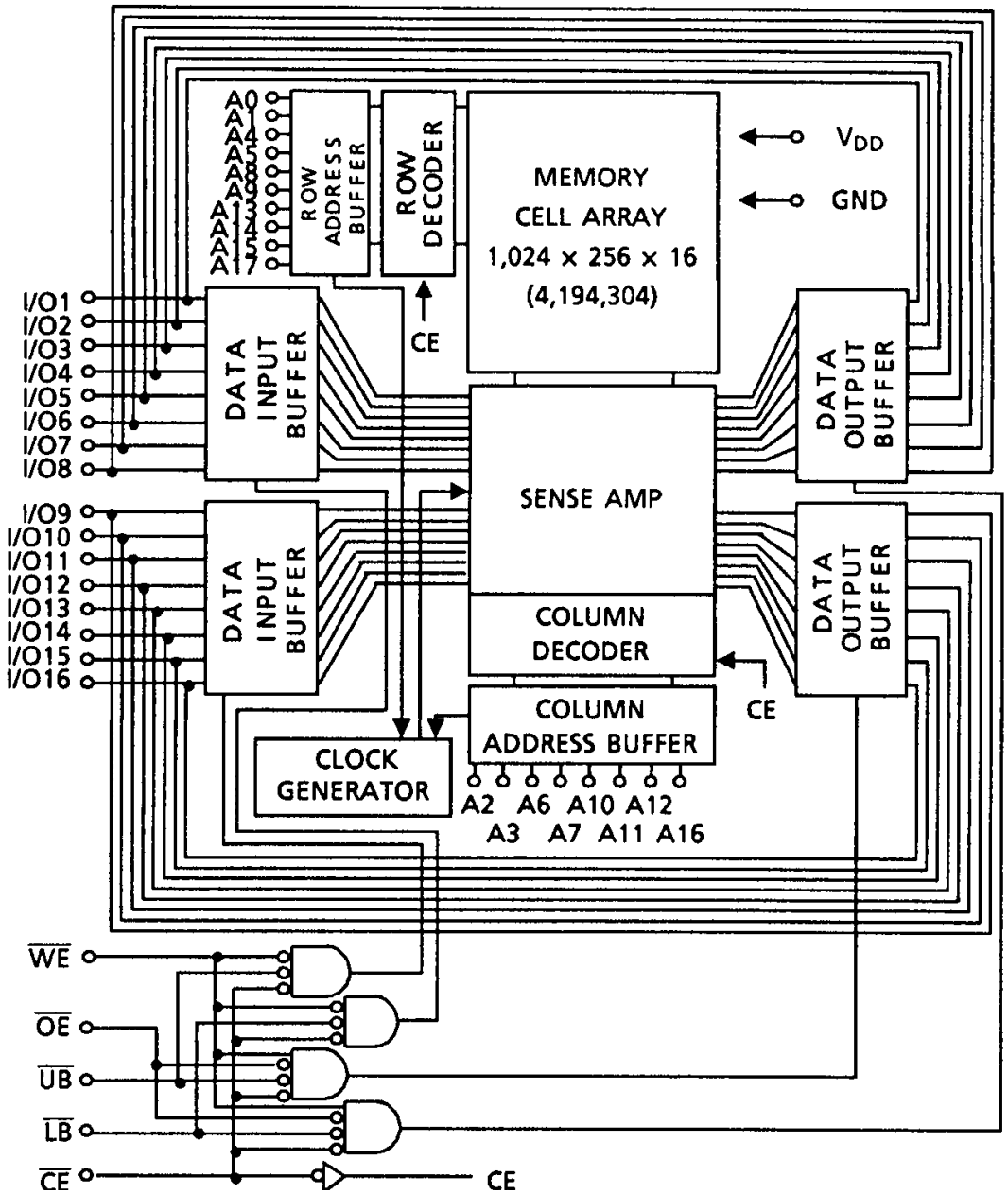

$\overline{CS1}$
CS2
$\overline{WE}$
$\overline{OE}$
Addr
Data
1
2
write 1
read 2

6264 SRAM Block Diagram

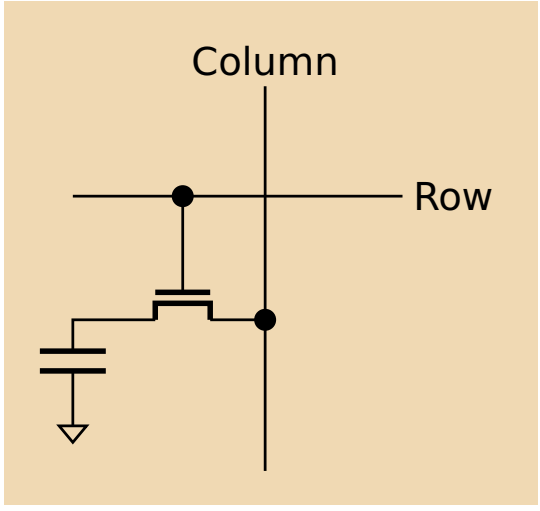


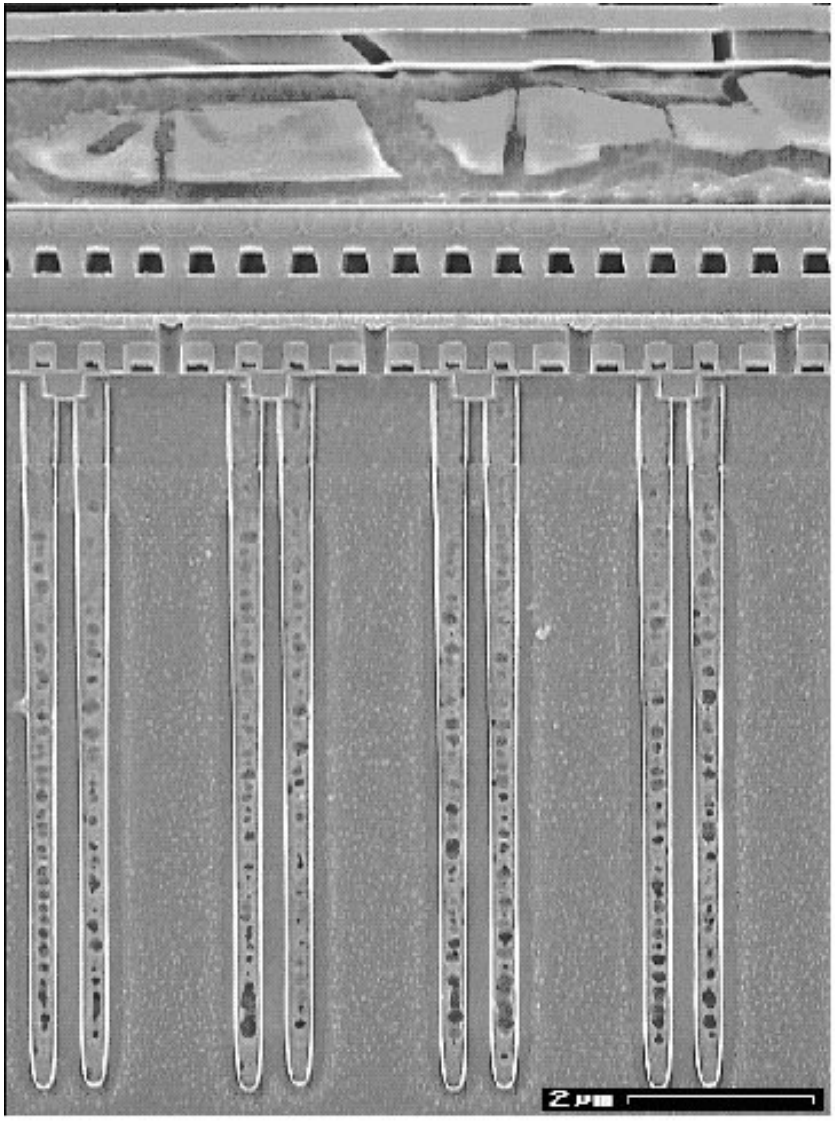
Toshiba TC55V16256J 256K × 16



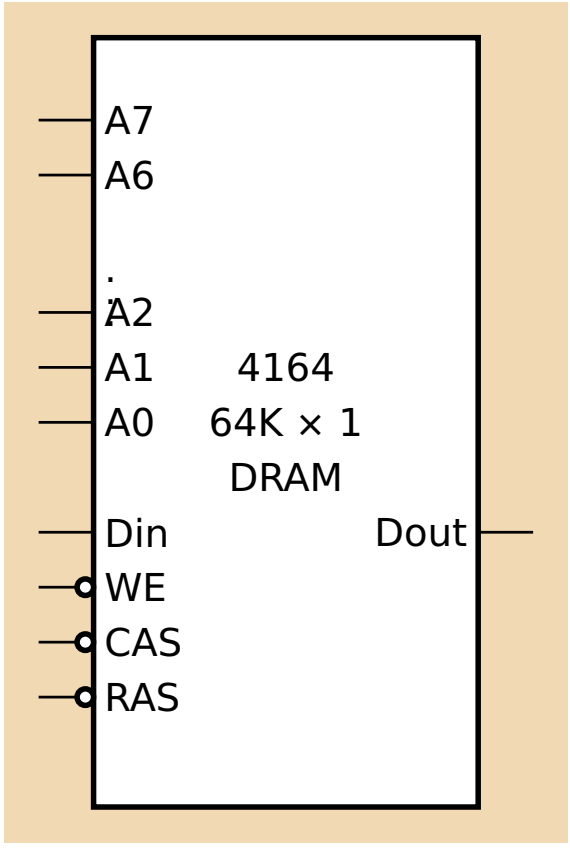


Dynamic RAM Cell

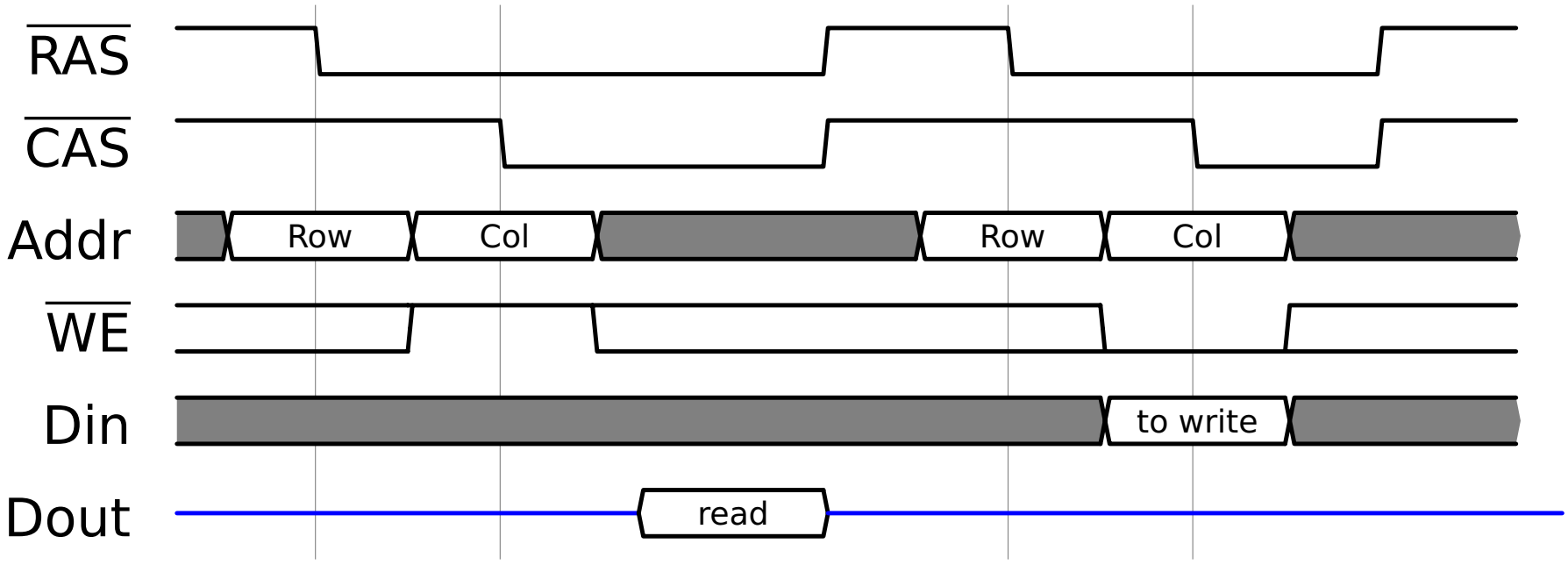




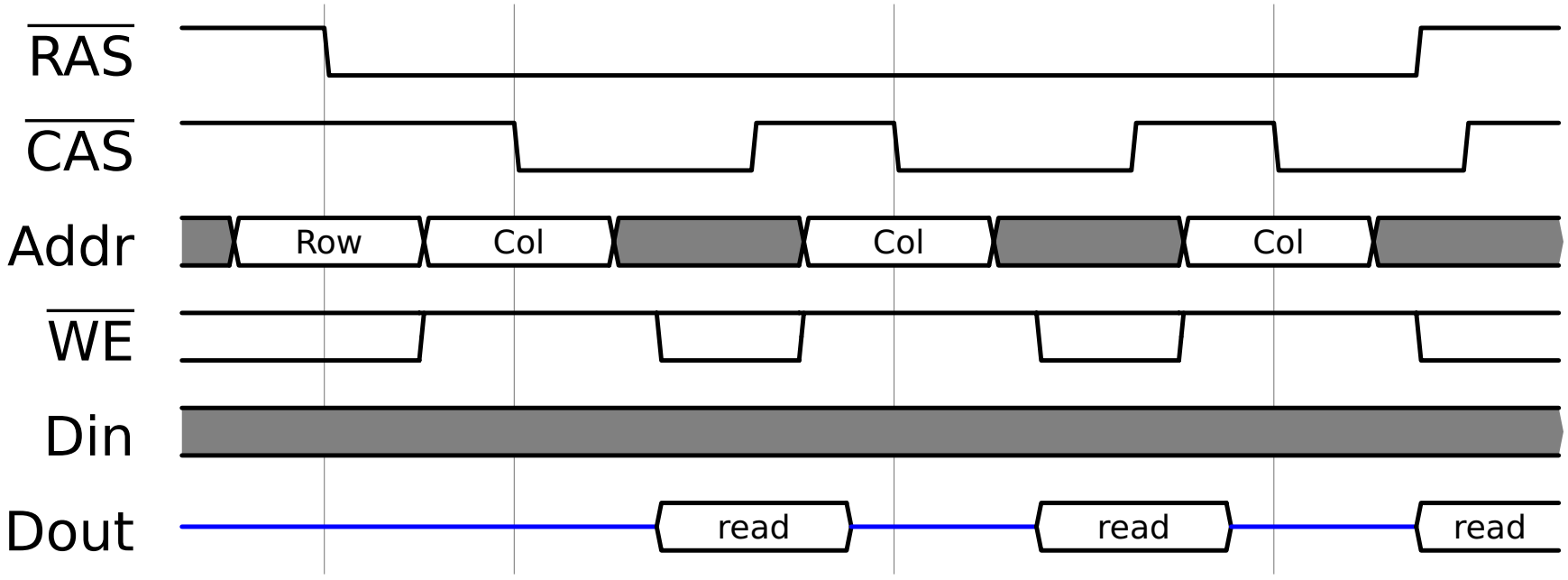
Ancient (c. 1982) DRAM: 4164 64K × 1



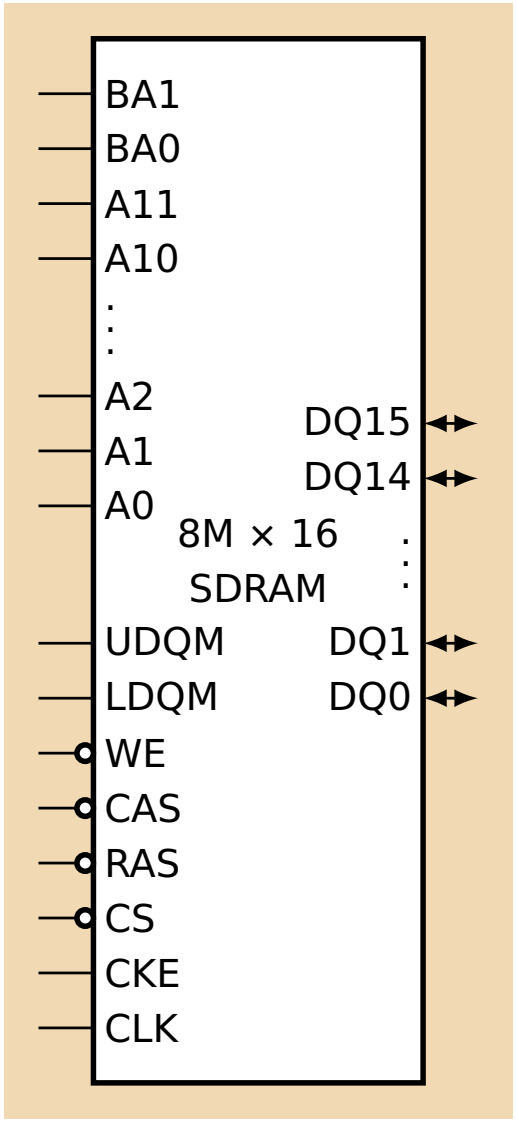
Basic DRAM read and write cycles

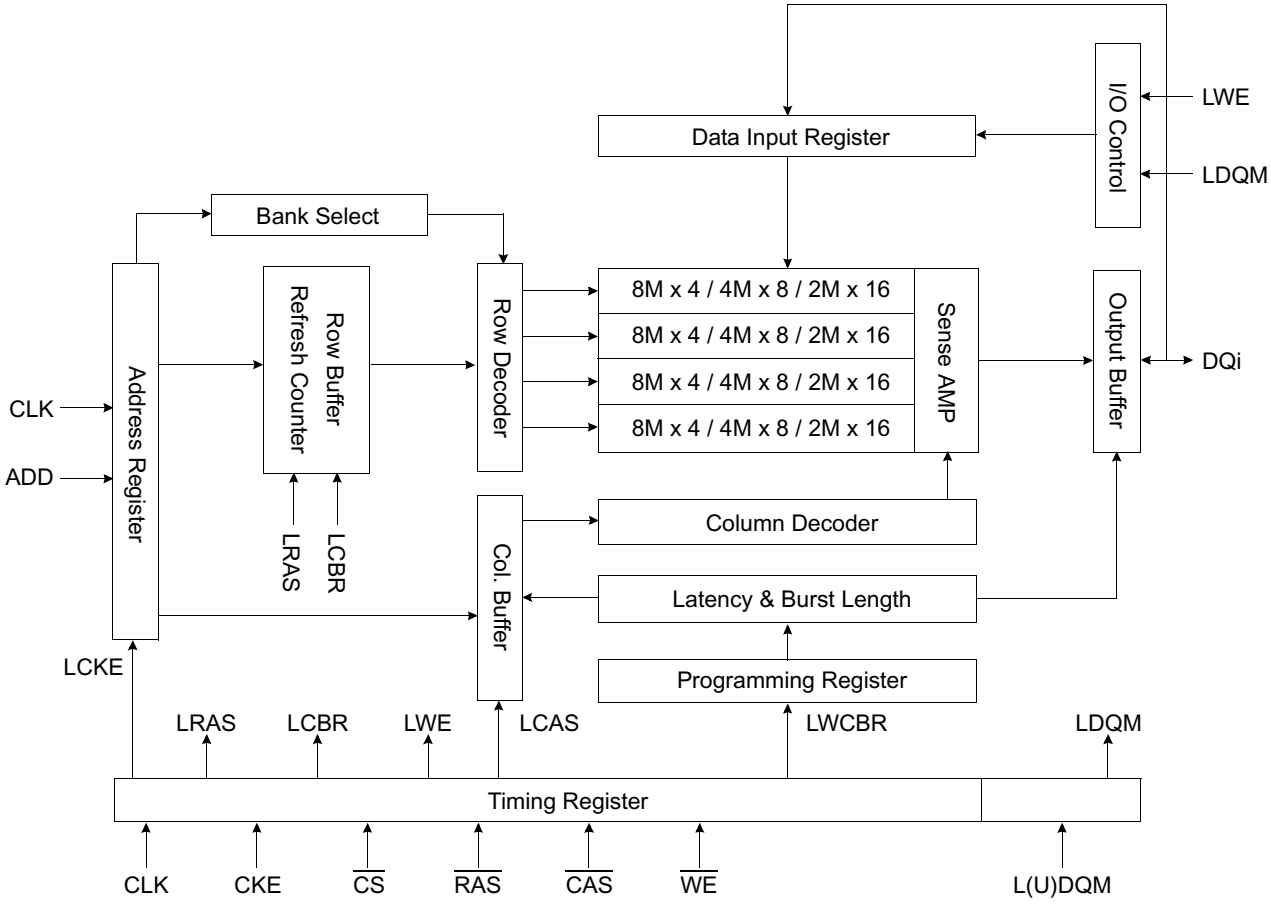


Page Mode DRAM read cycle



Samsung 8M × 16 SDRAM





SDRAM: Control Signals

$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Action
1	1	1	NOP
0	0	0	Load mode register
0	1	1	Active (select row)
1	0	1	Read (select column, start burst)
1	0	0	Write (select column, start burst)
1	1	0	Terminate Burst
0	1	0	Precharge (deselect row)
0	0	1	Auto Refresh

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write

SDRAM: Timing with 2-word bursts