# CSEE W3827

## Fundamentals of Computer Systems

## Homework Assignment 2

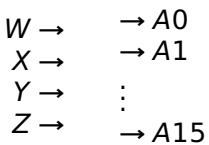
Profs. Stephen A. Edwards & Martha Kim

Columbia University

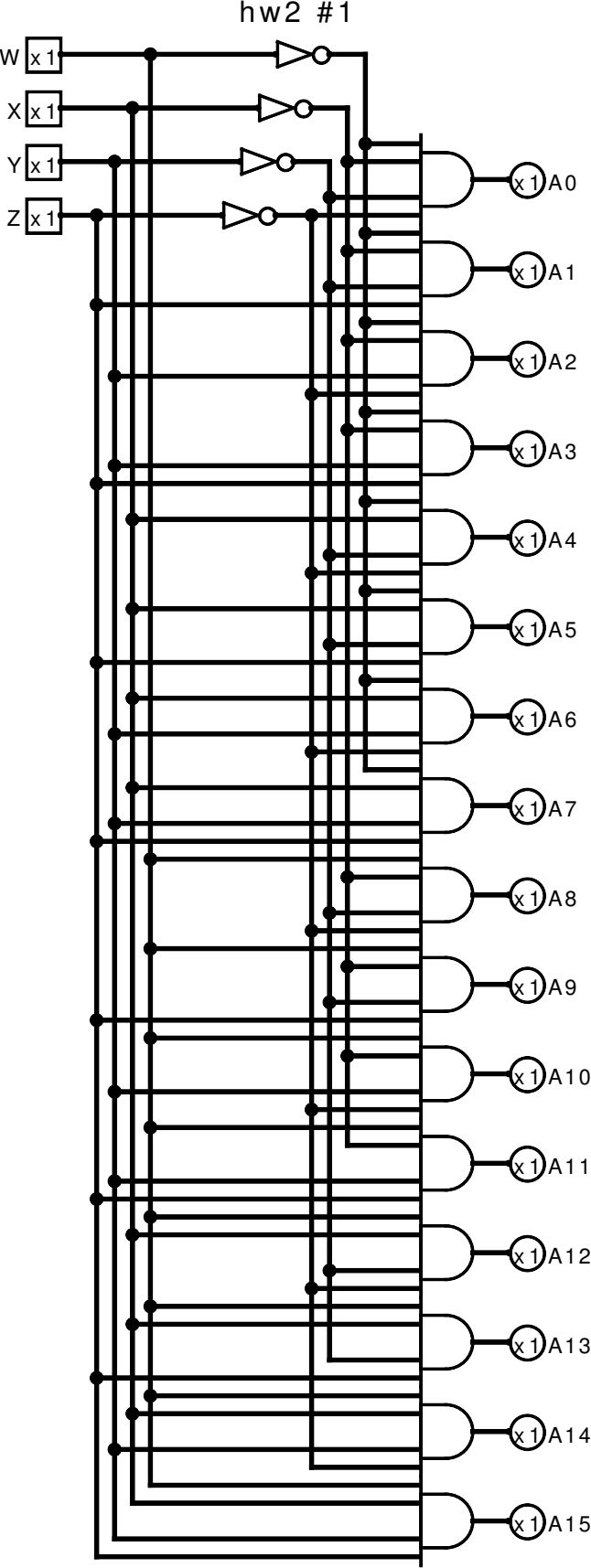
Due October 9, 2012 at 11:59 PM

Upload your solution to each problem as a Logisim .circ file to CourseWorks.

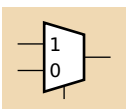
1. (20 pts.) Create a circuit for a 4-to-16 decoder using AND gates and inverters only. Arrange and name the inputs and outputs as shown below. Treat $W$ as the most significant bit and let $A0$ be true when all inputs are false. Only one of the outputs should ever be true.




Name your solution “hw2-1.circ” and submit it via Courseworks.


hw2 #1
W
X
Y
Z
x 1
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15

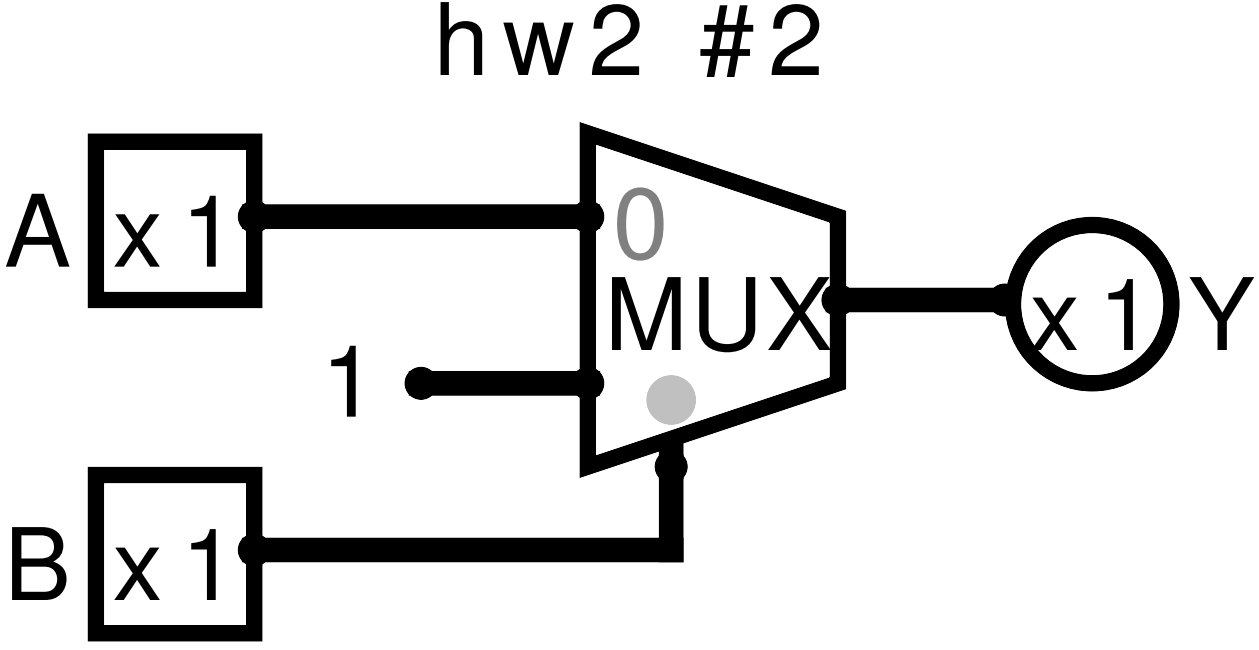
2. (10 pts.) In Logisim, implement the logical OR function using just a single two-input MUX (under “Plexers→Multiplexer”; set “include enable” to “no”) and constant “0” and “1” inputs (“Wiring→Constant”). Do not use additional gates.




Draw your inputs and outputs as shown below:

$$\begin{matrix} A \rightarrow \\ B \rightarrow \end{matrix} \qquad \rightarrow Y$$

Name your solution “hw2-2.circ” and submit it via Courseworks.


hw2 #2
A
x 1
0
MUX
1
x 1
Y
B
x 1

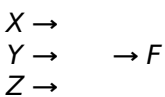
3. (15 pts.) In Logisim, implement $F = \overline{X}\,\overline{Y}\,\overline{Z} + \overline{Y}Z + X\overline{Y}$ using just constants and

   (a) a 3-to-8 decoder (under "Plexers→Decoder." Set "include enable" to "No" and note the input wires are a bundle at the bottom) and an OR gate;

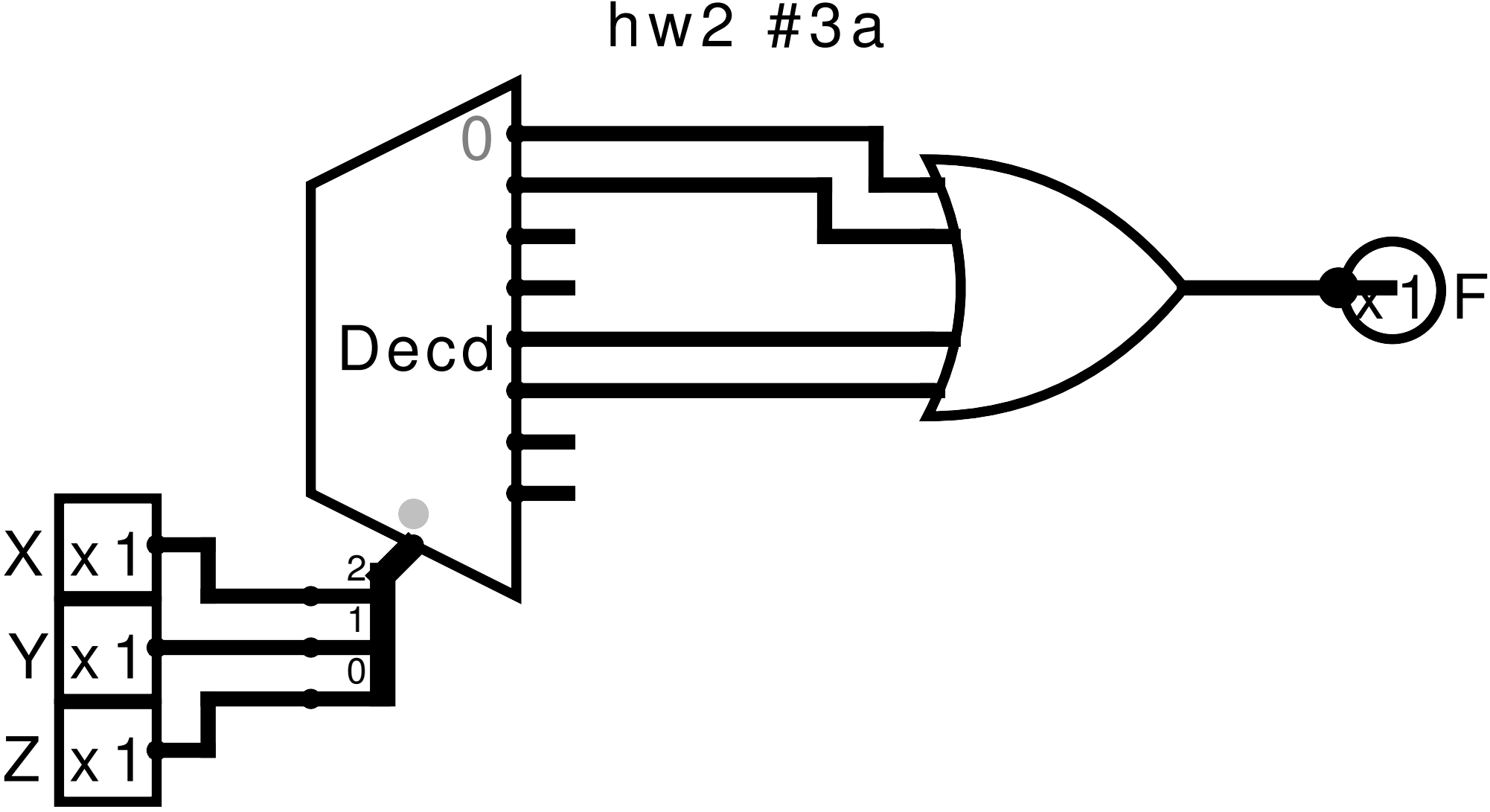
   (b) an 8 input mux; and

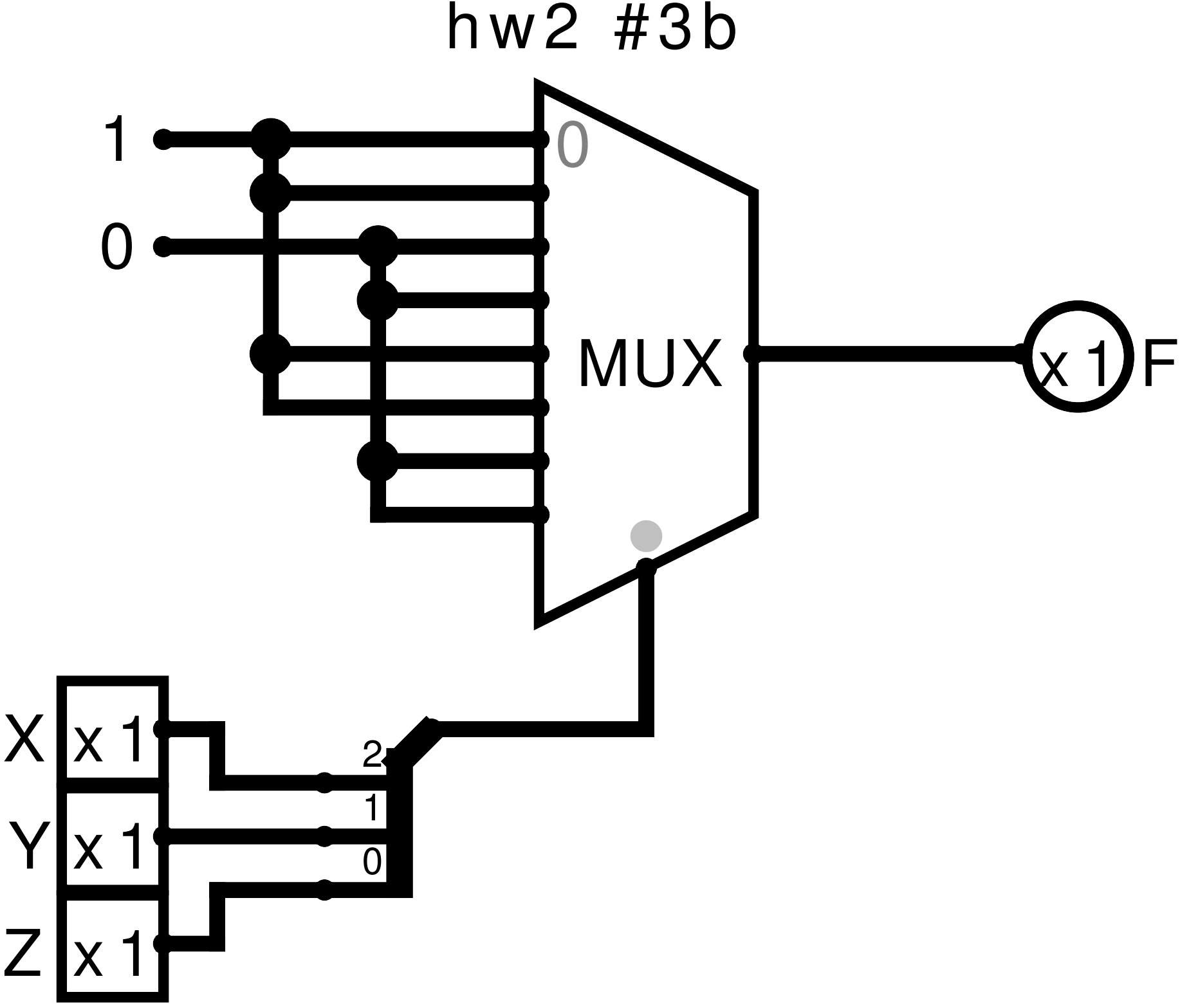
   (c) a 4 input mux whose select inputs are $X$ and $Y$, and an inverter.

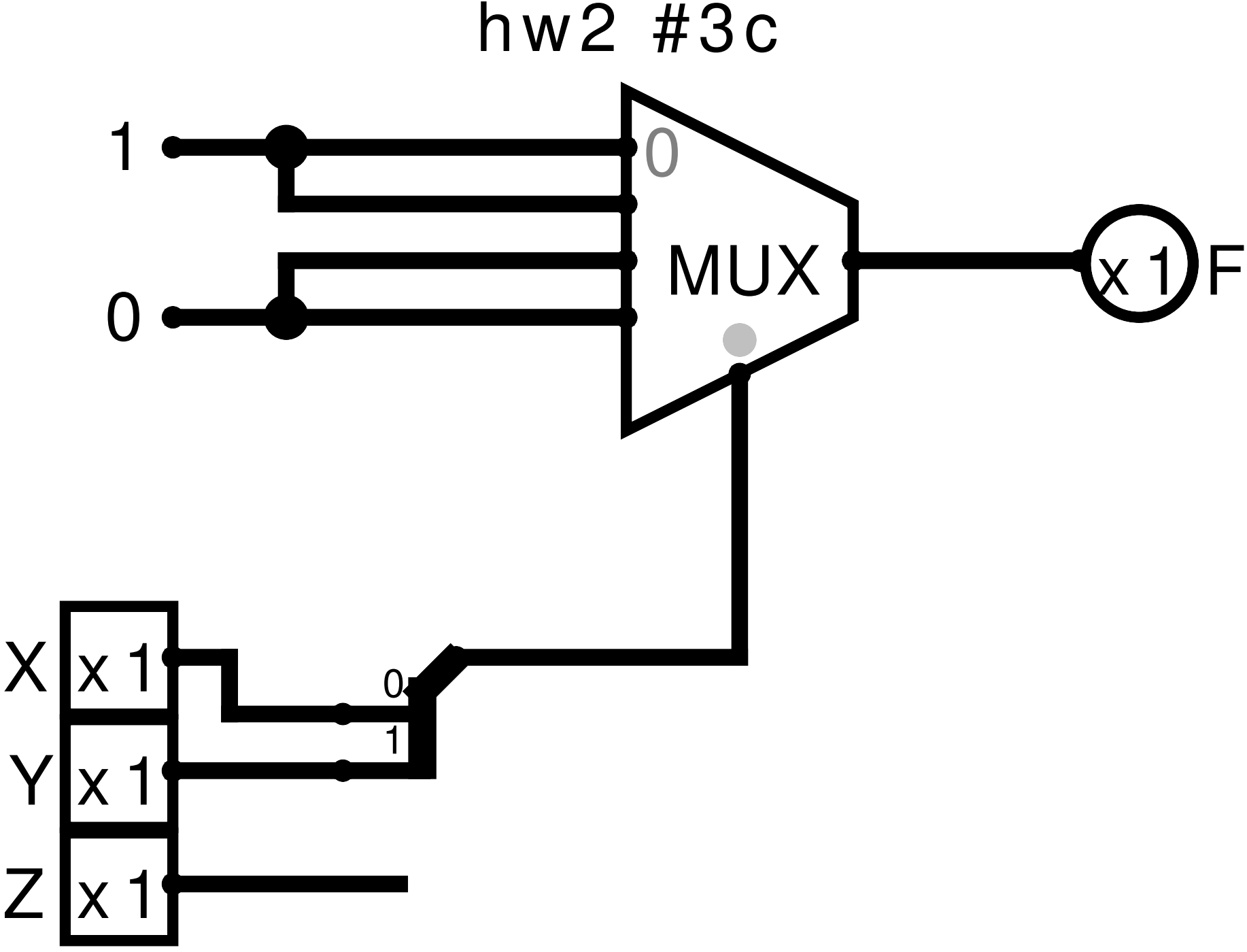
   Arrange your inputs and outputs as shown below and name your files "hw2-3a.circ," "hw2-3b.circ," and "hw2-3c.circ."



# hw2 #3a

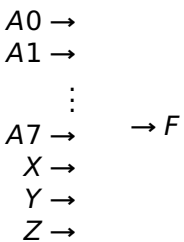



hw2 #3b
1
0
0
MUX
x 1
F
X
x 1
Y
x 1
Z
x 1
2
1
0


hw2 #3c
1
0
0
MUX
x 1
F
X
x 1
Y
x 1
Z
x 1
0
1

4. (20 pts.) Implement an eight-input mux using three four-input muxes and no other gates (constants are OK).

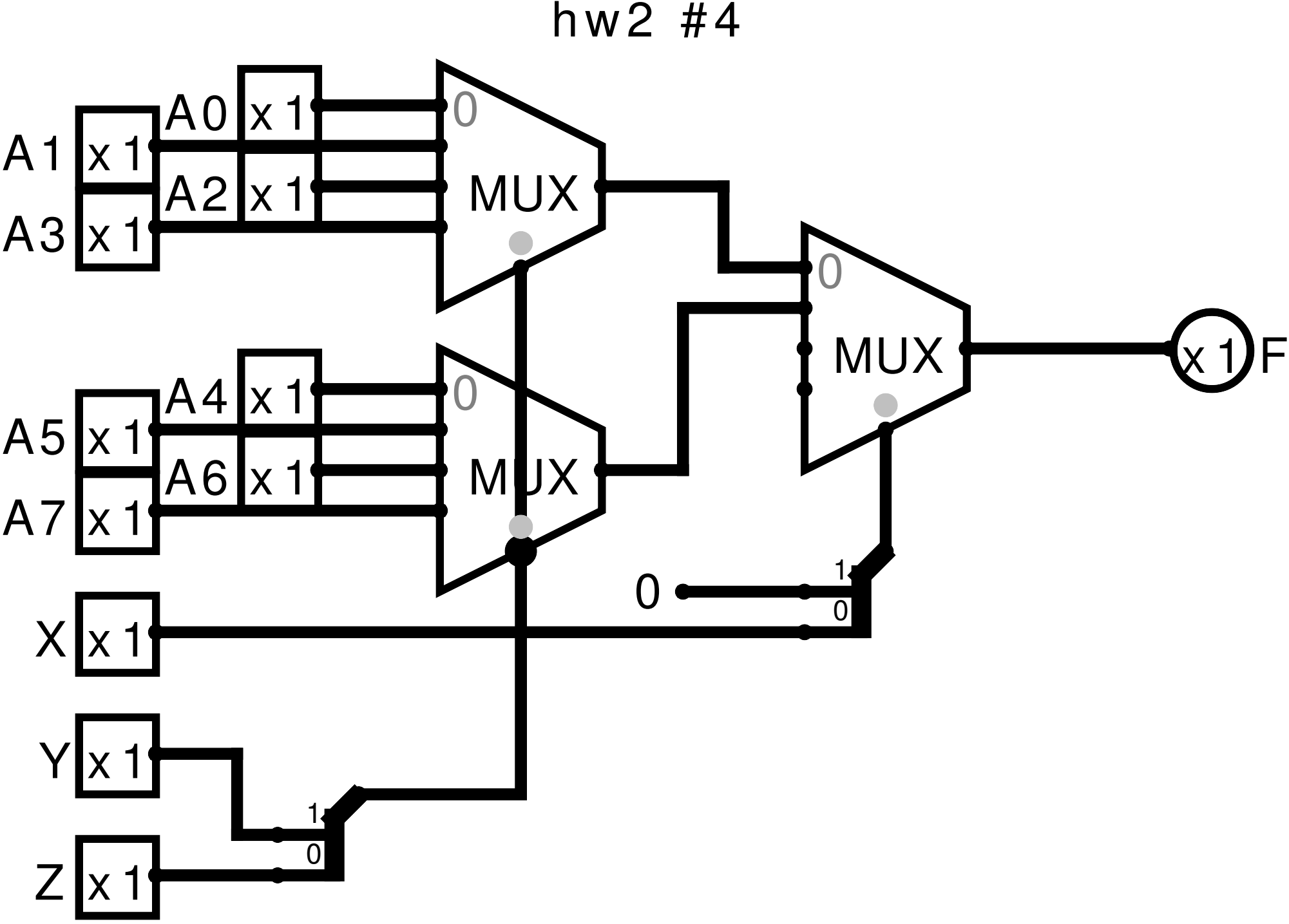
   Arrange your inputs and outputs as shown below and name your solution “hw2-4.circ”



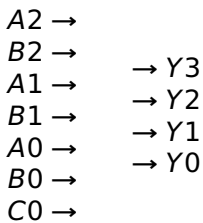

   Here, $A0$ through $A7$ are the eight inputs, and $X$, $Y$, and $Z$ are the three selects. $X$ is the most significant bit, selecting between, e.g., $A0$ and $A4$.

   Name your solution “hw2-4.circ.”

# hw2 #4


A0
x 1
A1
x 1
A2
x 1
A3
x 1
0
MUX
A4
x 1
A5
x 1
A6
x 1
A7
x 1
0
MUX
0
MUX
x 1
F
1
0
0
X
x 1
Y
x 1
1
0
Z
x 1

5. (35 pts.) Implement a three-bit binary carry-lookahead adder "hw2-5.circ." $A0$ through $A2$ and $B0$ through $B2$ are the two binary inputs ($A0$ and $B0$ are the LSBs), $C0$ is the carry in, and $Y0$ through $Y3$ is the four-bit output. Arrange your inputs and outputs like this:



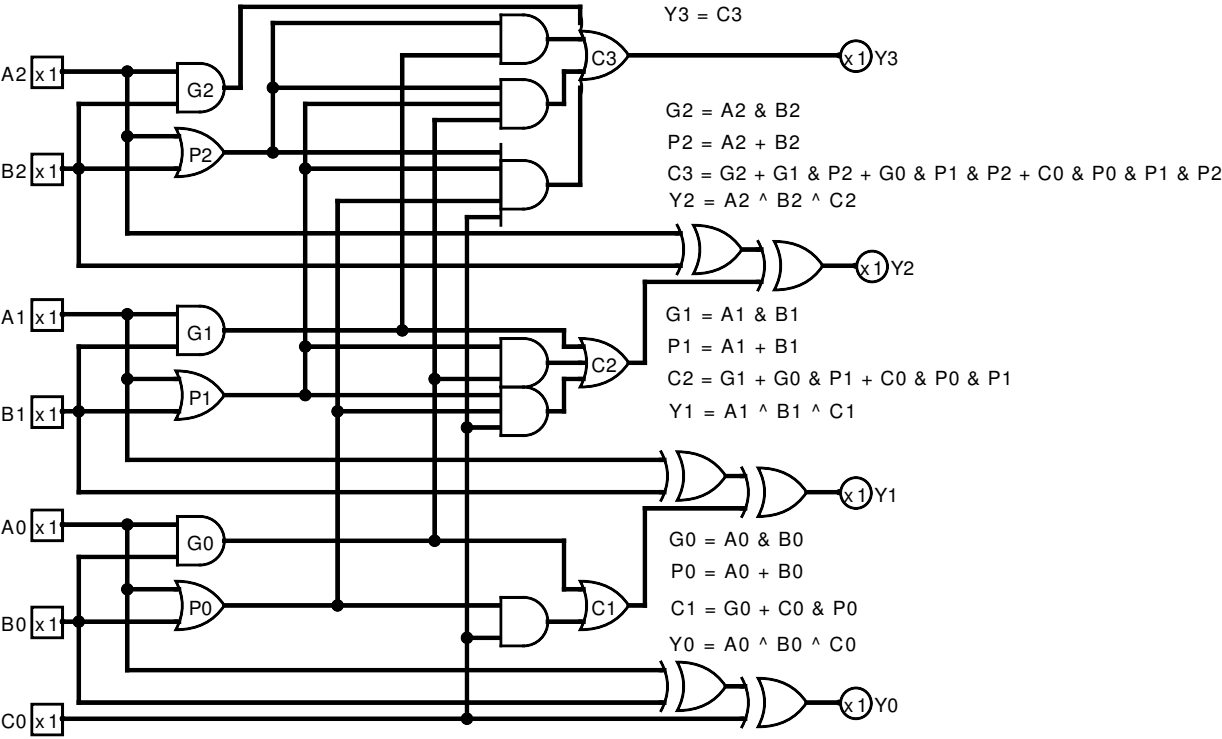

(a) As text labels in your solution, write expressions for $G_0, \ldots, G_2$ and $P_0, \ldots, P_2$, the carry generate and propagate functions, in terms of the inputs.

(b) Write sum-of-product expressions for $C_1, \ldots, C_3$ in terms of the $G$'s, $P$'s, and $C_0$. Use + for OR, & for AND, and ! for NOT.

(c) Write the equations for the $Y$'s in terms of these. Use ^ for XOR.

(d) Implement the carry-lookahead adder circuit corresponding to these equations using inverters, AND, NAND, OR, NOR, and

# hw2 #5


A2
B2
A1
B1
A0
B0
C0
x 1
G2
P2
G1
P1
G0
P0
C3
C2
C1
Y3
Y2
Y1
Y0
Y3 = C3
G2 = A2 & B2
P2 = A2 + B2
C3 = G2 + G1 & P2 + G0 & P1 & P2 + C0 & P0 & P1 & P2
Y2 = A2 ^ B2 ^ C2
G1 = A1 & B1
P1 = A1 + B1
C2 = G1 + G0 & P1 + C0 & P0 & P1
Y1 = A1 ^ B1 ^ C1
G0 = A0 & B0
P0 = A0 + B0
C1 = G0 + C0 & P0
Y0 = A0 ^ B0 ^ C0