Verishort

Verilog for the Traditional Programmer

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Motivation

Verilog syntax is cryptic We love Java and C

```
1  module _gcd(_clock, _reset, _num0, _num1, _start, _greatest);
2  input _clock;
3  input _reset;
4  input [7:0] _num0;
5  input [7:0] _num1;
6  input _start;
7  output [7:0] _greatest;
8  reg [7:0] __reg_greatest;
9
10 reg _found;
11
12 assign _greatest[7:0] = __reg_greatest[7:0];
13 always @ (*) begin
14 if (_start)
15 begin
16 if ((_num0[7:0]<_num1[7:0]))
17 begin
18 __reg_greatest[7:0]=_num0[7:0];
19 end
20 else
21 begin
22 __reg_greatest[7:0]=_num1[7:0];
23 end
24 end
25 else
26 begin
27 end
28 if (_reset) begin
29 __reg_greatest= 0;
30 _found= 0;
31 end
32 end
33 always @ (posedge _clock) begin
34 if ((~_found))
35 begin
36 if ((((_num0[7:0]%_greatest[7:0])==0)&((_num1[7:0]%_greatest[7:0])==0)))
37 begin
38 _found=1;
39 end
40 else
41 begin
42 __reg_greatest[7:0]=(_greatest[7:0]-1);
43 end
44 end
45 else
46 begin
47 end
48 end
49 always @ (negedge _clock) begin
50 end
51 endmodule
```

```
1  module gcd(input num0[8], num1[8], start; output greatest[8]) {
2      register found;
3
4      if (start) {
5          if (num0<num1) {
6              greatest = num0;
7              }
8          else {
9              greatest = num1;
10             }
11         }
12
13     if (posedge) {
14         if (~found) {
15             if (num0%greatest==0 & num1%greatest==0) {
16                 found = 1;
17                 }
18             else {
19                 greatest = greatest -1;
20                 }
21             }
22         }
23
24     }
```

Motivation

- Describing hardware with sequence of instructions
- Complex syntax
- Paradigms unlike true programming languages
- Subset of Verilog for basic use
- Reduce verbosity

Implementation

- Translator
- Multiple ASTs
- Standard testbench

- Verilog is syntactically inflexible
- Add'l structures created from Verishort code
- Intermediate AST contains add'l info

Misunderestimating the Language

- Bus widths
- Sign extensions
- Conditional statements
- New intermediate AST
- Extra variables
- Clock edges
- Closer to Verilog