



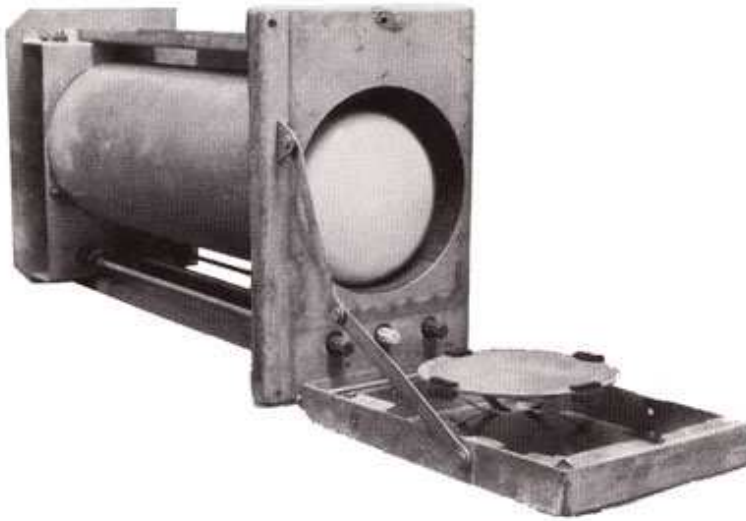
# Memory

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Spring 2010

# Early Memories



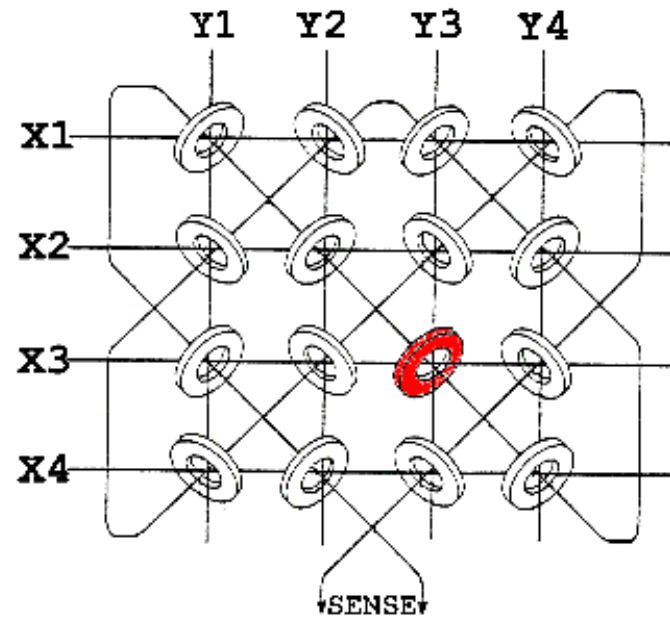
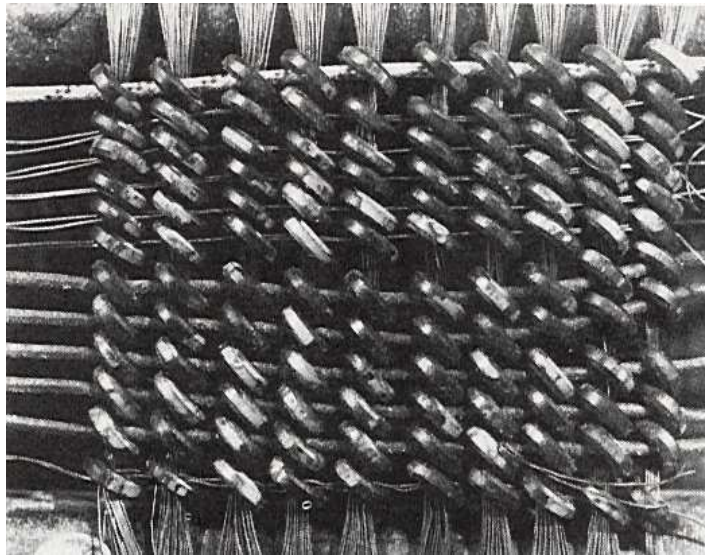
Williams Tube CRT-based random access memory, 1946. Used on the Manchester Mark I. 2048 bits.

# Early Memories



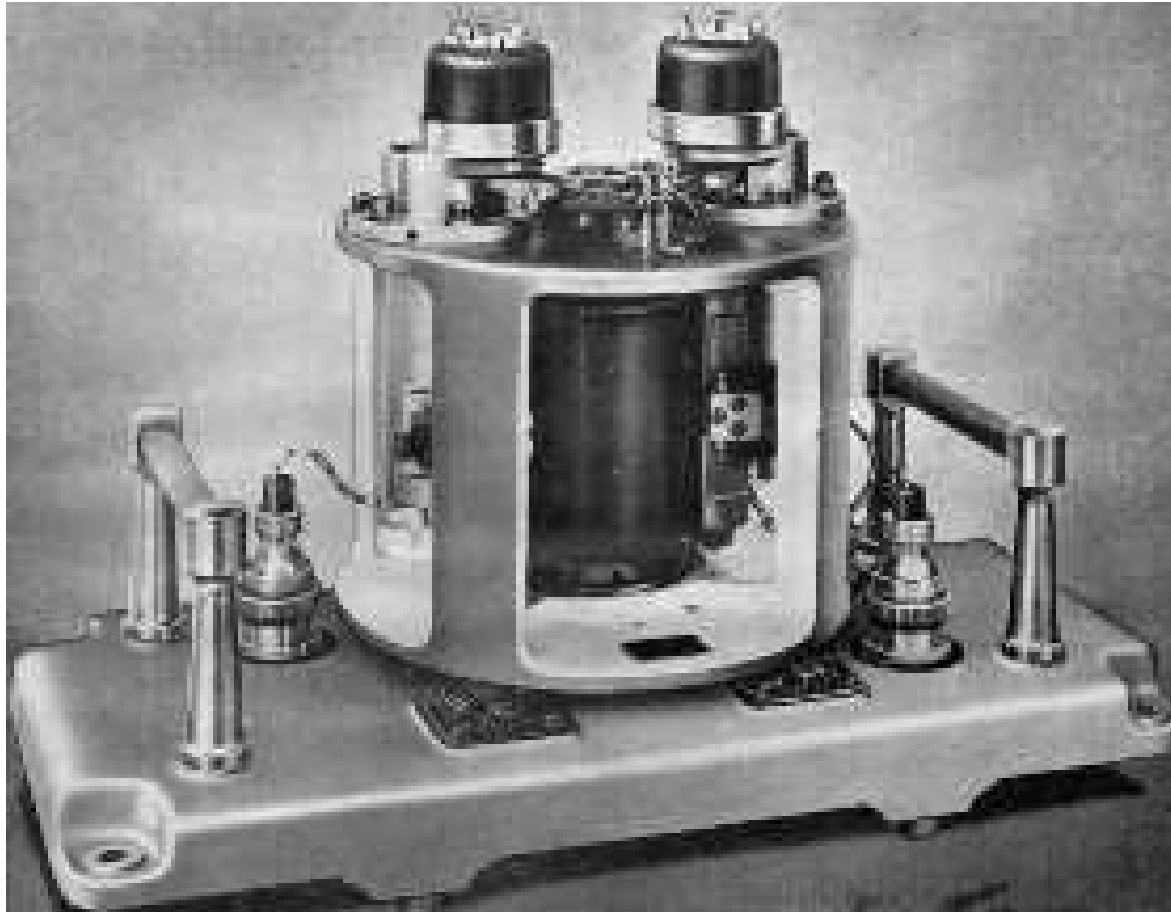
Mercury acoustic  
delay line.  
Used in the EDASC,  
1947.  
 $32 \times 17$  bits

# Early Memories



Magnetic core memory, 1952. IBM.

# Early Memories



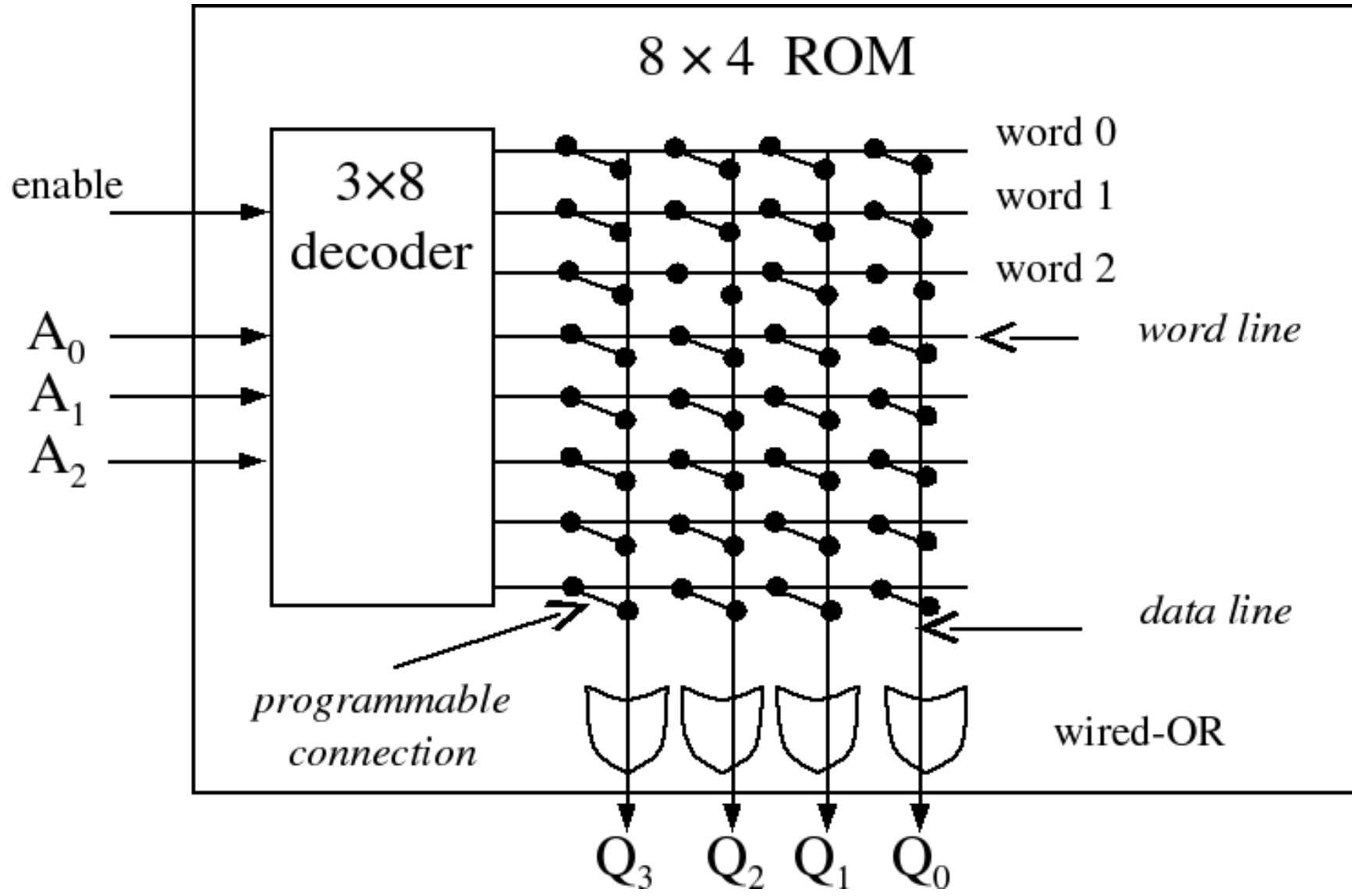
Magnetic drum memory. 1950s & 60s.  
Secondary storage.

# Modern Memory Choices



Family	Programmed	Persistence
Mask ROM	at fabrication	$\infty$
PROM	once	$\infty$
EPROM	1000s, UV	10 years
FLASH	1000s, block	10 years
EEPROM	1000s, byte	10 years
NVRAM	$\infty$	5 years
SRAM	$\infty$	while powered
DRAM	$\infty$	64 ms

# ROMs

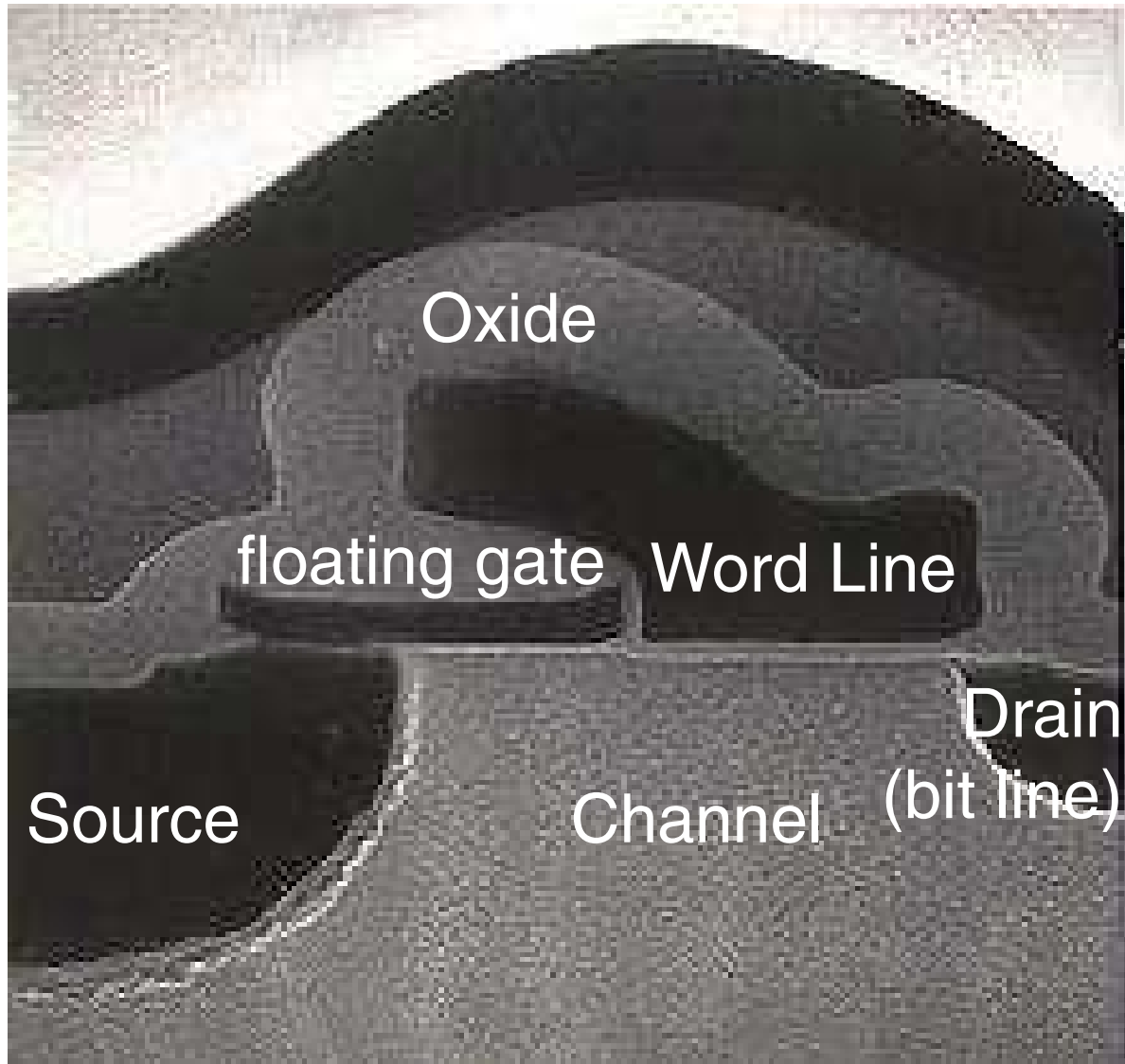


# EPROMs





# EEPROM and FLASH



Slow write

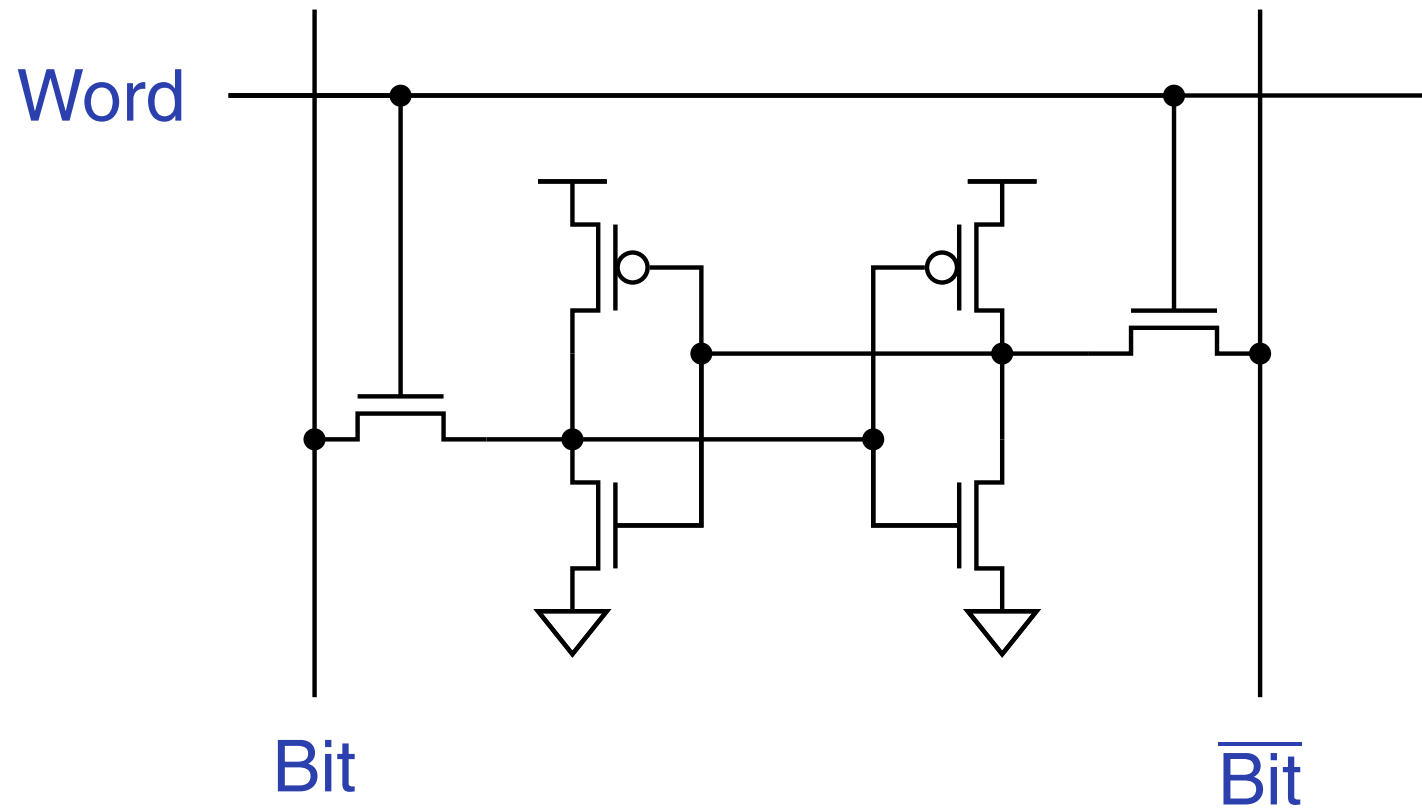
Fowler-Nordheim Tunneling

EEPROM: bit at a time

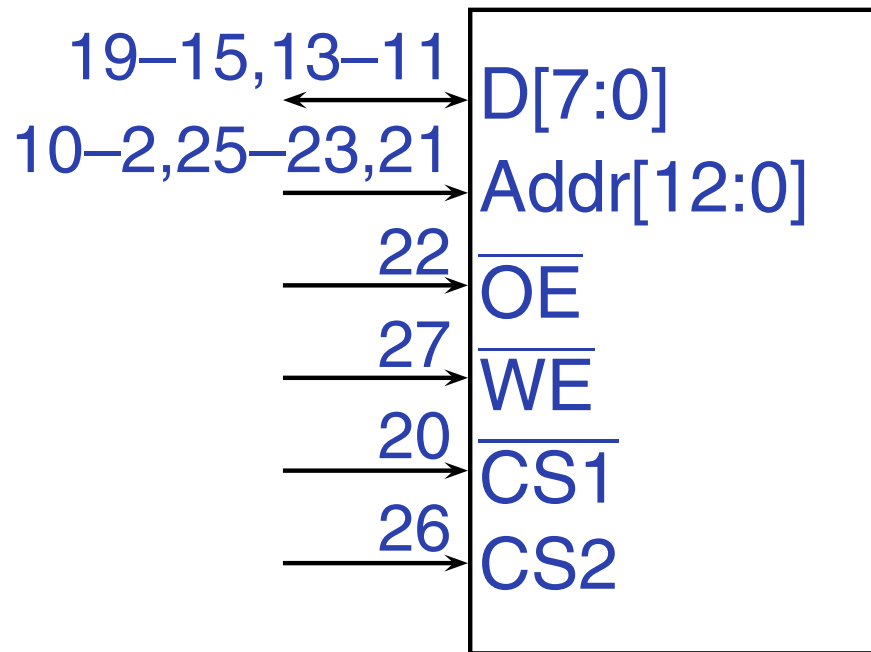
FLASH: block at a time

Source: SST

# Static RAM Cell



# Standard SRAM: 6264

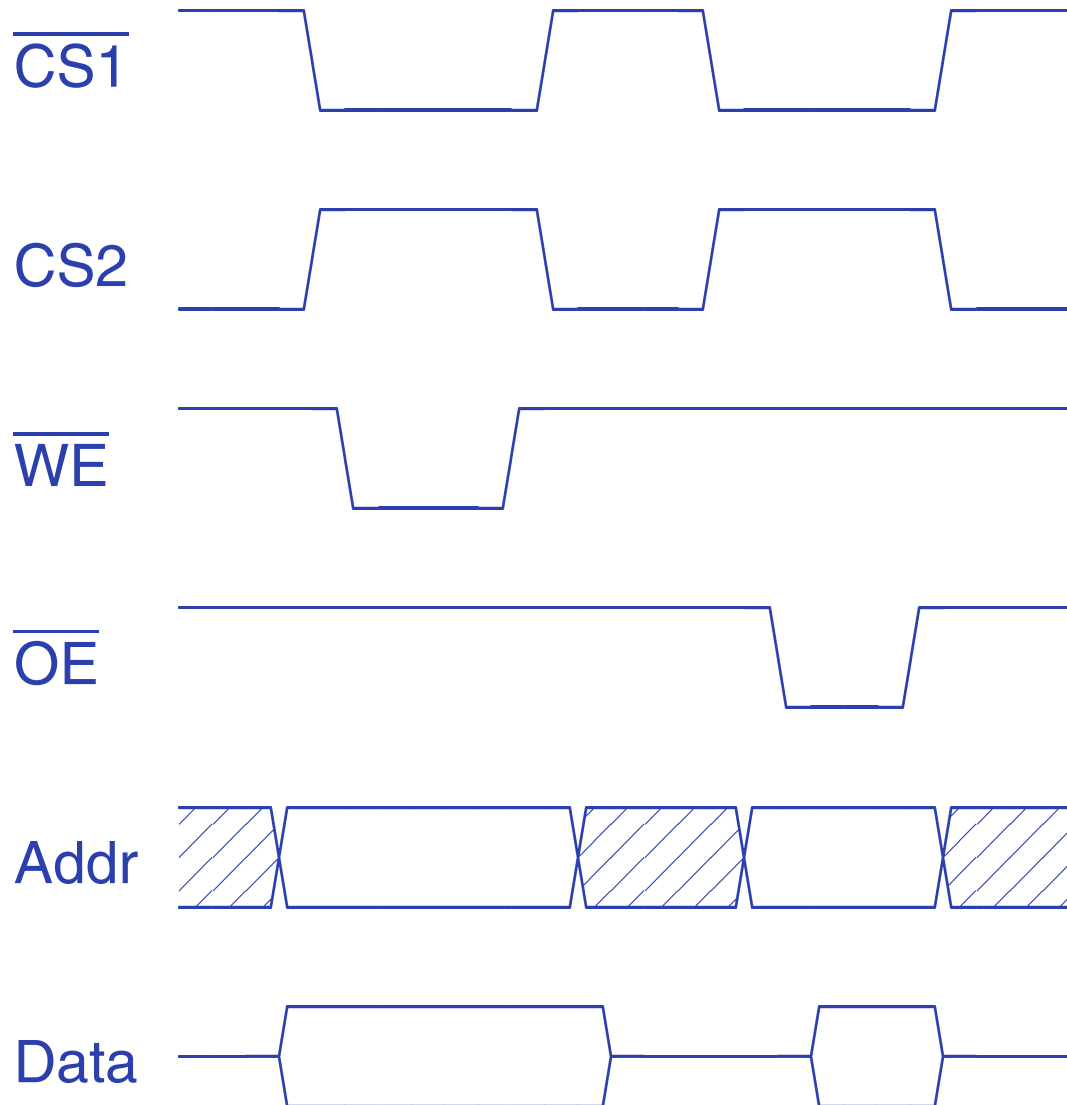


8K × 8

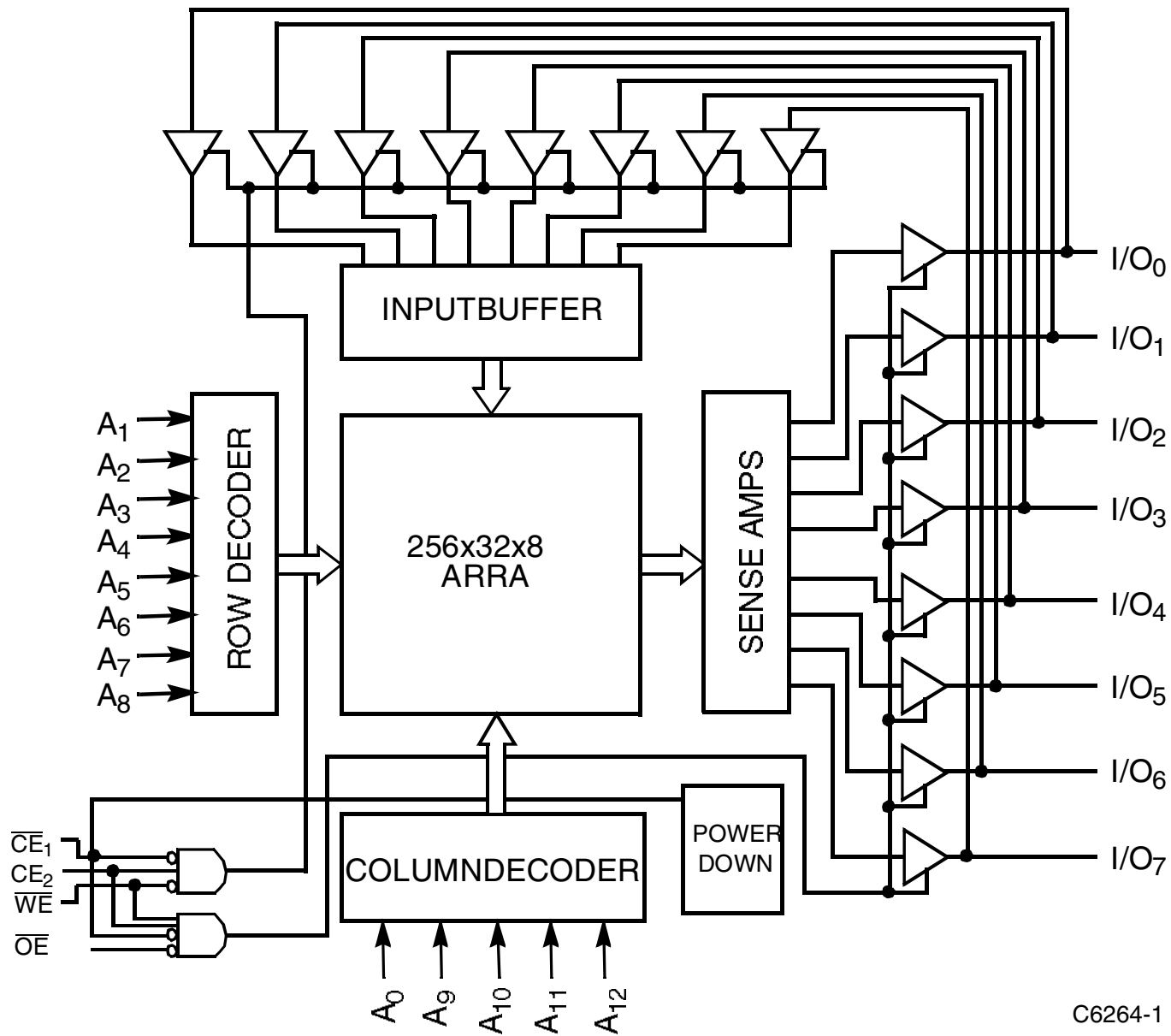
Can be very fast:  
Cypress sells a 55ns  
version

Simple, asynchronous  
interface

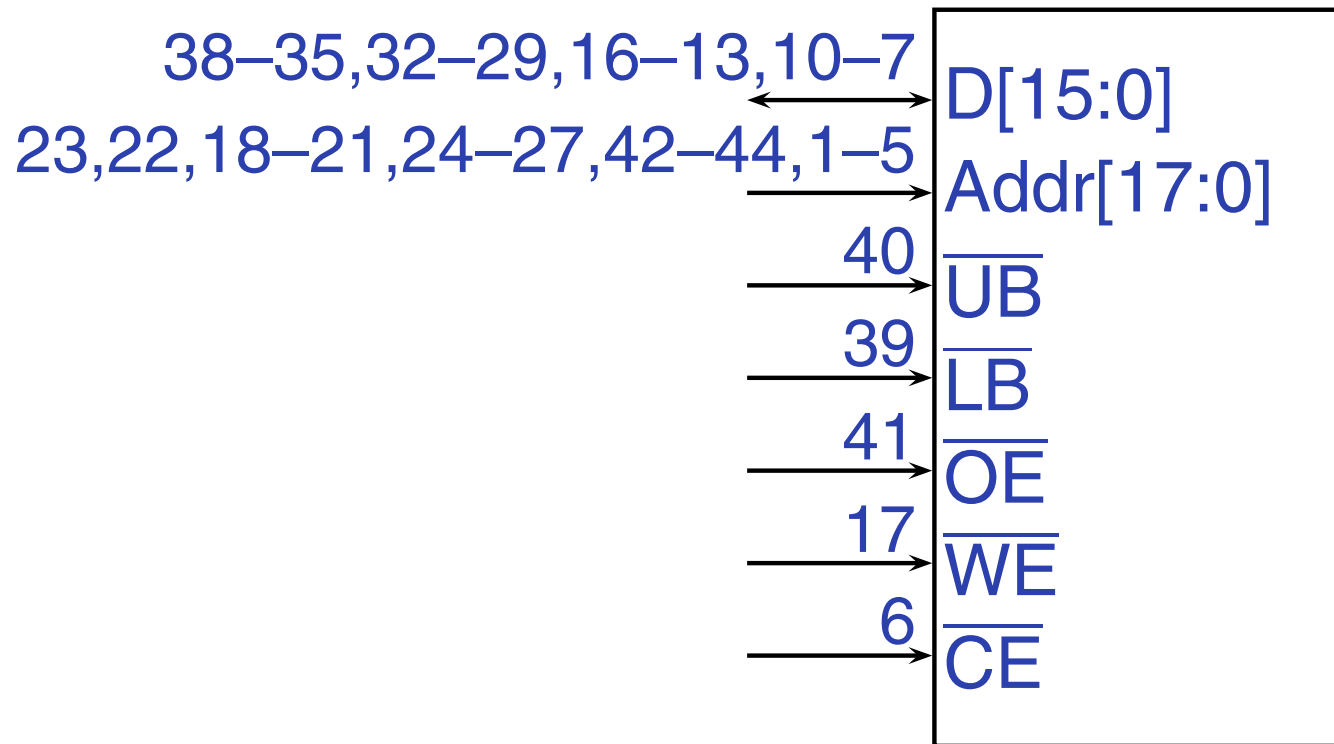
# Standard SRAM: 6264



# Standard SRAM: 6264



# Toshiba TC55V16256J 256K × 16

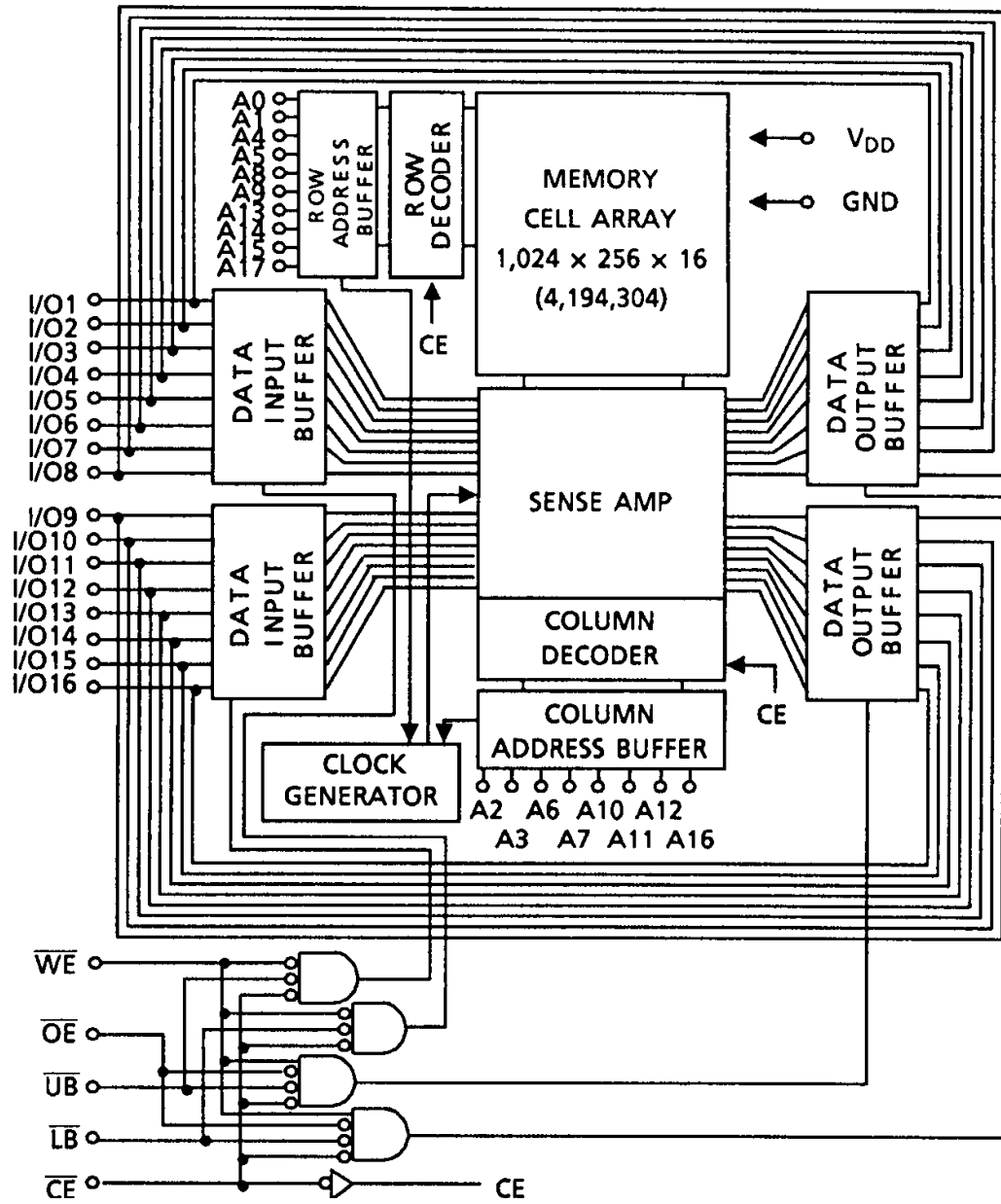


12 or 15 ns access time

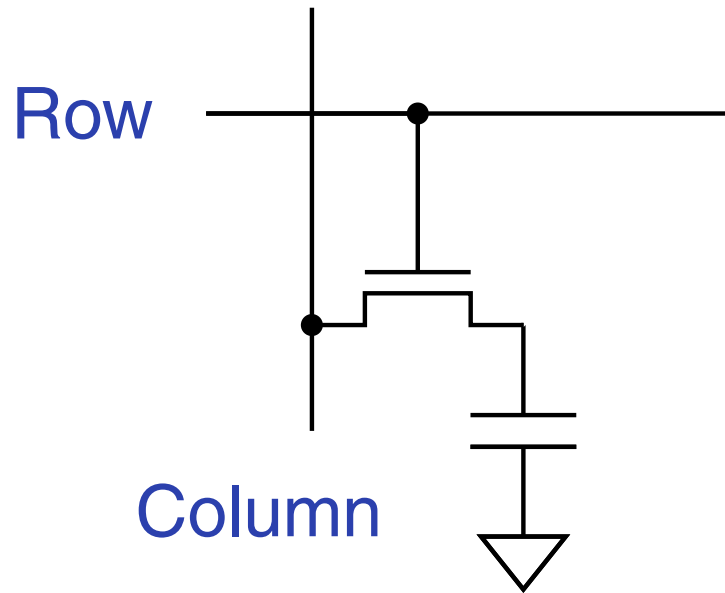
Asynchronous interface

$\overline{UB}$ ,  $\overline{LB}$  select bytes

# Toshiba TC55V16256J 256K × 16



# Dynamic RAM Cell



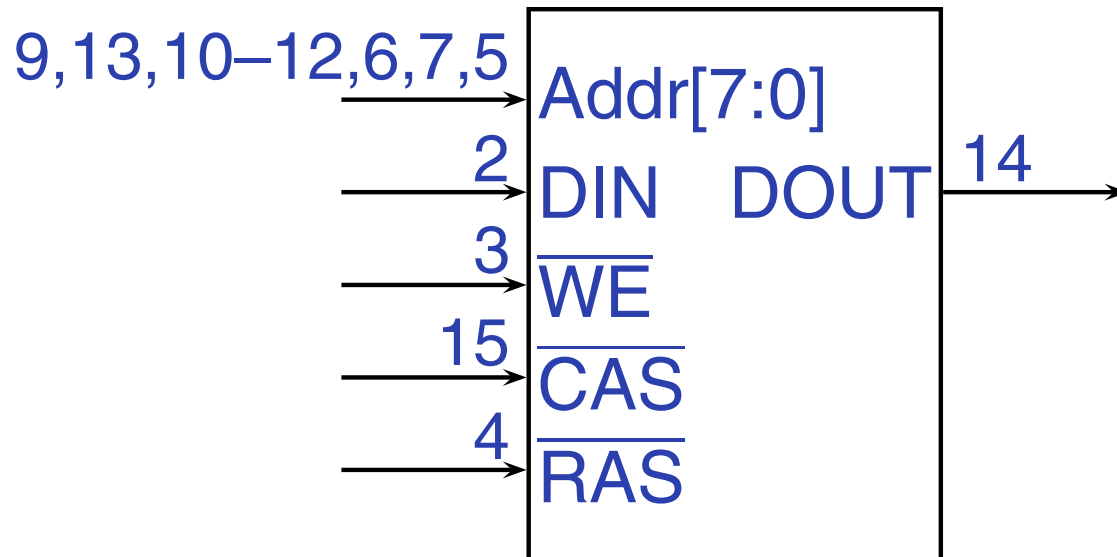
Basic problem: Leakage

Solution: Refresh

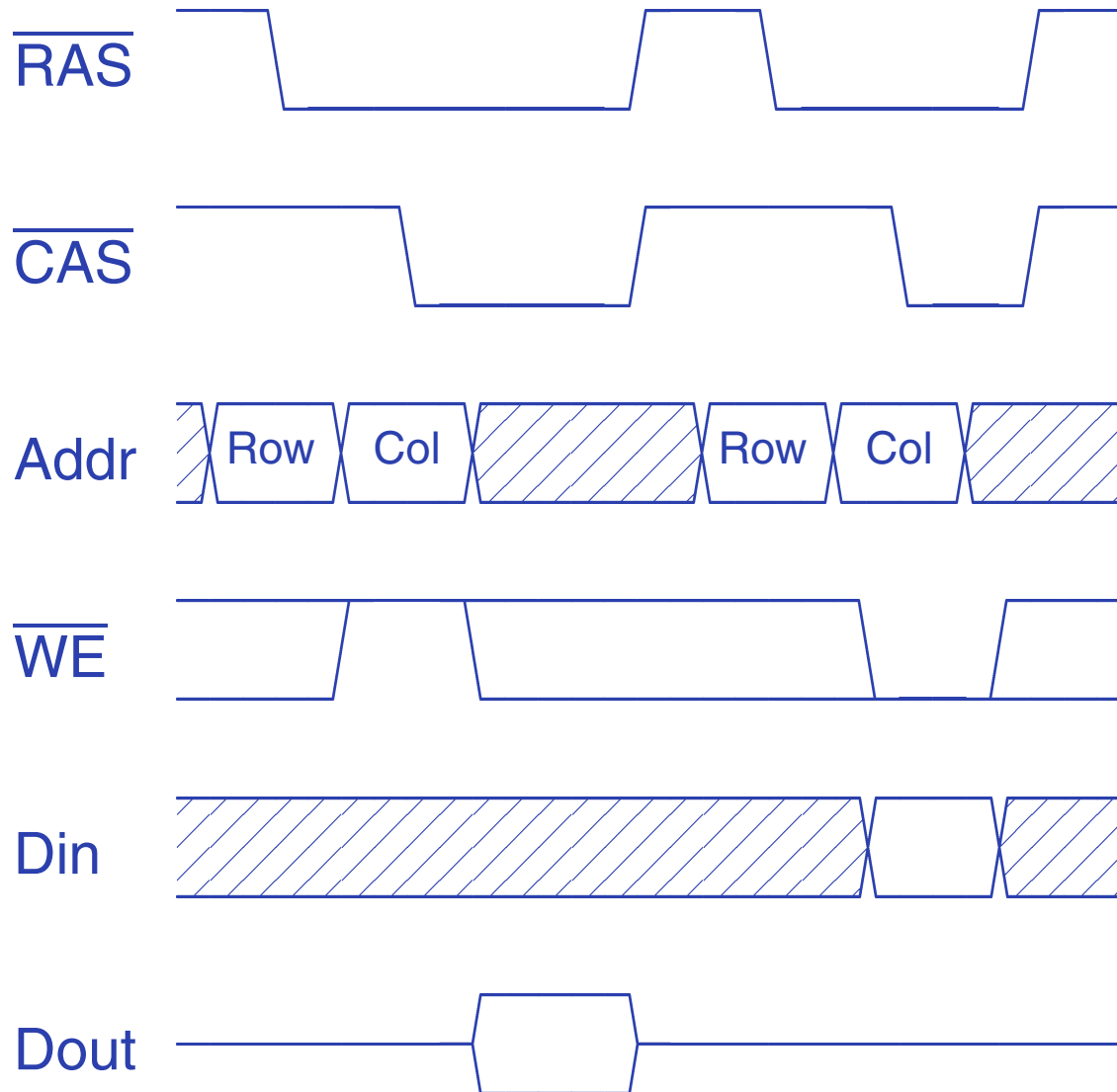


# Ancient DRAM: 4164

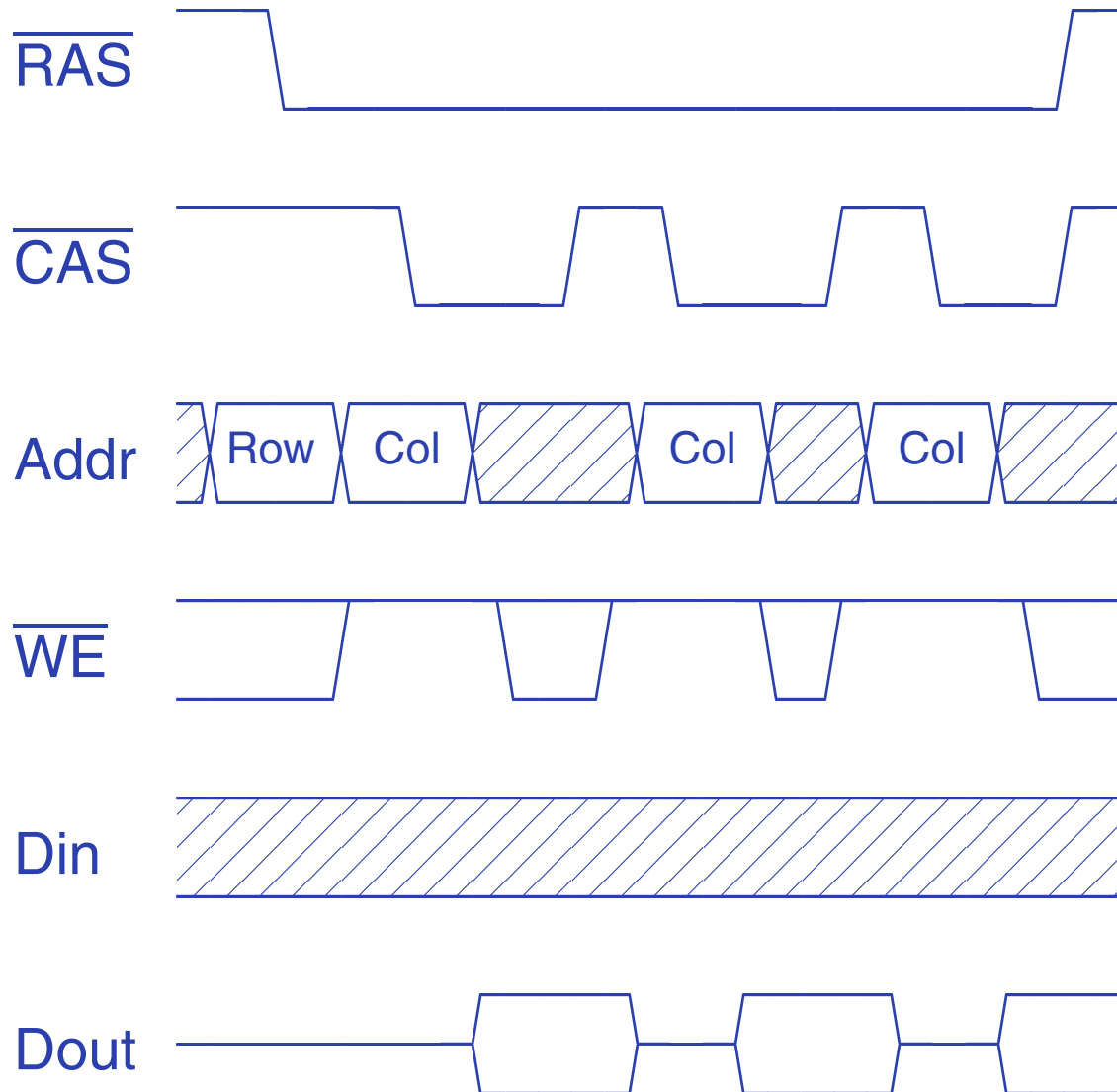
64K × 1  
Apple IIe vintage



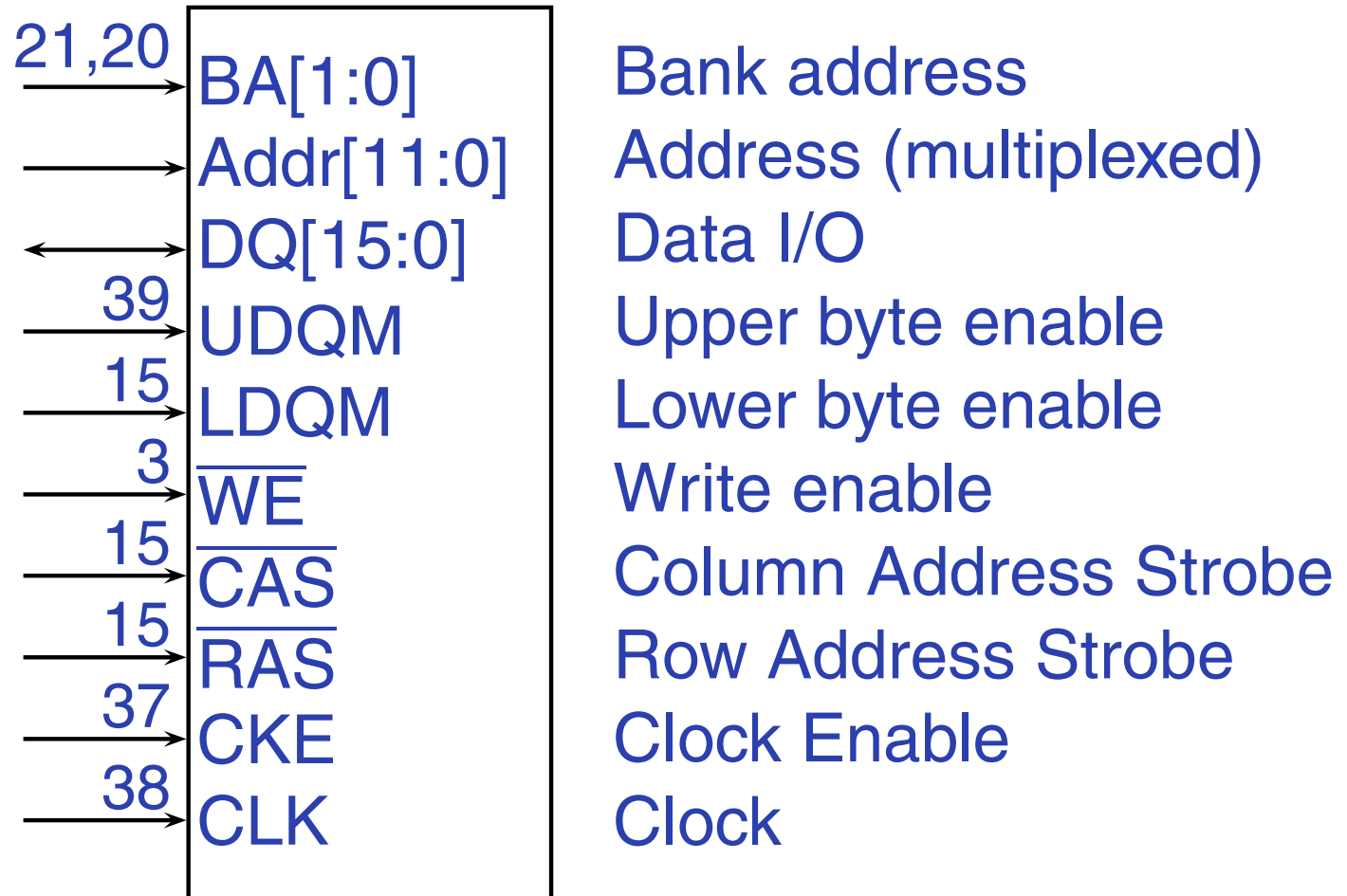
# Basic DRAM read and write cycles



# Page mode read cycle



# Samsung 8M × 16 SDRAM

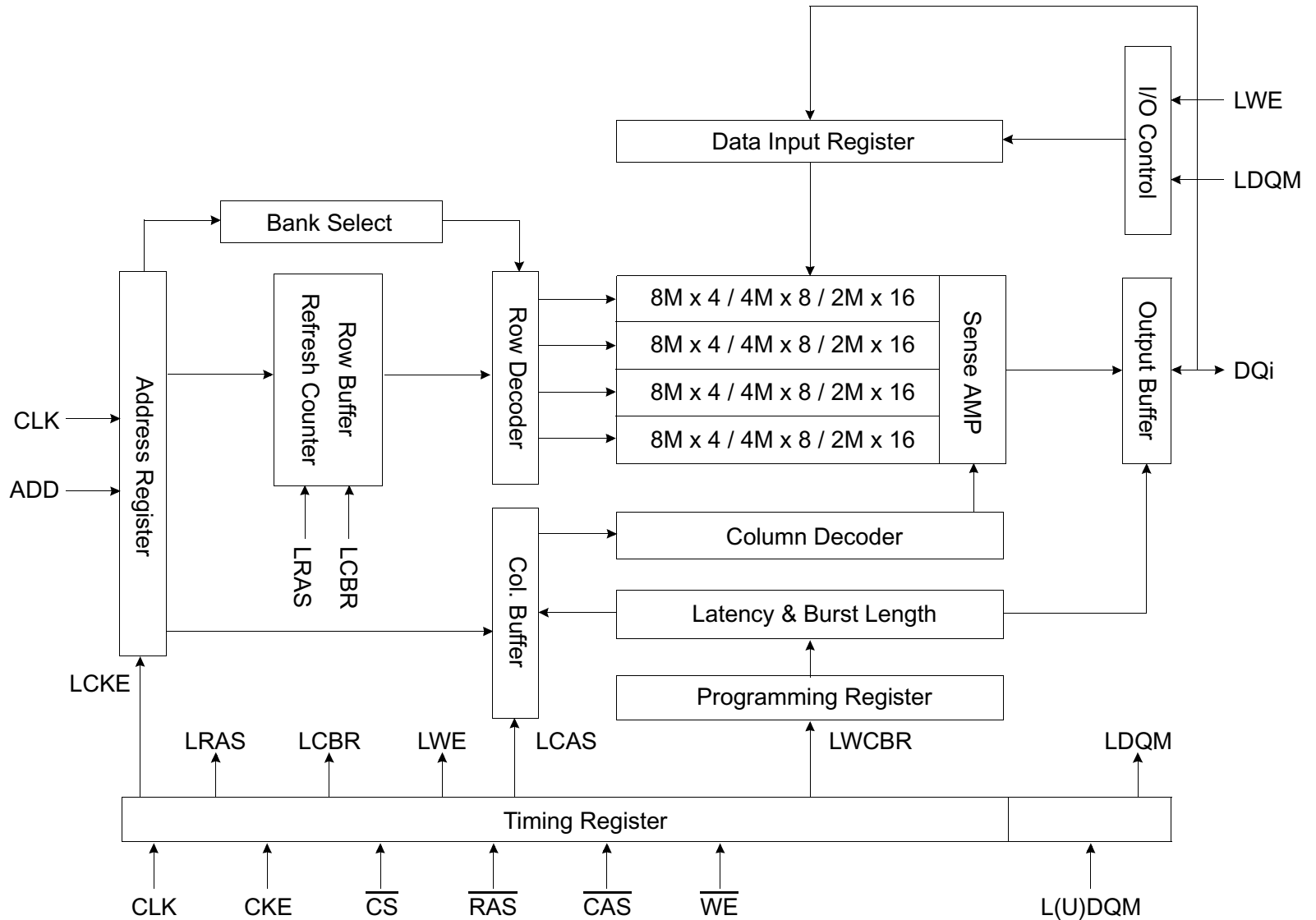


Synchronous interface

Designed for burst-mode operation

Four separate banks; pipelined operation

# Samsung 8M × 16 SDRAM



# SDRAM: Control Signals

$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	action
1	1	1	NOP
0	0	0	Load mode register
0	1	1	Active (select row)
1	0	1	Read (select column, start burst)
1	0	0	Write (select column, start burst)
1	1	0	Terminate Burst
0	1	0	Precharge (deselect row)
0	0	1	Auto Refresh

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write

# SDRAM: Timing with 2-word bursts

